

15th Pacific Northwest Test Workshop

aka: BAST 2006

Bodega Bay, California, Feb 28 – Mar 3, 2006

CALL FOR PARTICIPATION

Committee:

General Chair Emeritus:

Edward J. McCluskey, Stanford CRC

General Chair:

Siyad Ma, IDT

Program Chair:

Samy Makar, Azul Systems

Registration Chair:

Erik Volkerink, Agilent & Stanford CRC

Registration Co-chair:

Intaik Park, Stanford CRC

Industrial Donors:

Garry Gillette, Credence

Finance Chair:

Kyoung Youn (Ken) Cho, Stanford CRC

Entertainment Chair:

Davia Lu, Intel

Steering Committee:

Edward J. McCluskey, Stanford CRC

Subhashish Mitra, Intel & Stanford CRC

Siyad Ma, IDT

Mike Purtell, National Semiconductor

Samy Makar, Azul Systems

Program Committee:

Ravi Apte - Syntest

Phil Burlison, Inovys

R Chandramouli, Virage Logic

Jayabrata Dastidar, Altera

Scott Davidson, SUN Microsystem

Bill Eklow, Cisco Systems

Rohit Kapur, Synopsys

Kee Sup Kim, Intel

Mike Li, Wavecrest

Samiha Mourad, SCU

Bruce Parnas, Advantest

Bill Price, Philips

Mike Purtell, National Semiconductor

Burnell West, Credence

The 15th annual BAST workshop, co-sponsored by the Stanford University Center for Reliable Computing (CRC) and the IEEE Computer Society Test Technology Technical Council (TTTC)*, will be held February 28 – March 3, 2006, in Bodega Bay, California. BAST is an informal workshop whose objective is to bring together engineers from the Pacific Northwest to discuss current work on testing electronic circuits. Attendance at BAST is restricted to fewer than 50 persons in order to facilitate better sharing of ideas.

BAST workshop is *unique in that all attendees are on the program*; everyone attending is expected to stay at the workshop for its duration, and to participate. Interaction is encouraged during every presentation, and during breaks and social events. Programs and reports from previous BAST workshops are available from the web site listed at the bottom of this page.

Interested persons are invited to submit a proposal containing a brief abstract of what they would like to discuss. Possible suggestions include:

SOC and SIP Test Methodology
Low-cost ATE
Defect Behavior and Detection
Yield Analysis
Online Test and Robust Designs
Diagnosis
System Test
Reliability Screening
Quality Level Prediction
Test Cost

Test Compression
Validation and Verification
Mixed Signal Testing
Testing High Speed I/Os
BIST
Debug
At-Speed Testing
Failure Mode Diagnosis
Memory Test and Repair
DFM

This is not an exclusive list; all interesting abstracts related to test are invited for submission (see reverse side for application information). If you are interested in attending, please email a softcopy of your proposal immediately to:

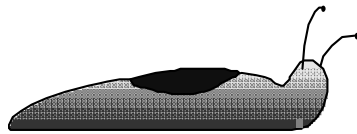
Erik Volkerink E-mail: volkerin@crc.stanford.edu
353 Serra Mall, Gates-2A, Room 234 Voice: 650-725-0487
Stanford, CA 94305-9020 FAX: 650-725-7411

Applications to attend the workshop will be considered on a first come first serve basis. Your proposal submission will reserve you a place and is not considered a commitment. **Invitations will be sent out promptly upon receipt of your proposal.** There is no on-site registration.

BAST web site: <http://crc.stanford.edu/BAST/BAST.html>

*Approval Pending

(See Reverse Side)



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Proposal for Participation, Please turn in immediately.

Name: _____

Address: _____

Tel.: () _____ Fax: () _____

E-Mail: _____

Company or University: _____

Referred by (Optional) : _____

ATTENDEE INFORMATION

Test Interests/experience	Title of Discussion	Previous BAST attendance
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Abstract of your discussion: (Please be brief)

(See Reverse Side)