

16th Pacific Northwest Test Workshop

aka: BAST 2007

Bodega Bay, California, Feb 27 – Mar 2, 2007

CALL FOR PARTICIPATION

Committee:

General Chair Emeritus:

Edward J. McCluskey, Stanford CRC

General Chair:

Siyad Ma, IDT

Program Chair:

Samy Makar, Azul Systems

Registration Chair:

Erik Chmelar LSI Logic & Stanford CRC

Vice Registration Chair:

Francois-Fabien Ferhani, Stanford CRC

Local Arrangements:

Jon Colburn, nVidia

Industrial Donors:

Laung-Terng Wang, Syntest

Finance Chair:

Kyoung Youn (Ken) Cho, Stanford CRC

Publicity Chair:

Erik Volkerink, Verigy & Stanford CRC

Entertainment Chair:

Davia Lu, Intel

Steering Committee:

Edward J. McCluskey, Stanford CRC

Subhasish Mitra, Stanford CRC

Siyad Ma, IDT

Kee Sup Kim, Intel

Program Committee:

R. Chandramouli, Virage Logic

Jayabrata Dastidar, Altera

Scott Davidson, SUN Microsystems

Rohit Kapur, Synopsys

Kee Sup Kim, Intel

Mike Li, Wavecrest

Samiha Mourad, SCU

Bruce Parnas, Advantest

Bill Price, Philips

Mike Purtell, Intersil

The 16th annual BAST workshop, co-sponsored by the Stanford University Center for Reliable Computing (CRC) and the IEEE Computer Society Test Technology Technical Council (TTTC)*, will be held February 27 – March 2, 2007, in Bodega Bay, California. BAST is an informal workshop whose objective is to bring together engineers from the Pacific Northwest to discuss current work on testing electronic circuits. Attendance at BAST is restricted to fewer than 50 persons in order to facilitate better sharing of ideas.

BAST workshop is *unique in that all attendees are on the program*; everyone attending is expected to stay at the workshop for its duration and to participate. Interaction is encouraged during every presentation, during breaks, and during social events. Programs and reports from previous BAST workshops are available from the web site listed at the bottom of this page.

Interested persons are invited to submit a proposal containing a brief abstract of what they would like to discuss. Possible topics include:

SOC and SIP Test Methodology

Low-cost ATE

Defect Behavior and Detection

Yield Analysis

Online Test and Robust Designs

Diagnosis

System Test

Reliability Screening

Quality Level Prediction

Test Cost

Test Compression

Validation and Verification

Mixed Signal Testing

Testing High Speed I/Os

BIST

Debug

At-Speed Testing

Failure Mode Diagnosis

Memory Test and Repair

DFM

This is not an exclusive list; all interesting abstracts related to test are invited for submission (see reverse side for application information). If you are interested in attending, please email a softcopy of your proposal immediately to:

Erik Chmelar

353 Serra Mall, Gates-2A, Room 234

Stanford, CA 94305-9020

E-mail: echmelar@crc.stanford.edu

Voice: 650-725-0487

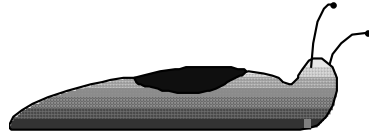
FAX: 650-213-8363

Applications to attend the workshop will be considered on a first come first serve basis. Your proposal submission will reserve you a place and is not considered a commitment. **Invitations will be sent out promptly upon receipt of your proposal.** There is no on-site registration.

BAST web site: <http://crc.stanford.edu/BAST/BAST.html>

* Approval pending

(See reverse side)



16th Pacific Northwest Test Workshop aka: BAST 2007

Bodega Bay, California, Feb 27 – Mar 2, 2007

Please complete this proposal for participation (fillable PDF) and return immediately via email, fax, or mail shown on reverse side.

Name: _____

Address: _____

Tel.: () _____ Fax: () _____

E-mail: _____

Company or University: _____

Referred by (optional) : _____

ATTENDEE INFORMATION

Test interests/experience	Title of discussion	Previous BAST attendance
Abstract of your discussion (please be brief):		

(See reverse side)