



BAST 2004 Workshop Program

Bodega Bay, California, February 24-27, 2004

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Tuesday, Feb 24

4:30 PM Registration

5:00 PM Reception, Dinner & After dinner remarks by Dr. Len Cutler.

Wednesday, Feb 25

- 7:00 AM CONTINENTAL BREAKFAST
- 8:15 AM Welcome E. J. McCluskey, General Chairman
- 8:20 AM Introduction Samy Makar, Program Chairman
- 8:30 AM **Session 1 Yield & DPM Modeling**
Session Chair: E. J. McCluskey Stanford CRC
- 1.1 A Simple Way of Computing Predictive Yields, *Scott Davidson, Sun Microsystems*
 - 1.2 Defect Levels of Pseudo-Random Testing, *Ahmad Al-Yamani, Stanford CRC*
 - 1.3 Product Quality is Predictable, *Paul Ryan, Intel*
 - 1.4 Firing Line: *Nirmal Saxena, Alliance, R. Chandramouli, Virage Logic*
- 9:30 AM- BREAK
- 10:30 AM **Session 2 Debug and Diagnostics**
Session Chair: *R. Chandramouli, Virage Logic*
- 2.1 How to Gain Debug Experience?, *Tony Altinis, Matrix Semiconductors*
 - 2.2 Rapid Defect Localization Techniques & Tester Interactions, *Marty Leibowitz, NPTest*
 - 2.3 System Test and Diagnostics, *Xinli Gu, Cisco*
 - 2.4 Firing Line: *Ken Skala, Credence, Nahmsuk Oh, Synopsys*
- 12:00 PM- LUNCH
- 1:30 PM **Session 3 Reducing Cost of Test**
Session Chair: *Bill Bottoms, 3MTS*
- 3.1 Software for an Open Architecture System, *Bruce Parnas, Advantest*
 - 3.2 Massively Parallel Wafer Test, *Garry Gillette, Credence*
 - 3.3 X-Compaction with Unbounded X's, *Erik Volkerink, Stanford CRC / Agilent*
 - 3.4 Firing Line: *Burnell West, NPTest, Alvin Jee, Neanderthal*
- 2:30 PM BREAK
- 3:30 PM **Session 4 SIP/SOC**
Session Chair: *Nirmal Saxena, Alliance*
- 4.1 Creating Patterns for a 0-Coverage SOC Design, *Samy Makar, Azul Systems*
 - 4.2 Memory Requirement for SIP, *Bill Price, Philips*
 - 4.3 Test Issues in Programmable Logic Devices, *Jayabrata Dastidar, Altera*
 - 4.4 Firing Line: *Bill Bottoms, 3MTS, Huong Nguyen LSI Logic*
- 6:00 PM DINNER FUN & GAMES

Thursday, Feb 26

7:00 AM CONTINENTAL BREAKFAST

8:30 AM **Session 5 GHZ Test**
Session Chair: *Rudy Garcia, NPTest*

- 5.1 RF Test is Mars, Digital Test is Venus, *Mark Roos, Roos Instruments*
- 5.2 Testing At-Speed Digital to 1.2 GHz, *Gary Fleeman, Advantest*
- 5.3 Jitter Transfer Function and its Relationship to the System, *Mike Li, Wavecrest*
- 5.4 Firing Line: *Saleh Moussali, LSI Logic, Davia Lu, Intel*

9:30 AM BREAK

10:30 AM **Session 6 System Level Test**
Session Chair: *Samiha Mourad, Santa Clara University*

- 6.1 System Level Insertion in a co-verification environment, *Bill Eklow, Cisco*
- 6.2 System Test: Challenges and its Future, *Kee Sup Kim, Intel*
- 6.3 Design for Availability: Implications of Robust System Design on Test, *Burnell West, NPTest*
- 6.4 Firing Line: *Yuhai Ma, Advantest, Francois Ferhani, Stanford CRC*

12:00 PM LUNCH

AFTERNOON: INDIVIDUAL DISCUSSION

7:30 PM **PANEL DISCUSSION**
At Arena Cove Lounge
Can the ATPG-ATE Gap be Reduced?

Moderator: *E. J. McCluskey, Stanford CRC*
Panelists: *Jim Sproch, Synopsys*
Samy Makar, Azul Systems
Marc Loranger, Credence
Mike Purtell, Advantest

Friday, Feb 27

7:00 AM CONTINENTAL BREAKFAST

8:30 AM **Session 7 Delay Test**
Session Chair: *Phil Burlison, Inovys*

- 7.1 Performance, Yield, Statistical Analysis and Test, *Dwayne Burek, Magma*
- 7.2 Can we Delay Test a Few Paths in the Circuit and Make Conclusions About the Remaining?, *Manish Sharma, Nvidia*
- 7.3 Delay Testing Using Process Monitors, *Subhasish Mitra, Intel*
- 7.4 Firing Line: *Donghwi Lee, Stanford CRC, Charlie McDonald, Logic Vision*

9:30 AM BREAK

CHECKOUT (before noon)

10:30 AM **Session 8 Quality and Yield**
Session Chair: *Mike Purtell, Advantest*

- 8.1 Infrastructure IP for Manufacturing and Field Maintenance, *R. Chandramouli, Virage Logic*
- 8.2 Detection of Systematic Defects, *Bob Madge, LSI Logic*
- 8.3 Test and Fault Tolerance in sub-100 Nanometer Circuits, *Jacob Abraham, UT Austin*
- 8.4 Firing Line: *Jon Colburn, Nvidia, Rathish Jayabharathi, Intel*

11:30 AM Closing Remarks. Questionnaire Collection

12:00 PM LUNCH