



# Ninth Pacific Northwest Test Workshop

aka: BAST 2000

Bodega Bay, California, Feb 15 - 18, 2000

## CALL FOR PARTICIPATION

**Committee:**

**General Chair:**

E.J. McCluskey, Stanford

**Co-General Chair:**

R. Chandramouli, Synopsys

**Program Chair:**

Hong Hao, LSI Logic

**Entertainment Chair:**

Davia Lu, IBM

**Local Arrangements:**

Siegrid V. Munda, Stanford

**Co-Local Arrangements Chair:**

R. Chandramouli, Synopsys

**Publicity Chair:**

Mike Purtell, Advantest

**Registration Chair:**

Chao-Wen Tseng, Stanford

**Finance Chair/IEEE Liaison:**

Catherine Yu, Stanford

**Steering Committee:**

E.J. McCluskey, Stanford

R. Chandramouli, Synopsys

Siyad Ma, Chameleon

Mike Purtell, Advantest

**Program Committee:**

Henry Chang, Cadence

Scott Davidson, Sun

Bob Huston, Credence

Rohit Kapur, Synopsys

Eric Larson, Teradyne

Mark Levitt, Sonics

Samy Makar, Cirrus Logic

Tony Taylor, Fluence

John Waicukauski, Synopsys

David Wu, Intel

The 9th annual BAST workshop, co-sponsored by the Stanford University Center for Reliable Computing (CRC) and the IEEE Computer Society Test Technology Technical Committee (TTTC)\*, will be held Feb 15 -18, 2000, in Bodega Bay, California. BAST is an informal workshop whose objective is to bring together engineers from the Pacific Northwest to discuss current work on testing electronic circuits.

Attendance at BAST is restricted to 50 persons in order to facilitate better sharing of ideas. This workshop is unique in that attendee-only reservations are not available; everyone is on the program and all are expected to stay at the workshop for its duration. Interaction is encouraged during every presentation, and during breaks and social events. Programs and reports from previous BAST workshops are available from the web site listed at the bottom of this page.

Interested persons are invited to submit a proposal containing a brief abstract of what they would like to present. Possible topics include:

**System on chip test methodology**  
**Impact of deep sub-micron test on ATE**  
**Design for debug and testability**  
**Fault coverage and fault models**  
**Test research**  
**Online test**

**Mixed signal testing**  
**Design for debug and testability**  
**Verification**  
**Embedded memory test**  
**Future test issues**  
**Testing high speed designs**

This is not an exclusive list; all interesting abstracts related to test are invited for submission (see reverse side for application information). If you are interested in attending, please send a proposal for participation by November 12, 1999 to:

Siegrid Munda  
 Gates Bldg. 2A  
 Stanford, CA 94305

E-mail: munda@crc.stanford.edu  
 Voice: 650-723-1258  
 FAX: 650-723-1451

Applications to attend the workshop will be considered on a first come first serve basis. **Invitations will be mailed out promptly upon receipt of your proposal.** There is no on-site registration.

Bast web site: <http://www-crc.stanford.edu/BAST/BAST.html>

\* Pending



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## Proposal for Participation, Abstracts due: November 12, 1999

Name: \_\_\_\_\_

Address: \_\_\_\_\_  
\_\_\_\_\_

Tel.: (    ) \_\_\_\_\_ Fax: (    ) \_\_\_\_\_

E-Mail: \_\_\_\_\_

Company or University: \_\_\_\_\_

### ATTENDEE INFORMATION

Test Interests/Experience	Title of Discussion	Previous BAST Attendance
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