

A Report on the 9th Pacific Northwest Test Workshop (BAST 2000)

BAST 2000 was held in Bodega Bay, California from February 15 through February 18, 2000. The objective of this workshop, co-sponsored by the Stanford University Center for Reliable Computing and the IEEE Test Technology Council, is to bring together test professionals from the Pacific Northwest to discuss current work on testing electronic circuits and systems. Attendees from academia, and from the Automatic Test, Semiconductor, and Design Automation industries provided a broad perspective of presentations and discussions. After the opening night dinner, distinguished guest speaker Dr. Ted Hoff gave an interesting talk. He is credited with inventing the microprocessor, an invention that eventually became the Intel 4004. Dr. Hoff was presented with a BAST distinguished speaker award following his talk. The remainder of the workshop consisted of 8 technical sessions, and a panel session.

The first technical session posed the question "Testers – Do they always tell the truth". One speaker pointed out that problems such as test generation, test coverage, and device node controllability and observability are not new, they are just getting worse. It was suggested that accuracy, speed, pin count and cost are not problems, even though industry consortia suggest otherwise. A novel test architecture with a limited number of channels to access test structures with high accuracy and speed, combined with low speed/low cost channels connected to the majority of device pins would alleviate many economic problems. A presentation was made that discussed test problems not detectable or supportable by device simulation software, such as calibration errors caused by drive and compare level changes, power supply problems caused by high rate of change of current (di/dt), socket effects, and round trip delay associated with bi-directional signals. Another presenter discussed testing source synchronous designs like Fibre Channel that embed the clock signal with the transmitted data. As cycle times have decreased from around 10nS to 1nS, it is very difficult to set timing guard-bands for accurate data detection by the tester.

The “Testing SOC” session included a discussion about communication based designs, and suggested that popular industry standardization groups do not adequately support them. Another presenter suggested that tester hardware be included in the platform based design environment to support manufacturing. A platform-based design uses a common set of circuit elements, subsystems, manufacturing and operations resources to implement large numbers of product variants that can be sold to a variety of market segments. A third presenter provided architectural suggestions to support IDDq measurement, such as providing current isolation between modules, and planning for IDDq testability in the early stages of the design rather than as an afterthought.

The “Functional Verification “ session started with more discussion about platform based design. A recommendation was made to base designs on platform template architectures, and to use these architectures for testing. One way to do this is merge test and verification. Other presenters talked about using test-related ideas to solve verification problems and a provided a recommendation to validate testability at the RT level.

The session titled “Myths vs. Data” provided insights mined from data collected during the Murphy test chip experiment conducted by Stanford University. Effectiveness of the stuck fault model applied to test vector generation, and the dependence of vector ordering, even for combinational circuits, was discussed. Surprising to most was that vector ordering did effect test results, which is contrary to conventional wisdom. Another presentation covered low temperature testing as a methodology for delay defect screening, and provided explanations of defects caused by open silicide and dark vias. The last presenter in this section described how tunneling opens cause a very high IDD current immediately after a state transition, followed by a gradual decrease over time. VLV (Very Low Voltage) testing and multiple continuous IDDq measurements are effective in detecting the tunneling opens.

The “VLSI Test – What’s Ahead?” session presented data showing that the pace of progress is much faster than predicted by industry experts. This was followed by a presentation describing high volume microprocessor test challenges, including those that are side effects of using copper and SOI processes, and

reduced feature sizes. The final presenter of this session made an interesting talk about the futility of designing test languages, and suggested an approach involving products with extensible capabilities, such as XML.

The session titled “Design and Test Methodologies” included a presentation about using a closed loop method for generating and verifying ATE test programs in a simulation environment. This loop involves device simulation, pattern development and debug, translation to ATE, and playback for comparison with the original device simulation output. A presentation about fault grading recommended the use of system level metrics to measure the quality of system test and to identify regions of poor test coverage. This could also be used to reduce the number of redundant tests, which would lower overall test cost. The final presenter in this session talked about BIST methodologies for D/A and A/D converters.

The “Application Specific Testing” session included a discussion about using synthesis tools for designing circuitry placed between the ATE system and device under test. These types of circuits, which are used for signal conditioning and relay switching when limited tester resources must be connected to multiple device pins, are often designed by the test engineer in an ad hoc manner. The use of synthesis tools would reduce the development time for these circuits, provide less reliance on the skill of the test engineer, and improve test quality. Other presentations described methods for reducing mixed signal test development time, and using the ATE software to test the accuracy of DSP computation offline, without using actual silicon or the test system.

The final session of BAST 2000 discussed “Testing Full Custom IC’s”. The first presenter described FPGA test challenges, which led to questions about how to test un-programmed FPGAs, and how to compute fault coverage based on the circuit design and the unused portions of the chip. A process for grading fault coverage when testing FPGA circuits, which is ongoing work, is needed. Another presenter talked about microprocessor debug problems and challenges, and the final presenter of BAST 200 discussed using BIST for testing of embedded memories to reduce ATE pin count requirement.

A panel session posed the question “Testing High Speed Designs – Can we do it or is it an oxymoron?” Discussions included the widening gap between capabilities of ATE, and the performance and specifications of devices under test, the inability to test complex circuits at high speed with data collisions, and the limitations of test and fault coverage analysis. In many cases, people are misled into believing that fault coverage is sufficient, when in reality it is not. One of the panelists suggested that test at any cost is viable in the design stage, but not in manufacturing. Attendees of the panel session raised many interesting issues, including the poor capability of ATE in synchronization with a device generated clock, and the assertion that ATE users spend twice as much money programming ATE than what they spend for purchasing the test system.

The workshop was organized by Edward .J. McCluskey of Stanford University, and Hong Hao of LSI Logic. In addition, Chaowen Tseng, Catherine Yu, Davia Lu and Mike Purtell served as , registration, finance, entertainment and publicity, chairs respectively. Local arrangements were managed by Siegrid Munda and Nahmsuk Oh. The tenth BAST workshop will be held in February 2001.