A Report on the 10th Pacific Northwest Test Workshop (BAST 2001)

BAST 2001 was held in Bodega Bay, California from February 6 through February 9, 2001. The objective of this workshop, co-sponsored by the Stanford University Center for Reliable Computing and the IEEE Test Technology Council, is to bring together test professionals from the Pacific Northwest to discuss current work on testing electronic circuits and systems. Attendees from academia included participants from Stanford University, Santa Clara University, UC Davis, and UC Santa Cruz. Industrial participants were from eight Automatic Test Equipment companies, nine Semiconductor companies, five Design Automation companies, and two Electronic System companies. This mix of attendees provided a broad range of presentations and discussions throughout the eight technical sessions, and the panel session. A copy of the technical program, including participants and affiliations, is available on the BAST website.

A session about BIST included a talk about using this technique for the detection of real defects. One speaker discussed using multiple LFSR seeds to reduce pattern length and application times, and also covered the use of test points, mapping logic, and weighted random BIST. Two other speakers described difficulties they have encountered using BIST, including problems with the software tools, the effects of BIST on circuit performance, power issues, lack of consensus on a use model and the lack customer requirements.

The "FPGA and Memory Test" session included a talk about test methods and challenges related to complex programmable system chips containing GHZ speed serial links, PLLs, and embedded cores. Cores often include test patterns with high coverage, so they are not a major challenge, however analog and differential signals faster than most ATE, closed loop response tests, interconnect routing, PLD size/complexity, and the large number of current and voltage measurements impose many challenges. Another presenter discussed the impact of embedded DRAM yield, which showed a chip containing blocks with yields of 85%, 90%, 25%, and 20%. Putting these blocks together on the same piece of silicon resulted

in a chip with no yield at all. The third speaker in this session talked about FPGA fault coverage and fault models, stressing the fact it is impossible for an FPGA manufacturer to anticipate and test all possible signal routes that a customer might use while designing a circuit. This imposes a huge burden on test.

The session titled “El Cheapo Testers” covered the effects of feature and performance compromise related to tester cost reduction. The first speaker described a cost model based on units tested per hour per $1000.00, and then described distributed test strategies using different test sets at probe and packaged device test stages. His conclusion was that tester throughput has much more effect on test cost than the purchase price of ATE. The next speakers described why “El Cheapo” tester customers do not tolerate major performance or feature reduction even from lower cost machines. The major differences between full featured and low cost testers now were asserted as being total pin count, parallelism, power consumption, vector memory depth, minimum pulse width, and pattern/timing generation architecture. These differences are all hardware related; low cost and full-featured testers need to have the same test programs and test tools. The third speaker in this session provided reasons why some testers cost as much as $10K per pin. These reasons included the necessity for test head cooling, fractional bus architectures requiring multiple pattern generators, and the requirement for tester device power supplies to deliver as much as 300 amperes to some devices. This speaker disputed estimates of future tester prices as high as $20M, stating that the estimate is wrong, and at that price there would not be any customers.

The “Core Test” session started with a presentation about Virtual Socket Interface Alliance (VSIA) test architecture, which provides accessibility to Virtual Components (VCs), enabling standalone tests of all VCs on a system chip, as well as interconnects and user defined logic testing. Similarities and differences between the VSIA architecture and the IEEE P1500 scalable test architecture, which both have similar objectives were discussed. The next speaker discussed methodologies used by his company for testing System on Chip (SOC) devices designed with test shells around each core, allowing each to be tested independently of the system chip. A large number of scan chains is used to reduce the time needed for transport of data from the IC to the tester. The final speaker of this session discussed the testing of mixed signal SOCs, and described techniques for reducing the analog simulation times by using adaptive

regression models, and simulating only the non-ideal circuit elements. A simulation estimated to take nearly 3 months to complete was reduced by a factor of more than 100, with only 0.3% error compared with the full simulation.

The "Optimizing Test " session started with a talk about test resource partitioning to reduce cost. An equation to calculate test cost that factored in the ATE and handler, total test time, and parallelism was presented. A distributed approach employing different test methodologies throughout manufacturing was recommended. Distinct test methodologies are capable of finding unique defects, however test cost reduction pressures require these methodologies to be used on different testers, and at different manufacturing test steps. Another speaker compared the fault coverage of two types of memory Built in Self Test (BIST) with checkerboard tests based on physical memory locations rather than logical addresses. The speaker concluded that the checkerboard test based on physical memory locations achieved slightly higher fault coverage than the BIST tests, however the physical address mapping is not always available, particularly when the memory is provided as a core for inclusion in a system chip, or as part of a system chip design. The last speaker of this session recommended a test cost model that includes front-end costs, such as simulation, synthesis, DFT insertion, layout, manpower, and resource consumption.

The "New Failure Mechanisms for Trans Gigahertz " session included a talk about new failure mechanisms that will emerge as local and cross chip clocks achieve speeds of 4.1GHz and 2.2GHz respectively. Failure mechanisms related to radiation, coupling, and noise are exacerbated by the limitations of orthogonal lithography, which uses sharp corners along signal routes and produces reflections that are insignificant at lower speeds. Effects such as edge pulling and undesired signal synchronization were also described. Another talk about the structured testing of AC coupled nets described the difficulty of applying low frequency measurement techniques to AC coupled paths that are optimized only for high frequency transmission. These circuits are not well supported by standards recommended by the VSIA or the P1500 groups, so either a new standard or an extension to an existing standard is needed. Ideally any new standard would not disturb existing test structures related to 1149.1 boundary scan. A third presenter in this session talked about test sensitivity analysis of open vias in deep sub micron devices.

The “Detecting and Diagnosing Failures“ session included two interesting talks related to the experimental test chip known as Murphy. The first speaker described a technique known as MinVDD, in which the minimum voltage for which a chip can operate is determined, using extremely relaxed timing and AC test conditions. Chips with a MinVDD greater than most devices are considered early life failure candidates. The second talk related to the Muphy chip described a diagnosis technique for sequence dependent failures. An interesting example of a possible sequence dependent fault in a NAND gate, where an open defect caused an expected logic high output level to float when the input pattern was ‘01’ was described. When the previous input pattern was ‘11’, with an expected output logic level of 0, the defect was detected. Any other pattern preceding the 01 input pattern allowed this fault to escape detection. Applying vectors in the effective sequence, in multiple sequences helps diagnosis and detection of sequence dependent faults. The third speaker in this session talked about using DFT tools as part of failure diagnosis, for tasks like test program optimization, scan data volume reduction using logic BIST, sequential ATPG, and test point insertion. Scan chain optimization was proposed for hierarchical SOC, with static timing analysis for scan chain setup and hold timing violation detection. Sample design flows were presented for high-level design and ATE flows.

The session titled “Test Methods” included two presentations related to analog and mixed signal testing. The first presenter described the application of test methods for verification of simple circuits combining optical and mechanical components. The second speaker talked about PLL test and characterization, describing tests such as lock, jitter, step and modulation response. This session concluded with a talk about data path direct access test as an alternative to full scan testing. This provides the same benefit as scan at a reduced cost, and enables automated test pattern generation for data blocks.

A panel session theme of “Guaranteeing Quality Throughout the Product Life Cycle – On-Line Test and Repair to the Rescue” covered several interesting scenarios, including whether or not there are defects yet to emerge that are not detectable using current production test methodologies. Interesting

discussions also included concurrent error detection, and consideration of whether the majority of future defects will be AC or DC in nature. The role of software in fault tolerance and fault repair was also discussed.

The workshop was organized by Edward .J. McCluskey of Stanford University, and Scott Davidson of Sun Microsystems. In addition, Subhasish Mitra, Ray Chen, Davia Lu and Mike Purtell served as registration, finance, entertainment and publicity chairs respectively. Local arrangements were managed by Siegrid Munda and Mike Purtell. The eleventh BAST workshop will be held in February 2002.