A Report on the 11th Pacific Northwest Test Workshop (BAST 2002)

BAST 2002 was held in Bodega Bay, California from February 5 through February 8, 2002. The objective of this workshop, co-sponsored by the Stanford University Center for Reliable Computing and the IEEE Test Technology Council, is to bring together test professionals from the Pacific Northwest to discuss current work on testing electronic circuits and systems. Attendees from academia included participants from Stanford University and UC Davis. Industrial participants were from Automatic Test Equipment, Semiconductor, Design Automation, Electronic System, and Computer companies. This mix of attendees provided a broad range of presentations and discussions throughout the eight technical sessions, and the panel session. A copy of the technical program, including participants and affiliations, is available on the BAST website.

The workshop opened with a session covering production test solutions for SOC (System on Chip) and SIP (System in Package) circuits using a partition test strategy. One speaker reviewed the history of DFT (Design for Testability) adoption, such as Scan and BIST (Built in Self Test). The complexity of modern devices, partitions used for data compress/decompress, re-configurable logic, clock generation, I/O wrap and core access were described, The speaker stated that other things likely to invade DFT include processors as BIST engines, bus structured test logic, and diagnosis programs stored on chip. A talk about test challenges for SIP described the limitations of SOC technology, including mixed functions and processes, as a justification for the use of System in Package solutions. Manufacturing strategies such as redundancy to enable reparability were covered. The final speaker of this session talked about test economics for multi-site test, with suggested cost reduction techniques.

The next session on production test started with a talk about test pattern data hierarchy in a structured test environment. The traditional test development process with a wall between design and test groups was contrasted with a structural test development process. A complicated process called pattern munging, used with patterns to support multiple cores, poses challenges as these patterns must be supported by a wide pattern covering all device pins, and a deep pattern to test all of the device functions, while maintaining the integrity of the system and all cores. A presentation was made about combining die information to improve pass/fail decisions, using a delayed binning technique to reduce the cost of device production, and to reduce the number of test errors. The final speaker of this session talked about DFT and production testing, and warned that with

test development cost accounting for 40% of the total device cost, and increasing, it is very important to adopt DFT wherever possible. This speaker also discussed the use of intelligent test flows that optimize production time by automatic reordering of tests.

The third session covering debug started with a talk about "Model-based" approaches to debug functional failures at board level. The model defines the extent to which logic is used during each of the functional tests. Good experimental results given the simplicity of the model achieved nearly 85% success rate after 2 repair attempts. The next speaker discussed challenges and advances in debug and diagnosis, describing the root cause difference between expected behavior and golden device performance. The final speaker presented data from the Murphy Chip experiment that showed the correlation of timing independent faults with single stuck-at fault models. A significant number of the timing dependent faults were shown to have a sequence dependency. Clustered defects and multiple faults were also discussed.

The fourth session titled "Beyond Digital Test" concluded the first day of the workshop. The first talk described the test challenges for optical products, such as jitter modulation with a 1Gs/s AWG (Arbitrary Waveform Generator), using independent timing sets. The speaker mentioned a loopback test where 11% of devices that passed functional tests failed jitter performance. The next speaker described the generation of WCDMA receiver baseband/IF test signals using a 4Gs/s AWG. These signals have a 5MHz spread spectrum centered at 161MHz, with controllable Error Vector Magnitude for receiver tolerance evaluation. The final speaker of the day talked about the limitations of conventional solutions in digital ATE. The conclusion of this talk was that tester hardware could only keep up with device gate counts at a reasonable cost if DFT and BIST are used.

Session 5 on Test Quality started with a talk about ATPG for defect-oriented test. The first speaker cited data showing that the bridge fault coverage of functional vectors is about 50%, compared with 30% to 40% for ATPG generated vectors. This led to a discussion of ways to improve test quality using commercial tools and circuit models. The next speaker described an academic developed tool for grading test vectors against a metric called TARO (Transition Sensitized to all Reachable Outputs). The speaker also talked about an automatic test pattern generation program to generate test vectors with100% TARO coverage. The final talk of this session discussed stuck at and transition n-detect fault coverage of pseudo random and deterministic patterns.

"Test Past, Present, and Future" included discussions about BIST, industry road maps, and a 10-billion transistor IC. The first speaker thanked the tester vendors for providing faster machines with deeper pattern memories, allowing him to avoid the use of logic BIST. This speaker mentioned that 38% of device cost is consumed by IC testing. The next speaker talked about inevitable change in industry and technology, and stated the manufacturers are likely to continue with functional test. The third speaker talked about a 10 billion transistor IC expected in 2010, and mentioned that the production volumes for such a chip will be very high, and will require flexibility and versatility at the application level.

The "Functional Test" session started with a talk about $1.00 /pin testers. Parallelism and highly integrated tester electronics were suggested as cost reduction methods, while faster test pattern generation provides lower test program development cost as a way to attain this goal. It was suggested that tester power consumption is one of the best indicators of test cost. The next speaker talked about grading functional vectors for the diagnosis of sequence dependent faults. The third speaker talked about the need for functional testing, with emphasis on at-speed tests. This speaker described the problems of cycle uncertainty, and that low speed single stuck-at tests can miss many defects.

The final session of Bast '02 covered the topic of test compaction. The first speaker predicted factor of 10 improvements in test time by using compressed stimuli from the tester, with decompression on chip. The device outputs also pass through a compactor to shorten the length of the tester comparison data. A raw device without test compression used 16 scan chains, and 2590 scan cycles per chain. The same device with test compression required only 253 scan cycles for each of the 16 scan chains. The next speaker, who talked about ATPG to target multiple faults, and fault simulation of reordered patterns, addressed compaction issues. The recommendations of this speaker were to use DFT to insert observe/control paths, encode optimized ATPG patterns, and to use MISRs (Multiple Input Shift Registers) to compact responses. The final speaker at BAST '02 talked about efficient response compaction, showing methods to realize an exponential reduction in the number of scan out pins using compaction techniques.

A panel session with a theme of "How do we find Failures in the Chips of Tomorrow" generated a lively discussion between the 4 panelists, moderator, and attendees. Some of the challenges mentioned for finding these failures included 40 Gb/s data rate of OC-768 devices, with thousands of pins per device. A

pessimistic viewpoint that high yield might not be affordable in the future was offered in contrast to an optimistic opinion that quality is improving, even though failures are emerging from new sources.

The workshop was organized by Edward J. McCluskey of Stanford University and Subhasish Mitra of Intel Corporation; Scott Davidson of Sun Microsystems was the program chair. In addition, James Li of Stanford University, Sungroh Yoon of Stanford University, Davia Lu of IBM Corp. and Mike Purtell of Advantest Corp. served as registration, finance, entertainment and publicity chairs respectively. Mike Purtell managed local arrangements. The twelfth BAST workshop will be held in February 2003.