

## **A Report on the Seventh BAST Workshop (BAST'98)**

The objective of this workshop, cosponsored by the IEEE Test Technology Technical Committee and the Stanford University Center for Reliable Computing is to bring together test professionals from the Pacific Northwest to discuss current work on testing electronic circuits and systems .

The evolving deep submicron technology has enabled the design of complete systems on single chips. In order to keep up with the silicon potential, designers will have to understand various test issues that arise out of the new design paradigm, system-on-a-chip (SOC). Some of the critical test challenges discussed by the speakers were, test of individual cores, isolation of cores, logic between the cores and interconnect test at the chip level and finally, the ability to debug and diagnose at the chip level. Various access schemes that help in providing access to cores from chip I/O were discussed. It was also pointed out that the test methodologies differ for different types of cores such as soft and hard cores. For hard cores, some manufacturers require a bypass mode during test so that core under test can be isolated for test application.

Since ATPG will still play a key role for manufacturing test, the next generation ATPG tools for SOC test must concentrate on standard user interfaces. According to the speakers, most of the problems in test generation software were attributed to user interfaces and not to the underlying test generation algorithms and heuristics. Some of the key interfaces are with respect to library, netlist and patterns. In the case of libraries, the user should be able to use standard simulation libraries, the netlist should be in one of the standard languages (e.g., Verilog, VHDL, Edif, etc) and the patterns should be in a standard format (eg., STIL, WGL, etc). One of the speakers was of the view that behavioral level analysis of the design can help in speeding up the performance of the ATPG tool. According to him, the key is to learn from humans as to how tests can be created. The learning process can be codified to work at the RT level for test generation. This is an approach that can be used to generate tests for soft cores (RT level descriptions).

One of the speakers raised the general issue of differing fault coverage metrics between ATPG tools. According to him different ATPG tools generate different fault coverages for the same design. The coverage difference between tools is easily in the range of 2-5%. This has been attributed to multiple definitions of fault types (eg., untestable, undetectable, etc) and formulas for the calculation of fault coverage. His suggestion was to standardize fault coverage calculations across all the ATPG tools. In the case of bridging faults, one of the speakers spoke on the results of fault simulation on a 228K gate design. The bridging faults were simulated at the gate level and it was found that most bridges were covered by stuck-at fault tests. About 5-10% of the bridging faults needed spice-level models. It was suggested that the inclusion of bridging fault test at the production stage improved the quality significantly. Another speaker working on Iddq measurement for very low power devices, showed that test escapes can occur due to test set ordering.

Fundamental changes to tester (ATE) architecture were proposed to cope with the rising cost of ATEs. For example, it was predicted that a 5500 pin tester would cost around \$55M. Some of the changes are , dual transmission line architecture for bi-directional signals, improved clock/signal distribution for high-frequency testing. The presence of BIST and scan on devices will not eliminate the need for testers. But testers should improve their hardware to match device requirements. Another area of higher cost is the development of test program using various different test formats. The solution is a common format that is independent of the tester architecture. STIL , similar to WGL is one such format that is being balloted on by the IEEE standards committee for adoption by the test community.

Even with advanced ATE architectures, diagnosis becomes an issue, if chips are not designed for it. In diagnosing devices, the cost of locating faults increases at various levels of chip integration. Two approaches to fault location were described where one uses a fault dictionary approach, and the other one uses a localized fault simulation approach. The use of a bridging fault model along with the traditional stuck-at model is becoming an essential part of diagnosis methodology. Bridging faults are used to model signal shorts.

While solutions for digital test are reasonably established, both mixed-signal and analog testing are still in their infancy. Various speakers described some of the common problems associated with the diagnosis of analog or mixed signal systems. One of the examples was the test of optical sensors. The user will have to generate a light source as DUT input. The light source should be available in production environment. The use of BIST for ADC designs is a promising start, but needs to be refined further for mass adoption.

A panel session debated whether the evolving test technology can handle current and future IC designs with “monster specs” (GHz frequency, 5-10K I/O, 50-100M devices, etc). There was optimism that the test community can handle the “monster” chip test problems. However, following were some of the salient comments that came out of the panel session.

- It is tough to build a tester that can test at 100ps accuracy. By the time a tester is designed, the designs are 3-4 years ahead of the tester
- Use of BIST to contain tester data volume and data bandwidth.
- Make intelligent use of microprocessors for testing other parts on a chip. This can also be called soft BIST
- Debug capabilities have to be built into designs
- The fundamental problem in current tester architecture is its reliance on synchronism with respect to a single clock.

The workshop was organized by E.J. McCluskey, Stanford University and R.Chandramouli, Synopsys. In addition, Siyad Ma, Subhasish Mitra, Siegrid Munda, Philip Shirvani, Jonathan Chang, Davia Lu and Carol Tong contributed ably as program co-chair, registration, local arrangements, finance, publicity and entertainment chairs respectively. The eighth BAST workshop will be held in Feb 1999 at Bodega Bay, CA.