

A Report on the Eighth BAST Workshop (BAST '99)

BAST '99 was held in Bodega Bay, California from February 23 through February 26, 1999. The objective of this workshop, co-sponsored by the IEEE Test Technology Committee and the Stanford University Center for Reliable Computing, is to bring together test professionals from the Pacific Northwest to discuss current work on testing electronic circuits and systems. The workshop began with a talk from a distinguished opening speaker, Professor John McCarthy of the Stanford University department of Computer Science. Prof. McCarthy, who originated the LISP programming language, talked about his early research in the development of general-purpose time sharing computer systems. The opening speaker was followed by 8 technical sessions consisting of test and design related presentations, and a panel session.

The first technical session analyzed results of various test industry experiments. One presenter showed a statistical analysis of data comparing the effectiveness of IDDQ, Functional, Stuck-At, and AC tests. New results on the Stanford CRC/LSI Logic testchip experiment were reported by another speaker, including transition fault and IDDQ test results. The speaker also showed that most of the bad parts failed every single test set. The third speaker compared fault simulation for different bridging fault models on a real microprocessor design using scan-based single stuck-at patterns. Each of the 3 presentations showed that the single stuck-at test can detect most defects.

The next session discussed test problems with current designs, such as embedded memory structures and mixed-signal cores in a deep submicron process technology. With complex memory cell structures and mixed-signal designs, new failure mechanisms are expected. Other test challenges are by-products of the new processing technologies, such as SOI (Silicon on Insulator) and copper interconnects. One presenter showed that it was possible to improve the overall chip quality by modifying the designs of the standard cells in a deep submicron design.

Virtual Test presentations, from ATE vendor and third party software development perspectives, provided interesting viewpoints of this technology. Virtual test enables simulation of the tester environment using models of the tester interface and the device. This allows engineers to develop accurate test programs and hardware before availability of the first silicon. One of the attendees at BAST '99, a user of the third party virtual test software, added interesting questions and comments to the vendor oriented presentations. Another presenter in this session discussed issues in test vector translation, used for delivery of test vectors from event based simulation environments to cycle based ATE test systems.

There was a session dedicated to analog and mixed signal design and test issues. In addition, at least four other sessions included presentations related to mixed signal. Presentations included testing high-resolution A/D converters (16 or more bits), and two presentations on using low voltage testing techniques to find elusive faults in Phase Locked Loop (PLL) circuits, and opamps. Presentations made in other sessions related to analog and mixed signal testing included a talk about Current and Future Challenges for Design and Test of Mixed Signal IC's, Mixed Signal Test on VLSI Testers, and Analog BIST.

Two ATE companies made presentations in a session on Distributed test. One of these presenters advocated a technique called BOST (Built Off Self-Test), which uses an active load board with BIST like structures, saving the space on the die that would be used for on-chip BIST structures. The other presentation on this topic was titled "Does BOST make sense". Conflicting opinions on this topic made this session very interesting.

System Chip design and test continues to be a popular topic. The session on system chip test included a representative of the VSI Alliance, who made a presentation which discussed design considerations in developing and integrating Analog/Mixed Signal in System-on-a-Chip. The session was

well balanced in having a second presenter from an IP provider discuss System-on-Chip debug and test, and a presenter from a semiconductor company who discussed the handling of multiple clocks in scan designs.

An interesting presentation in the ATE issues session covered the effect of jitter on test, and emphasized the point that jitter becomes a larger portion of the test cycle as test speeds increase. Different types of bounded and unbounded jitter were discussed. A presentation about Mixed Signal test on VLSI Testers analyzed whether it is easier to add analog capability to a digital VLSI tester, or to add "world class" digital capabilities to an analog oriented machine. A third presenter discussed the tradeoffs faced when designing low cost testers.

The final session addressed improvements in test generation tools that are necessary to meet the high quality goal of testing beyond the single stuck-at fault model. The first presenter viewed delay fault testing, which was suggested to be essential in the future, as an equivalent to timing verification. One speaker advocated using two fault models for IDDQ test vector selection, which were pseudo stuck at and toggle models. Issues concerning generating tests for near full-scan designs with embedded memory were also presented.

A panel session titled "Test Wisdom From the Veterans" discussed various topics including predictions of future shifts in the testing paradigm, similar to the effect that scan, bist, atpg and IDDQ have had on today's test strategies. Also discussed were the effects of copper interconnect on testing.

The workshop was organized by Edward .J. McCluskey of Stanford University, and Siyad Ma of Advanced Micro Devices. In addition, Nahmsuk Oh, Subhasish Mitra, Philip Shirvani, Davia Lu, and Mike Purtell served as , registration, finance, local arrangements, entertainment and publicity, chairs respectively. The ninth BAST workshop will be held in February 2000 at the same location, Bodega Bay California.