



# BAST 2000 Workshop Program

The Inn at the Tides, Bodega Bay, California  
February 15-18, 2000

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# BAST 2000 Workshop Program

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## \*\*\* Tuesday, Feb 15 \*\*\*

6:00 PM - 7:00 PM

Registration & Reception

7:00 PM – 8:00 PM

Dinner

8:00 PM – 8:30 PM

Remarks: *Ted Hoff*

## \*\*\* Wednesday, Feb 16 \*\*\*

7:15 AM	CONTINENTAL BREAKFAST
8:15 AM - 8:20 AM	Welcome <i>Edward J. McCluskey, General Chairman</i>
8:20 AM - 8:25 AM	Introduction <i>Hong Hao, Program Chairman</i>
8:30 AM - 9:30 AM	<b>Session 1 Testers - Do They Always Tell the Truth?</b> Session Chair: <i>Mike Purtell, Advantest</i>  1.1 Timing and Clock Accuracy and its Impact on Structural Testing, <i>Burnell West, Schlumberger</i> 1.2 Challenges in Testing Source Synchronous Designs, <i>Kevin Giebel,</i> <i>Teradyne</i> 1.3 ATE Reality versus Simulated Reality, <i>Eric Larson, Teradyne</i> 1.4 Firing Line: <i>Don Sireci, Advantest; Ajay Khoche, Agilent</i>
9:30 AM-10:30 AM	BREAK
10:30 AM-11:30 AM	<b>Session 2 Testing SOC</b> Session Chair: <i>Samy Makar, Transmeta</i>  2.1 SOC Testing - Throwing the Baby out with the Bath Water!, <i>Marc</i> <i>Levitt, Sonics</i> 2.2 SOC Platform Based Design Methodology and Test Strategies, <i>Henry Chang, Cadence</i> 2.3 IDDQ Consideration for SOC, <i>Bob Duell, Synopsys</i> 2.4 Firing Line: <i>Bill Chown, IMS</i>
12:00 PM- 1:00 PM	LUNCH
1:30 PM - 2:30 PM	<b>Session 3 Functional Verification – Can We Help?</b> Session Chair: <i>Manuel d'Abreu, Level One</i>  3.1 Platforms and the Unified Test Bench, <i>Chris Lennard, Cadence</i> 3.2 Use of Test Techniques and Tools for Verification, <i>Jacob Abraham,</i> <i>Stanford CRC</i> 3.3 Scalable Framework for Generating Functional Models at RTL, <i>Minesh Amin, Synopsys</i> 3.4 Firing Line: <i>Nahmsuk Oh, Stanford CRC; Subhasish Mitra,</i> <i>Stanford CRC</i>
2:30 PM - 3:30 PM	BREAK

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3:30 PM - 4:30 PM

## **Session 4 Myths versus Data**

Session Chair: *Joel Ferguson, UC Santa Cruz*

- 4.1 Murphy-Experimental Data, *Edward J. McCluskey, Stanford CRC*
- 4.2 Cold Delay Defect Screening, *Chaowen Tseng, Stanford CRC*
- 4.3 Explaining VLV-only Failures with Tunneling Opens, *James Li, Stanford CRC*
- 4.4 Firing Line: *Peter Hashem, Teradyne; Fred Watt, Finley Design*

6:15 PM

DINNER

7:30 PM

FUN & GAMES

**\*\*\* Thursday, Feb 17 \*\*\***

7:30 AM

CONTINENTAL BREAKFAST

8:30 AM - 9:30 AM

**Session 5 VLSI Test – What’s Ahead?**

Session Chair: *Robert Huston, Credence*

- 5.1 Will Current ATE Architecture Survive in Next Millennium, *Hira Ranga, Third Millennium Test Solutions*
- 5.2 Next Generation HVM Microprocessor Test Challenges, *David Wu, Intel*
- 5.3 Stop Designing Languages, *Gordon Robinson, Credence*
- 5.4 Firing Line: *Bruce Parnas, Advantest; Garry Gillette, Credence*

9:30 AM - 10:30 AM

BREAK

10:30 AM - 11:30 AM

**Session 6 Design and Test Methodologies**

Session Chair: *L.T. Wang, Syntest*

- 6.1 Verifier - A "Closed-loop" Method for Generating and Verifying ATE Test Programs in Simulation Environment, *Peter Dahlgren, Simutest*
- 6.2 System Level Fault Grading, *Scott Davidson, Sun*
- 6.3 BIST Test Program Generation, *Mike Kondrat, Fluence*
- 6.4 Firing Line: *Bob Devor, Transmeta; Shalini Ghosh, UC Santa Cruz*

12:00 PM - 1:00 PM

LUNCH

AFTERNOON: FREE

7:30 PM - 9:30 PM

**PANEL DISCUSSION**

*at Arena Cove*

**Testing High Speed Designs - Can We Ever Do It or Is It an Oxymoron?**

Moderator:

*Edward J. McCluskey, Stanford CRC*

Panelist:

*Bill Bottoms, Third Millennium Test Solutions*

*Robert Huston, Credence*

*John Waicukauski, Synopsys*

*Burnell West, Schlumberger*

*David Wu, Intel*

\*\*\* Friday, Feb 18 \*\*\*

7:30 AM

CONTINENTAL BREAKFAST

8:30 AM - 9:30 AM

## **Session 7 Application Specific Testing**

Session Chair: *Davia Lu, IBM*

- 7.1 Synthesized ATE, *Marc Loranger, Credence*
- 7.2 Verifying DSP Software for Testing ADC, *Mike Purtell, Advantest*
- 7.3 How to Reduce the Test Development Time for Mixed-Signal Devices, *Daniel D'souza, Datapath Systems*
- 7.4 Firing Line: *Catherine Yu, Stanford CRC*

9:30 AM - 10:30 AM

BREAK

## **CHECKOUT (before noon)**

10:30 AM - 11:30 AM

## **Session 8 Testing Full Custom ICs**

Session Chair: *Bulent Dervisoglu, Intellitech*

- 8.1 Fault Coverage Analysis in FPGA: Challenges and Opportunities, *Zhi-Min Ling, Xilinx*
- 8.2 Microprocessor Test, *Sridhar Narayanan, Sun*
- 8.3 □ PRAT for Memory Testing, *Mike Lin, Intel*
- 8.4 □ Firing Line: *Patrick Fasang, Hitachi USA; Khader Abdel-Hafez, Cirrus Logic*

11:30 AM - 12:00 Noon

Closing Remarks  
Questionnaire Collection & Souvenir Distribution

12:30 PM - 1:30 PM

LUNCH  
*at Poolside (weather permitting)*