



BAST 2001 Workshop Program

The Inn at the Tides, Bodega Bay, California
February 6-9, 2001

CONFERENCE COMMITTEE

General Chair: E. J. McCluskey
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Advantest	Credence	Intel	Teradyne
Agilent Technologies	Finley Design Services	LogicVision	Third Millennium
Cirrus Logic	Fluence	Sun	Transmeta
Compaq	IBM	Syntest	Xilinx

aaa Tuesday, Feb 6 aaa

6:30 PM - 7:30 PM

Registration & Reception

7:30 PM

Dinner

aaa Wednesday, Feb 7 aaa

7:15 AM

CONTINENTAL BREAKFAST

8:15 AM - 8:20 AM

Welcome E. J. McCluskey, General Chairman

8:20 AM - 8:25 AM

Introduction Scott Davidson, Program Chairman

8:30 AM - 9:30 AM

Session 1 El Cheapo Testers

Session Chair: *Ed McCluskey, Stanford CRC*

- 1.1 The Cost of Low Cost Testers, *Burnell West, Schlumberger*
- 1.2 Low Power / Low Cost Test, *Garry Gillette, Credence*
- 1.3 Is the Cost of High Performance ATE Really the Problem? *Kevin Giebel, Teradyne*
- 1.4 Firing Line: *Hira Ranga, Third Millennium; Kevin Slaboda, LSI Logic*

9:30 AM-10:30 AM

BREAK

10:30 AM-11:30 AM

Session 2 Core Test

Session Chair: *Scott Davidson, Sun Microsystems*

- 2.1 VSIA Test Architecture, *Samy Makar, Transmeta*
- 2.2 State of art in SOC testing, *Frank Bouwman, Philips*
- 2.3 Testing SOCs, especially those with Analog modules, *Jacob Abraham, Stanford CRC*
- 2.4 Firing Line: *Tony Taylor, Synopsys; Bulent Dervisoglu, Cadence*

12:00 PM - 1:00 PM

LUNCH *at Poolside (weather permitting)*

1:30 PM - 2:30 PM

Session 3 Optimizing Test

Session Chair: *Siyad Ma, Zettacom*

- 3.1 Test Resource Partitioning, *Ajay Khoche, Agilent*
- 3.2 Testing and Yield Modeling and Critical Area Optimization, *Alvin Jee, HPL*
- 3.3 A Uniform Way of Studying Test Economics, *R. Chandramouli, Synopsys*
- 3.4 Firing Line: *Phil Burlison, Inovys; Bruce Parnas, Advantest*

2:30 PM - 3:30 PM

BREAK

3:30 PM – 4:30 PM

Session 4 Defects and Defect Models

Session Chair: *Eric Larson, Teradyne*

- 4.1 New Failure Mechanisms for Trans Gigahertz, *Bill Bottoms, Third Millennium*
- 4.2 Test Sensitivity Analysis for Open Vias in Deep Submicron, *Joey Jia, Xilinx*
- 4.3 Structured Testing of AC Coupled Nets, *Bill Eklow, Cisco*
- 4.4 Firing Line: *Ray Chen, Stanford CRC; Jon Colburn, HPL*

6:15 PM

DINNER

7:30 PM

FUN & GAMES

aaa Thursday, Feb 8 aaa

7:30 AM

CONTINENTAL BREAKFAST

8:30 AM - 9:30 AM

Session 5 FPGA and Memory Test

Session Chair: *Hong Hao, LSI Logic*

- 5.1 System on a Programmable Chip Test Methods and Challenges, *Michael Harms, Altera*
- 5.2 Embedded DRAM Yield, *Manuel D'Abreu, Ample Communications*
- 5.3 FPGA Fault Coverage and Fault Models, *Shahin Toutounchi, Xilinx*
- 5.4 Firing Line: *Arun Balakrishnan, NEC; Thai Nguyen, LSI Logic*

9:30 AM - 10:30 AM

BREAK

10:30 AM-11:30 AM

Session 6 Detecting and Diagnosing Failures

Session Chair: *Joel Ferguson, UC Santa Cruz*

- 6.1 Minvdd Testing, *Chaowen Tseng, Stanford CRC*
- 6.2 Diagnosis of Sequence Dependent Failures, *James Li, Stanford CRC*
- 6.3 DFT Tools Contribution to Failure Dagnostics, *Bob Duell, Synopsys*
- 6.4 Firing Line: *Samiha Mourad, Santa Clara University; Tom Austin, Teradyne*

12:00 PM - 1:00 PM

LUNCH

at Poolside (weather permitting)

AFTERNOON: INDIVIDUAL DISCUSSION

7:30 PM - 9:30 PM

PANEL DISCUSSION

at Arena Cove Lounge

Guaranteeing Quality Throughout the Product Life Cycle – On-line Test and Repair to the Rescue

Moderator: *E. J. McCluskey, Stanford CRC*

Panelists: *Scott Davidson, Sun*
John Waicukauski, Synopsys
Burnell West, Schlumberger

aaa Friday, Feb 9 aaa

7:30 AM

CONTINENTAL BREAKFAST

8:30 AM - 9:30 AM

Session 7 Test Methods

Session Chair: *Mike Purtell, Advantest*

7.1 Applying Test Methods in Mixed Signal Prototyping, *Davia Lu, IBM*

7.2 Characterization and Verification of Embedded PLLs, *Tom Egan, Teradyne*

7.3 Data Path Direct Access Test, *Kee Sup Kim, Intel*

7.4 Firing Line: *Fred Watt, Finley Design Services; Jon Turino, Fluence*

9:30 AM - 10:30 AM

BREAK

CHECKOUT (before noon)

10:30 AM-11:30 AM

Session 8 BIST

Session Chair: *R. Chandramouli, Synopsys*

8.1 Detecting Real Defects with BIST, *Subhasish Mitra, Stanford CRC*

8.2 Why the Ultra Sparc III does not have Logic BIST?, *Farideh Golshan, Sun*

8.3 Logic BIST, *Yaron Kretchmer, LSI Logic*

8.4 Firing Line: *Givargis Danialy, Logic Vision; Hussain Al –Assad, UC Davis*

11:30 AM - 12:00 Noon

Closing Remarks
Questionnaire Collection

12:00 PM - 1:30 PM

LUNCH
at Poolside (weather permitting)