



# BAST 2002 Workshop Program

The Inn at the Tides, Bodega Bay, California  
February 5-8, 2002

## CONFERENCE COMMITTEE

General Chair: Edward J. McCluskey  
Co-General Chair: Subhasish Mitra  
Program Chair: Scott Davidson  
Registration Chair: James Li  
Local Arrangements Chair: Mike Purtell  
Finance Chair: Sungroh Yoon  
Publicity Chair: Mike Purtell  
Entertainment Chair: Davia Lu

---

### DONORS

Advantest  
Chip Engines  
Credence  
HPL  
IBM  
IMS  
Intel  
Schlumberger  
Synopsys  
Syntest  
Teradyne  
Third Millennium  
Transmeta

### Steering Committee

E.J. McCluskey, Stanford CRC  
R. Chandramouli, Synopsys  
Siyad Ma, Zettacom  
Mike Purtell, Advantest

---

## Tuesday, Feb 5

5:30 PM Registration & Reception  
7:30 PM Dinner

## Wednesday, Feb 6

- 7:15 AM CONTINENTAL BREAKFAST
- 8:15 AM Welcome E. J. McCluskey, General Chairman
- 8:20 AM Introduction Scott Davidson, Program Chairman
- 8:30 AM **Session 1 SoC Test**  
Session Chair: *Scott Davidson, Sun Microsystems*
- 1.1 Production Test Solutions for SOC or SIP (System in Package) circuits using a partition test strategy, *Bill Bottoms, 3MTS*
  - 1.2 Test Challenges for SiP (system in package), *Bill Price, Phillips*
  - 1.3 Test Economics for Multi-site Test with Modern Cost Reduction Techniques, *Erik Volerink, Agilent*
  - 1.4 Firing Line: *John Waicukauski, Synopsys; Samy Makar, Transmeta*
- 9:30 AM- BREAK
- 10:30 AM **Session 2 Production Test**  
Session Chair: *Mike Purtell, Advantest*
- 2.1 Test Pattern Data Hierarchy in a Structured Test Environment, *Phil Burlison, Inovys*
  - 2.2 Combing Die Information to Improve Pass/Fail Decisions, *Stuart Nelson, Teradyne*
  - 2.3 DFT and Production Testing, *Hira Ranga, 3MTS*
  - 2.4 Firing Line: *Mike Kondrat, IMS; Tony Taylor, Synopsys*
- 12:00 PM- LUNCH
- 1:30 PM **Session 3 Debug**  
Session Chair: *Subhasish Mitra, Intel*
- 3.1 Empirical Analysis of a Model-based Functional Debug Strategy, *Bill Eklow, Cisco*
  - 3.2 Challenges and Advances in Debug and Diagnostics, *Srikanth Venkataraman, Intel*
  - 3.3 Diagnosis of Sequence Dependent Chips, *James Li, Stanford CRC*
  - 3.4 Firing Line: *Phil Burlison, Inovys; Sammy Lee, Syntest*
- 2:30 PM BREAK
- 3:30 PM **Session 4 Beyond Digital Test**  
Session Chair: *Bill Bottoms, 3MTS*
- 4.1 Mixed Signal High Speed Product Testability, *Salem Abdennadher, Intel*
  - 4.2 CDMA BB to IF Modulation, *Mike Purtell, Advantest*
  - 4.3 Limitation of Conventional Solutions in Digital ATE, *Bob Huston, 3MTS*
  - 4.4 Firing Line: *Paul Patton, Advantest; Marc Loranger, Credence*
- 6:15 PM DINNER FUN & GAMES

## Thursday, Feb 7

7:30 AM CONTINENTAL BREAKFAST

8:30 AM **Session 5 Test Quality**  
Session Chair: *Samy Makar, Transmeta*

- 5.1 ATPG for Defect oriented Test, *Jon Colburn, HPL*
- 5.2 TARO ATPG, *Sungroh Yoon, Stanford CRC*
- 5.3 Stuck-At and Transition N-Detect fault coverage of Pseudo Random and Deterministic Patterns, *Dwayne Burek, LogicVision*
- 5.4 Firing Line: *Tony Taylor, Synopsys; Marc Loranger, Credence*

9:30 AM BREAK

10:30 AM **Session 6 Test Past, Present and Future**  
Session Chair: *Kee Sup Kim, Intel*

- 6.1 Review/Revision of a BIST prediction, *Jim Stewart, QS Tech*
- 6.2 Time for Changing the Test Paradigm, *Rudy Garcia, Schlumberger*
- 6.3 A 10-Billion Transistor IC architecture, implementation and test, *Burnell West, Schlumberger*
- 6.4 Firing Line: *Davia Lu, IBM; Hussain Al-Assad, UC Davis*

12:00 PM LUNCH at Poolside (weather permitting)

AFTERNOON: INDIVIDUAL DISCUSSION

7:30 PM **PANEL DISCUSSION**

*at Arena Cove Lounge*

**How do we find Failures in the Chips of Tomorrow?**

Moderator: *E. J. McCluskey, Stanford CRC*

Panelists: *Manuel d'Abreu, Ample Communications*  
*Scott Davidson, Sun*  
*Srikanth Venkataraman, Intel*  
*Bill Bottoms, 3MTS*

## Friday, Feb 8

7:30 AM CONTINENTAL BREAKFAST

8:30 AM **Session 7 Functional Test**

Session Chair: *Burnell West*

7.1 Functional Test for \$1 / pin, *Garry Gillette, Credence*

7.2 Problems in Getting and Grading Functional Vectors, *Nirmal Saxena, Stanford CRC/Chip Engines*

7.3 The Need for Functional Test, *Kee Sup Kim, Intel*

7.4 Firing Line: *Scott Davidson, Sun; Rudy Garcia, Schlumberger*

9:30 AM BREAK

### **CHECKOUT (before noon)**

10:30 AM **Session 8 Test Compaction**

Session Chair: Ed McCluskey, Stanford CRC

8.1 Test Compression, *Janusz Rajski, Mentor*

8.2 Compaction Issues, *John Waicukauski, Synopsys*

8.3 X Compact, *Subhasish Mitra, Intel*

8.4 Firing Line: *Alvin Jee, HPL ; Prabhu Krisnamurthy, LSI Logic*

11:30 AM Closing Remarks. Questionnaire Collection

12:30 PM LUNCH at Poolside (weather permitting)