



# BAST 2003 Workshop Program

The Flamingo Resort Santa Rosa, California  
February 25-28, 2003

## CONFERENCE COMMITTEE

General Chair: Edward J. McCluskey  
Co-General Chair: Subhasish Mitra  
Program Chair: Samy Makar  
Registration Chair: Ahmad Alyamani  
Local Arrangements Chair: Nahmsuk Oh  
Finance Chair: Erik Volkerink  
Publicity Chair: Mike Purtell  
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Edward J. McCluskey, Stanford  
Subhasish Mitra, Intel  
R. Chandramouli, Synopsys  
Siyad Ma, Zettacom  
Mike Purtell, Advantest

5:30 PM Registration & Reception

7:00 PM Dinner & After dinner remarks by Dr. Leonard Kleinrock.

## Wednesday, Feb 26

- 7:00 AM CONTINENTAL BREAKFAST
- 8:15 AM Welcome E. J. McCluskey, General Chairman
- 8:20 AM Introduction Samy Makar, Program Chairman
- 8:30 AM **Session 1 2010 Testers**  
Session Chair: E J McCluskey CRC
- 1.1 Future of Test, *Bill Bottoms, 3MTS*
  - 1.2 Let's start talking about the cost of quality, *Burnie, West NPTest*
  - 1.3 Open Architecture, *Eric Kushnick Advantest*
  - 1.4 Firing Line: *Garry Gillette, Credence, Ken Posse, Teseda*
- 9:30 AM- BREAK
- 10:30 AM **Session 2 How will production test change?**  
Session Chair: *Mike Purtell, Advantest*
- 2.1 IC & Wafer Circuit Probing: Current status vs new Demands, *Marty Leibowitz, NPTest*
  - 2.2 How much retention testing should we retain ?, *Rob Aitken, Artisan Components*
  - 2.3 Production test issues for high volume manufacturing at .13 micron, *John Colburn, NVidia*
  - 2.4 Firing Line: *Ahmad ALYamani ,CRC, Kirit Khichadia, Simutest*
- 12:00 PM- LUNCH
- 1:30 PM **Session 3 High Speed IO**  
Session Chair: *Samy Makar, Transmeta*
- 3.1 Test challenges of emerging high speed IO's, *Rudy Garcia, NPTest*
  - 3.2 The future of high speed I/O test, *Klaus-Dieter Hilliges Agilent*
  - 3.3 Outstanding issues in design verification and testing for > 1Gb/s Communication Systems, *Mike Li, Wavecrest*
  - 3.4 Firing Line: *David Wu, Intel, Jacob Abraham, UT Austin*
- 2:30 PM BREAK
- 3:30 PM **Session 4 FPGA**  
Session Chair: *Davia Lu*
- 4.1 Application dependent testing of FPGAs , *Mehdi Tahoori, Stanford CRC*
  - 4.2 Fault coverage issues in PLDs, *Jayabrata Dastidar, Altera*
  - 4.3 Path phase difference delay fault testing of Routing Resources in FPGAs with diagnosis, *Erik Chmelar, Stanford CRC*
  - 4.4 Firing Line: *Hira Ranga, 3MTS, William DeWilkins, Agilent*
- 6:00 PM DINNER FUN & GAMES

## Thursday, Feb 27

7:00 AM CONTINENTAL BREAKFAST

8:30 AM **Session 5 SOC**  
Session Chair: *Jacob Abraham, UT, Austin*

5.1 Hierarchical, model-based Methodology for SOC Test, *Jim Sproch, Synopsys*

5.2 SOC Testing, *Frank Bouwman, Philips*

5.3 Test Vector Compression using feedback scan chain architecture, *Nahmsuk Oh, Synopsys*

5.4 Firing Line: *Davia Lu, Robert Thompson, Mentor Graphics*

9:30 AM BREAK

10:30 AM **Session 6 BIST++**  
Session Chair: *Wu-Tung Cheng, Mentor Graphics*

6.1 BIST reseeding with very few seeds, *Ahmad Al-Yamani CRC*

6.2 Low Power LogicBIST, *Dwayne Burek, Logic Vision*

6.3 The impact of Compression on Defect Coverage, *Erik Volkerink, Agilent*

6.4 Firing Line: *John Waicukauski, Synopsys, Robert Thompson, Mentor Graphics*

12:00 PM LUNCH

AFTERNOON: INDIVIDUAL DISCUSSION

7:30 PM **PANEL DISCUSSION**  
**Test compaction**

Moderator: *E. J. McCluskey, Stanford CRC*

Panelists: *Robert Thompson, Mentor Graphics*

*Subhasish Mitra, Intel*

*John Waicukauski, Synopsys*

*Dwayne Burek, Logicvision*

## Friday, Feb 28

7:00 AM CONTINENTAL BREAKFAST

8:30 AM **Session 7 Reliability/Yield/DPM**  
Session Chair: *Subhasish Mitra, Intel*

- 7.1 DPM modeling and test quality, *Srikanth Venkataraman, Intel*
- 7.2 Yield Management in SOC designs, *Marc Loranger, Credence*
- 7.3 Is CMOS more reliable with scaling?, *TM Mak, Intel*
- 7.4 Firing Line: *Robert Aitken, Artisan, Frank Bouwman Philips*

9:30 AM BREAK

### **CHECKOUT (before noon)**

10:30 AM **Session 8 Delay Test**  
Session Chair: *Kee Sup Kim, Intel*

- 8.1 Testing of speed paths in Microprocessors, *Rathish Jayabharathi, Intel*
- 8.2 AC scan Test Strategy, *Phil Burlison, Inovys*
- 8.3 Delay Testing, *David Wu, Intel*
- 8.4 Firing Line: *Bill Price, Philips, Francois Ferhani, CRC*

11:30 AM Closing Remarks. Questionnaire Collection

12:00 PM LUNCH