



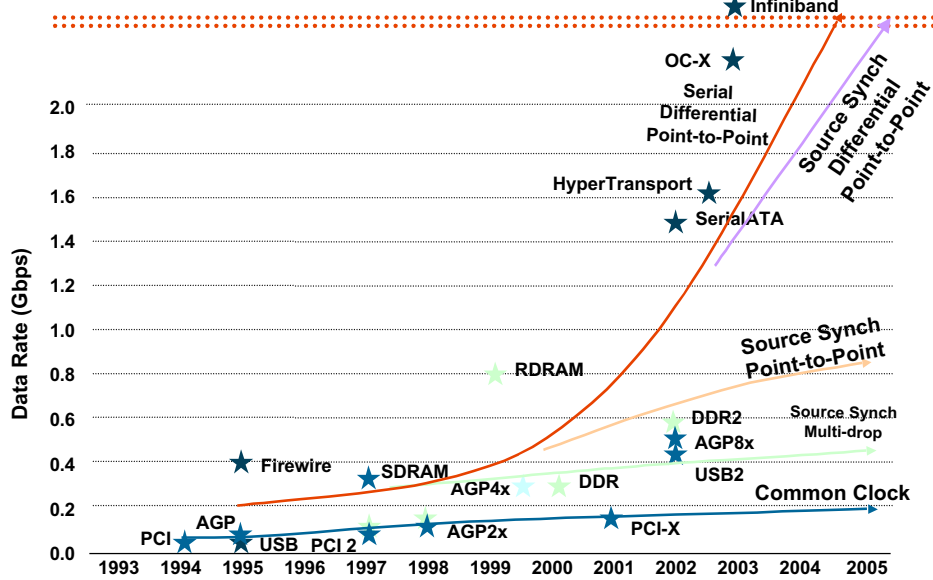
Test Challenges of High-Speed I/Os

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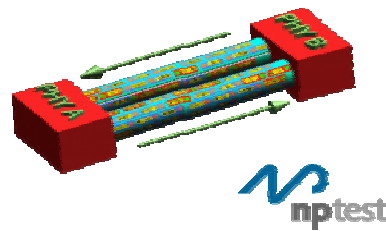


I/O Trends

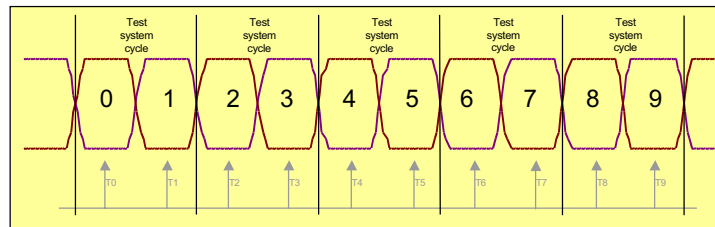


Source Synchronous Interfaces

- Typically 1 clock + 8 data per link
- Unidirectional and terminated environment
- Low voltage differential signaling
- Data rates 1.6Gbps or more
- Multiple links per device
- Examples: HyperTransport, RapidIO



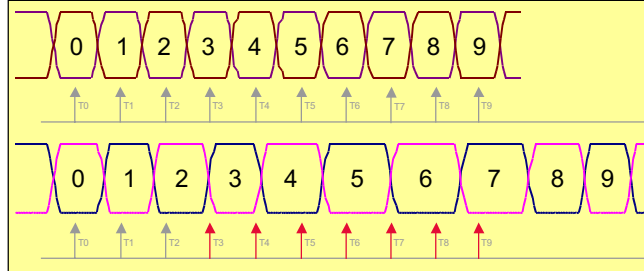
Source Sync Test Challenge



- DUT cycles segmented into “test system cycles”
- ATE drive and strobe edges timed from the beginning of each test system cycle
- Period and delay of test system edges may change cycle to cycle but all are based on internal ATE system oscillator



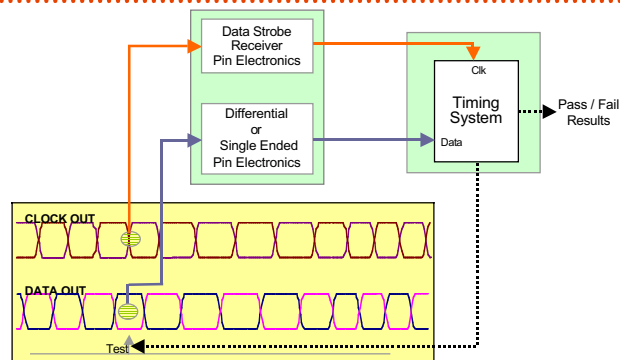
Source Sync Test Challenge



- DUT output shifts (jitters) due to:
 - Cycle-to-cycle jitter
 - Pattern dependent jitter
 - Pin-to-pin skew
 - Accumulated phase error
- Good device may fail functional tests due to output jitter



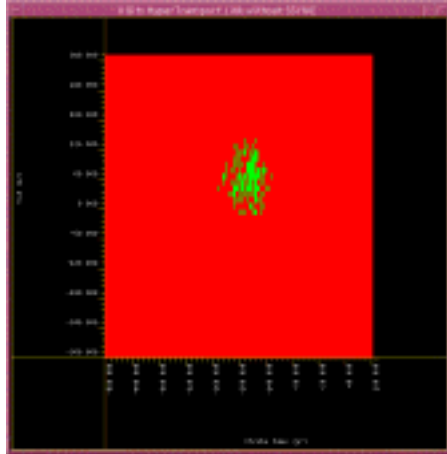
Source Sync Test Solution



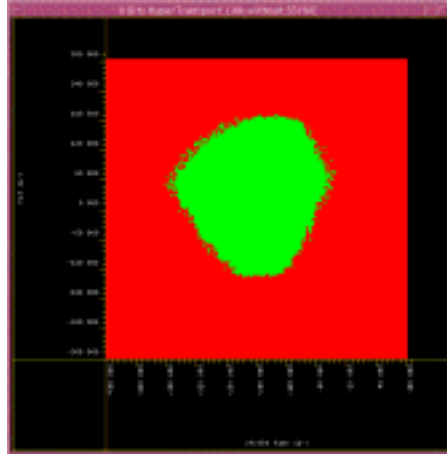
- Enhance test system with true source synchronous timing
- Up to 2 bit cell widths of cycle-to-cycle jitter
- Up to 4ns of accumulated phase shift
- Multiple and independent HyperTransport link testing



Source Sync Test Solution



HyperTransport output without source sync enabled



HyperTransport output with source sync enabled

