



BAST'03
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Built-In Reseeding

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Research Interests: BIST, Defect Based Testing

Motivation, Objective and Contribution

❖ Motivation

- BIST \Rightarrow Fault Coverage $< 100\%$

❖ Objective

- 100% Fault Coverage
 - No test point insertion or design modification
 - No performance overhead

❖ Contribution

- On-Chip Reseeding
- Seed Ordering to minimize number of seeds

Built-In Reseeding

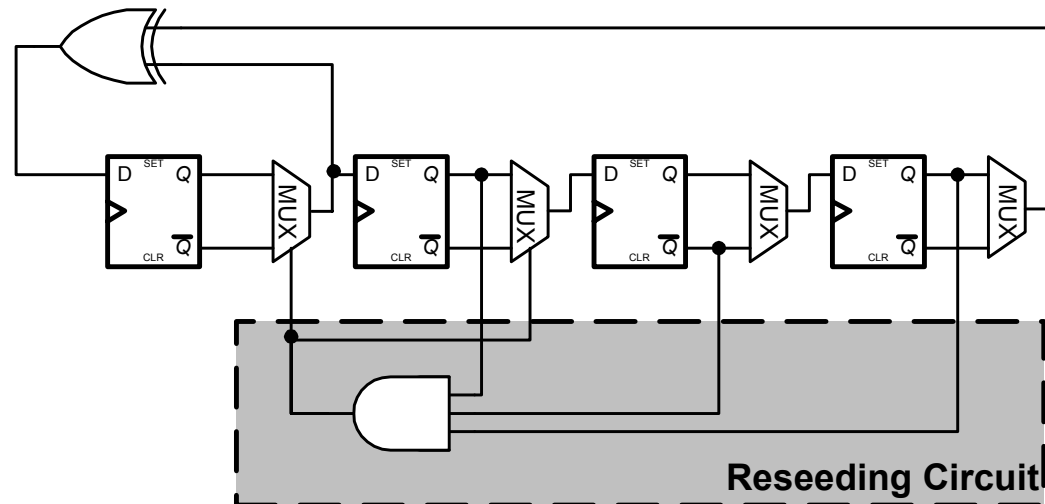
Cycle	Q1	Q2	Q3	Q4	Cycle	Q1	Q2	Q3	Q4
0	1	0	0	0	8	1	1	0	1
1	1	1	0	0	9	0	1	1	0
2	1	1	1	0	10	0	0	1	1
3	1	1	1	1	11	1	0	0	1
4	0	1	1	1	12	0	1	0	0
5	1	0	1	1	13	0	0	1	0
6	0	1	0	1	14	0	0	0	1
7	1	0	1	0	15	1	0	0	0

End of Sequence (EOS) = c6 = 0101

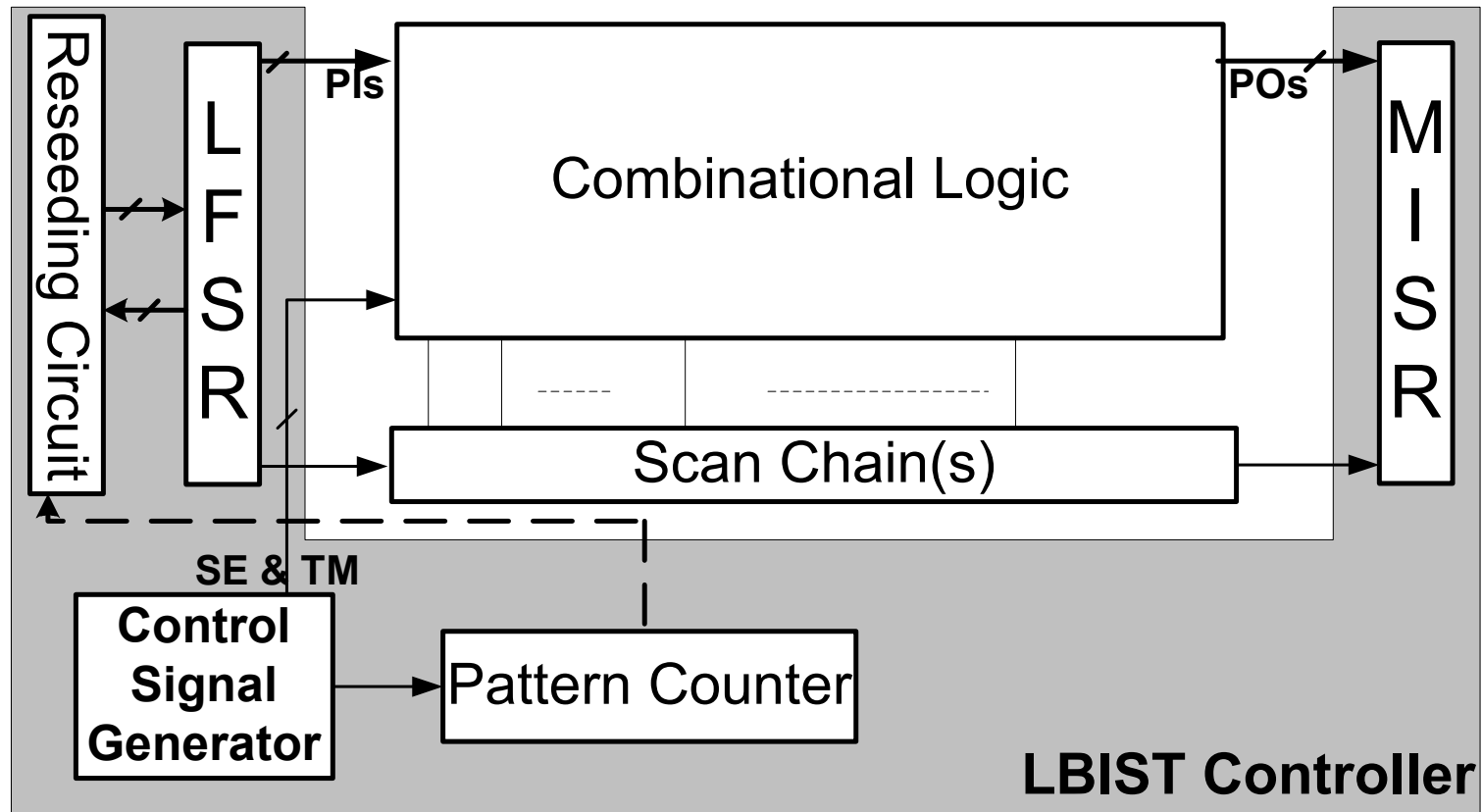
Seed = 0100 = c12

Select Lines Activated = (c6) XOR (c11)
 = 0101 XOR 1001
 = 1100

=> Select lines of Q1 and Q2 activated



System Level View



Results

- ❖ 100% fault coverage for SSF and transition
- ❖ Special HW to minimize area overhead
- ❖ Low area overhead
 - 10 benchmark circuits
 - 4% on average for SSF and transition
- ❖ In what order should seeds be applied?

Seed Ordering

- ❖ Seed = Initial state of PRPG $s(0)$
- ❖ After filling the scan chain, final state $s(m+1)$
- ❖ If $s(m+1)$ matches another seed
 - No need to load the other seed
 - If not, try for few more cycles
- ❖ Use degrees of freedom in solving for the seeds
 - Increase the chance for a match
- ❖ 34% to 80% reduction in seed storage
- ❖ 7% to 85% reduction in area overhead