The Cost of IC Quality

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Near-term Trends in Cost of Test

Cost of test:
- Structural Test
- Functional Test
- Design Validation
- Design Debug

High Volume Manufacturing

Engineering Qualification

- Structural test on DFT Testers
- Distributed Test
- Open ATE Architecture
• Increasing soft error rates
  – Memory – *largely due to radiation effects*
  – Logic – *largely due to pattern-dependent crosstalk*

• On-line test
  – Redundancy overhead
  – Repair overhead
  – Data Recovery Prep impact on overall performance

• Yield loss - two things to calculate
  – Number of good IC’s not shipped (faulty testing)
  – *Number of good circuits not shipped* (faulty devices)
A Distributed Test Strategy

- **Wafer Fab**
  - Wafer Parametrics
  - Structural Scan/Delay Tests
  - Test During Burn-in
  - Package
  - BIST
  - Focused
  - SHIP
Guaranteeing IC Quality: Cost Factors

• Amortizable Costs:
  – Test Capital Cost -- $K / Useful Life
  – F. A. Capital Cost -- $K / Useful Life
  – Facility Cost -- $K / Useful Life
  – Tooling Costs -- $K / devices shipped per type

• Unit Costs:
  – On-chip Q A Circuits -- % of device area required
  – Test time -- seconds per device (all test stages)
  – Staffing cost -- $ / hour / devices shipped hourly
  – Availability -- % of a 24 hour day
  – Yield -- % of devices not rejected during test
  – Maintenance -- $ / hour / devices shipped hourly
  – Lot Size Effects -- lot switch time / available time
  – CONQ -- $ / device returned / devices shipped
Calculating the Cost of Quality

\[ C_Q = \left( \sum n_T c_T + \sum n_S c_S + C_{ONQ} + \sum n_F c_F \right) \times \frac{R}{N} \]

- \( n_T \): the number of devices tested at step T
- \( n_S \): the number evaluated during the QA screen process
- \( n_F \): the faulty devices analyzed
- \( C_{ONQ} \): the Cost of Non-Quality –
  - the cost of making good to the customers
  - all the damages incurred due to shipment of faulty product
- \( R \): the silicon ratio – DFT/QA Silicon / Mission Silicon
- \( N \): devices shipped