Stuck-At and Transition N-Detect fault coverage of Pseudo Random and Deterministic Patterns

Dwayne Burek
BAST 2002
At-Speed Test Quality

Source: ITC '95 / Center for Reliable Computing, Stanford University
Why N-Detect is Important

Defects Requiring Multiple Detections
Logic BIST N-Detect Results

High-quality test

Percentage of faults detected n times

Number of detections

- Deterministic: compaction level 4
- Deterministic: compaction level 1
- Logic BIST

© LogicVision, Inc., 2002
Benchmark Circuit

- Embedded Logic Test (ELT) Block
- Single Clock Domain
- Gate Count (extracted): 798192
- Flop Count: 33403
- Test Points: 244 (200 OBS, 44 CNTRL)
- DTPG Pattern Count:
  - Compression Level 1: 4037
  - Compression Level 4: 3060
- DTPG Redundant Faults: 0.74%
- DTPG Aborted Faults: 0.22%
Logic BIST SA and TR Coverage
Logic BIST vs SCAN ATPG (SA)
Logic BIST vs SCAN ATPG (TR)
Logic BIST vs SCAN ATPG (SA)
Logic BIST vs SCAN ATPG (TR)
Conclusion

- At-Speed pseudo random testing provides superior quality over both low-speed and at-speed deterministic:
  - Confirmed by Stanford CRC, ITC ’95.
  - 4 escapes corresponds to DPM level of 720
- Higher levels of Stuck-At and Transition N-Detect coverage result in higher quality test.
- Logic BIST Stuck-At and Transition N-Detect coverage can be significantly higher than compacted deterministic ATPG patterns.