A Technique to Reduce the Occurrence of Overkill

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Abstract

A reduction in supply voltage due to the resistance of power-ground network is called IR-drop (also called supply voltage droop). IR-drop may slow down operation speed of a chip unnecessarily; this could result in failing the structural test even though the chip could operate correctly in its application (i.e., overkill). This paper investigates a technique to reduce IR-drop and its impact on overkill. Experiments were conducted on ELF13 test chips fabricated in 0.13μm technology. This technique effectively reduced overkill up to 20% without increasing the number of escapes.

1. Introduction

Chips that produce correct results under normal operating conditions (*good chips*) may fail structural tests applied via scan chains (also called *scan chain caused overkill*). Some of the potential causes of overkill are (1) multi-cycle paths, (2) false paths, and (3) excessive switching activities.

1. *A multi-cycle path* is a path that requires two or more clock cycles for a signal to propagate to the destination flip-flops [Saxena 02]. Scan-based transition delay test patterns can be generated without considering multi-cycle paths. In this case, the multi-cycle paths may cause overkill.
2. *A false path* is a path that cannot be sensitized during normal operation. In scan-based transition delay testing, some test patterns could sensitize and test the false paths, and good chips may fail the test.
3. The values of many flip-flops switch multiple times during scan shift of structural test patterns, hence all the nodes in the network that are connected to the flip-flop outputs need to switch their values during scan shift (also called *switching activity*). This may generate current spikes which are usually higher than the currents during functional operation [Sankaralingam 00]. The resulting current spike through the resistance of power-ground network can cause the supply voltage to drop (also called *IR-drop*) [Saxena 03] and this IR-drop could reduce the speed of a device [Mak 04]. Therefore, a structural test containing excessive switching activity may fail even though the device operates correctly in normal operation (with normal switching activity). Therefore, excessive switching activity of test patterns may cause overkill.

This paper introduces a new technique that reduces the occurrence of overkill. The proposed technique introduces certain amount of time (or *idle cycles*) between the last shift cycle and the launch cycle. During the idle cycles, a chip could recover from IR-drop, which may have caused a chip to operate at slower speed. Therefore, overkill can be reduced by applying test patterns with idle cycles.

We applied structural tests, system level test and functional test to all of ELF13 test chips. In System Level Test (SLT), a chip is inserted in an actual system and tested whether it produces correct outputs in an actual system. On the other hand, functional test patterns were generated based on the verilog simulation and applied on the tester. We first applied structural test sets under various test conditions to characterize the test chips. Then, SLT and functional test were applied to identify overkill and defective chips. In this experiment, chips that pass SLT and functional test, but fail structural tests are considered as overkill. After classifying the test chips, the proposed technique was applied to overkill and defective chips. Experiments were conducted on test chips manufactured in 0.13μm technology.

This paper is organized as follows. Section 2 presents previous work. Section 3 presents the test chips. This section also presents how test chips were collected and categorized. Section 4 presents the implementations of the proposed technique. Section 5 presents the experimental results and analysis. Section 6 presents the potential cause of overkill based on the experimental results. This paper concludes with Section 7.

2. Previous work

Low power or low switching activity test patterns can be generated by ATPG algorithms or post-processing algorithms.

The test scheduling algorithm provides a way to generate patterns that satisfy the power budget while minimizing test time [Chou 97]. [Wang 98] proposed modified PODEM algorithm that minimizes heat dissipation during test application.

Post-processing algorithms to reduce switching activity or power consumption are proposed by [Saxena 03] and [Sankaralingam 00]. [Saxena 03] generated test patterns with less switching activities than normal patterns (also called *quiet patterns*). By applying test patterns with less switching activity, chips pass at lower V_{dd}. [Sankaralingam 00] proposed the static compaction algorithm that minimizes either average power or peak power.

Power consumption also can be reduced by changing the circuit design. [Gerstendorfer 99] proposed gating scan elements to reduce power consumption.

[Volkerink 04] presented techniques to reduce power and evaluated the impact on test escapes. However, previous work on reducing power consumption or switching activity did not investigate the impact on overkill. This paper will provide a new technique that reduces the occurrence of overkill without increasing the number of test escapes.

3. Test chips

3.1 Test chip selection

Table 1 summarizes the characteristics of test chips.

Table 1 Characteristics of test chips

Feature size	0.13μm
Number of logic gates	7.2M
Number of flip-flops	NA
Number of clock domains	> 10

ELF 13 is an NVIDIA's graphics processor using 0.13μm technology. It has 7.2 million logic gates and more than 10 clock domains. The nominal supply voltage is 1.355V.

Figure 1 presents the ELF13 production test flow. NVIDIA selected 259 ELF13 chips using the production test flow. 259 ELF13 chips were retested using more thorough structural test sets under various test conditions to characterize them.

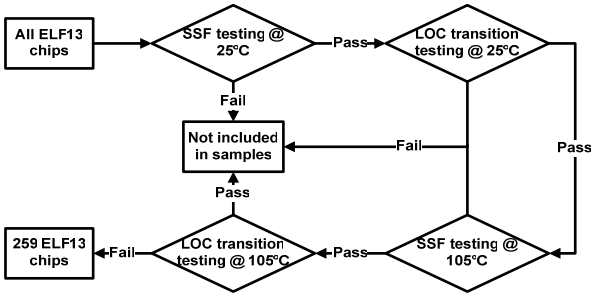


Figure 1 Production test flow

Table 2 presents the summary of the test set length and the fault coverage of the test sets.

Table 2 Structural test sets

Test set	Test set length	Fault coverage
LOC	25,909	89.8%
2-detect	11,777	94.3%

Structural test sets in Table 2 have higher fault coverage and longer test set length than the structural test sets used in the production test flow. Fault coverage of LOC transition delay test set is obtained by running the fault simulation over the transition delay faults. Similarly, fault coverage of 2-detect SSF test set is obtained by running the fault simulation over the single stuck-at faults.

In System Level Test (SLT), a chip is inserted in an actual system and tested if it operates correctly in an actual system. Functional test patterns were generated based on the verilog simulation and applied on the tester. SLT and functional test were also applied to 259 ELF13 chips. All the structural tests were applied at room (25°C) and hot (105°C) temperatures while SLT and functional test were applied only at room (25°C) temperature. Table 3 presents the test conditions for classifying the test chips.

Table 3 Test conditions

Test	Test conditions			
	Test set	Speed	Voltage	Temperature
Test 1	LOC	Nominal	1.355 V	25°C
Test 2	LOC	10MHz	1.355 V	25°C
Test 3	2-detect	<10 MHz	0.9 V	25°C
Test 4	2-detect	<10 MHz	1.355 V	25°C
Test 5	2-detect	<10 MHz	1.6 V	25°C
Test 6	LOC	Nominal	1.355 V	105°C
Test 7	LOC	10 MHz	1.355 V	105°C
Test 8	2-detect	<10 MHz	0.9 V	105°C
Test 9	2-detect	<10 MHz	1.355 V	105°C
Test 10	2-detect	<10 MHz	1.6 V	105°C

LOC test patterns were applied at nominal voltage with two different speeds: nominal speed and slow speed which is slower than 10MHz. 2-detect test patterns were applied at three different supply voltages: low V_{dd} (0.9V), nominal V_{dd} (1.355V), and high V_{dd} (1.6V). Low V_{dd} was selected under the following criteria: (1) this value should not cause good chips to fail, (2) this value should not cause chips to fail during scan data loading.

3.2 Definitions of chip categories

3.2.1 Test escape

A chip that passes all the structural tests but fails system level test or functional test is called a *structural test escape*.

3.2.2 Rated-speed failure

An LOC transition delay test set is applied at the rated speed and the slow speed. A chip that passes slow speed test but fails rated speed LOC transition delay test is called a *rated-speed failure*. Slow speed LOC transition delay test and 2-detect test with nominal and high V_{dd} are slow speed tests.

3.2.3 Slow-speed failure

A chip that fails the slow speed test is called a *slow-speed failure*.

3.2.4 Weak suspect

Weak ICs contain *flaws*, which are defects that do not necessarily cause failures under normal operating conditions but may result in early-life-failure. Weak chips due to certain flaws can be easily detected by tests that are applied at lower-than-normal power supply voltage (also called *Very-Low-Voltage test*) [Hao 93]. A chip that fails 2-detect test with low V_{dd} but passes all other structural tests is categorized as a weak suspect.

3.2.5 Overkill candidate

A chip that passes SLT and functional test, but fails structural tests is called an *overkill candidate*.

3.3 Test chip classification

Table 4 presents the test results of ELF13 classification.

Table 4 Test chip classification

Temp.	Category	SLT or functional test		Total
		Pass	Fail	
Hot (105°C) temp. only	Structural test escape (TE)	NA	0	0
	Rated-speed failure	89	20	109
	Slow-speed failure	22	7	29
	Weak suspect (WS)	15	3	18
	Overkill candidate	126	0	126
Room (25°C)te mp. only	Structural test escape (TE)	NA	26	26
	Rated-speed failure	1	0	1
	Slow-speed failure	10	2	12
	Weak suspect (WS)	19	2	22
	Overkill candidate	30	0	30
Hot (105°C) and room (25°C) temp.	Structural test escape (TE)	NA	9	9
	Rated-speed failure	20	21	41
	Slow-speed failure	7	7	14
	Weak suspect (WS)	12	5	17
	Overkill candidate	39	0	39

4. Switching activity of test patterns

4.1 Transition delay test set

The *transition fault* models a delay of a transition at the inputs and outputs of logic gates [Waicukauski 88]. Figure 2 presents the timing diagram of two different transition delay test sets.

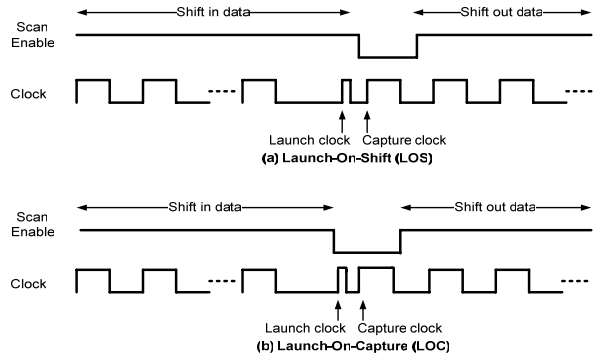


Figure 2 Timing diagrams of transition delay test set

In order to detect transition faults, a transition on a node needs to be initialized and propagated to an observable output. Therefore, two vectors (V_1, $V2$) are required, in which V_1 initializes the value of the node, V_2 makes a transition on the node and sensitizes a path that propagates the transition to an observable output. Most commercial ATPG tools support two kinds of transition delay test sets: *Launch-On-Shift (LOS)* and *Launch-On-Capture (LOC)* [Saxena 02]. In LOS test patterns, scan data is loaded through scan chains. Nodes in a CUT are initialized at the last shift clock, or launch clock. In order to make transitions and capture the response of a CUT, scan enable signal must go from 1 to 0 before the subsequent capture clock. Because scan enable signal changes between launch and capture clock, which is applied at system speed, scan enable signal should be designed to operate at system speed. Due to this design restriction, LOC test patterns are more frequently used.

In LOC test patterns, scan enable signal does not need to operate at system speed. Once scan data is loaded through scan chains, scan enable signal transitions to 0. Subsequently, launch and capture clocks are applied. Launch vector should be calculated from the response of a CUT at the capture clock because launch and capture clocks are applied while scan enable is low. Due to this restriction, LOC test set suffers from large test set size and low fault coverage compared to LOS test set. In addition, it requires more ATPG computation and restrictions than LOS test set whose launch vector is simply shifted in.

4.2 Test set with idle cycles

An *idle cycle test set* is the test set with idle cycles inserted between the last shift and launch clock per pattern.

A *Launch-On-Capture Idle Cycle (LOC-IC) test set* is the LOC test set with idle cycles inserted between the last shift and launch clock per pattern. A *base LOC test set* is the LOC test set before idle cycles are inserted. A base LOC test set is directly generated from a commercial ATPG tool. Figure 3 presents the timing diagram of LOC-IC.

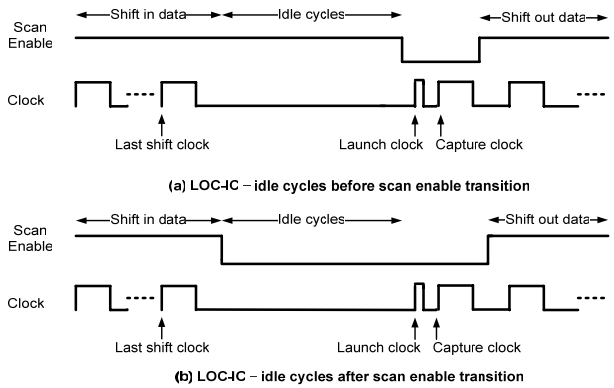


Figure 3 Timing diagram of LOC-IC transition delay test pattern

As can be seen from Figure 3, LOC-IC transition delay test set can be implemented in two ways:

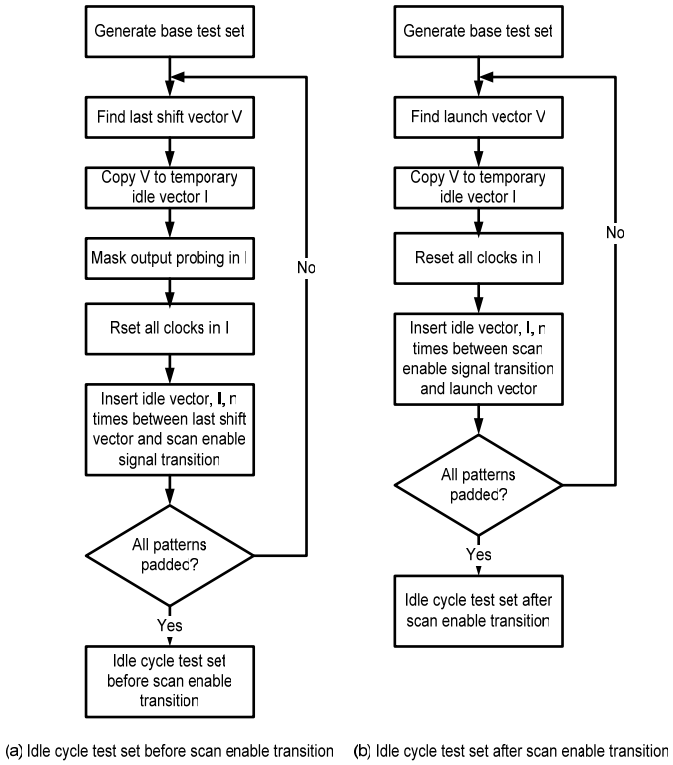
(a) Idle cycles are inserted before scan enable signal transition.

(b) Idle cycles are inserted after scan enable signal transition.

Idle cycle test sets could reduce overkill by the following manner. First, Idle cycles can provide a CUT with time to recover its original supply voltage which could have been degraded by IR-drop. Second, temperature increase during scanning in data can be alleviated. As a result, exacerbated delay due to IR-drop or temperature increase can be reduced.

An *SSF-IC test set* is the idle cycle test set using SSF test set as the base test set and can be implemented in a similar way explained above.

Figure 4 presents the flowchart that implements idle cycle test sets.



(a) Idle cycle test set before scan enable transition (b) Idle cycle test set after scan enable transition

Figure 4 Flowchart of idle cycle test set generation

Key properties of the idle cycle test set are listed below.

1. The expected values of test patterns do not change. Therefore, no additional ATPG time is required.
2. No clocks pulse during idle cycles. Otherwise, expected values will change.
3. No outputs are compared during idle cycles.
4. Primary input values are not changed during idle cycles.
5. The idle cycle test set has the same fault coverage as the base test set.
6. The idle cycle test set initializes and propagates faults to the observable outputs the same as the base test set does.

4.3 Test setup

Test sets given in Table 2 are used as the base test sets to generate LOC-IC and 2-detect SSF-IC test sets as discussed in the previous section. The number of idle cycles varies from 100 to 1000. Idle cycles are inserted both before and after the scan enable signal transition.

All idle cycle test sets are summarized in Table 5.

Table 5 Summary of test sets with idle cycles

Test set	Idle cycle position	# of idle cycles	Fault coverage	Test set length
LOC	After	100	89.8%	25,909
		200	89.8%	25,909
		300	89.8%	25,909
		500	89.8%	25,909
		1000	89.8%	25,909
	Before	1000	89.8%	25,909
SSF	After	100	94.3%	11,777
		200	94.3%	11,777
		300	94.3%	11,777
		500	94.3%	11,777
		1000	94.3%	11,777
	Before	1000	94.3%	11,777

Second column in Table 5 presents the position of inserted idle cycles with respect to the scan enable signal transition. Note that fault coverage and test set length of LOC-IC/SSF-IC test sets are the same as those of the base LOC/SSF test set. However, the total number of test vectors per pattern is increased by the number of inserted idle cycles. Idle cycle test sets given in Table 5 were applied to chips that fail the original test sets to find out the effect of idle cycles on test results. Idle cycle test sets are applied as follows.

1. All LOC-IC test sets were applied to 109 chips, which are categorized as rated-speed failures at hot temperature only (see Table 4). Among them, 89 chips are overkill candidates and 20 chips are defective chips.
2. Among 29 chips that are categorized as slow-speed failures at hot temperature only (see Table 4), 19 chips fail 2-detect test set at nominal supply voltage. All SSF-IC test sets were applied to those 19 chips. Among them, 15 chips are overkill candidates and 4 chips are defective chips.

5. Experimental results

5.1 Idle cycle test sets

Table 6 presents the experimental results on idle cycle test sets.

Table 6 Experimental results on LOC-IC/SSF-IC

Test set	Idle cycle position	# of idle cycles	Overkill candidate		Defective chips	
			Pass	Fail	Pass	Fail
LOC	After	100	4	85	0	20
		200	4	85	0	20
		300	6	83	0	20
		500	15	74	0	20
		1000	18	71	0	20
	Before	1000	0	89	0	20
SSF	After	100	1	14	0	4
		200	1	14	0	4
		300	1	14	0	4
		500	1	13	0	4
		1000	2	13	0	4
	Before	1000	NA*	NA*	NA*	NA*

(*Final version will include the results.)

As can be seen from Table 6, the more idle cycles are inserted, the more overkill candidates pass idle cycle test sets. However, no test escapes observed from idle cycle test sets. No chips pass LOC-IC test set if idle cycles are inserted before scan enable transition.

5.2 ATPG overhead and test time

Implementation of idle cycle test sets takes advantage of commercial ATPG tools. No new ATPG algorithm is required and any compaction algorithm in commercial ATPG tools can be utilized. We can generate a base test set as compact as possible using commercial ATPG tools. After that, idle cycles can be easily inserted using a script. There is no ATPG overhead involved with implementing idle cycle test sets. However, test application time increases since idle cycles increase the number of tester cycles per test pattern. Table 7 presents test application time of various idle cycle test sets.

Table 7 Summary of test application time

Test set	Idle cycle position	# of idle cycles	Test time	Additional test time
LOC	NA	0	11.304s	0s
	After	100	11.674s	0.3701s
		200	12.044s	0.7403s
		300	12.414s	1.110s
		500	13.154s	1.851s
		1000	15.005s	3.701s
	Before	1000	15.005s	3.701s
SSF	NA	0	5.138s	0s
	After	100	5.306s	0.1682s
		200	5.475s	0.3365s
		300	5.643s	0.5047s
		500	5.979s	0.8412s
		1000	6.821s	1.6824s
	Before	1000	6.821s	1.6824s

In Table 7, test sets with zero number of idle cycles refer to the base test sets.

5.3 Delay size and minimum operating voltage

The base LOC test set was used to obtain shmoo plots. From shmoo plots, maximum operating frequencies at nominal supply voltage were collected.

Excess delay is the additional delay that causes a chip to fail a transition delay test. Excess delay can be calculated using the following equation.

$$\textit{Excess delay} = \frac{1}{\textit{maximum operating frequency}} - \frac{1}{\textit{system frequency}}$$

The first term represents the maximum operating speed of a chip in time. The second term represents the system speed in time at which a good chip should operate. Therefore, excess delay of a chip can be expressed as the difference of the two terms.

A chip that fails the base LOC test set and passes one or more LOC-IC test sets whose idle cycles are inserted after scan enable signal transition is called an *LOC-IC passing chip*. A chip that fails the base LOC test set and all LOC-IC test sets whose idle cycles are inserted after scan enable signal transition is called an *LOC-IC failing chip*. Therefore, there are four categories of test chips:

1. LOC-IC passing chips which are overkill candidates
2. LOC-IC failing chips which are overkill candidates
3. LOC-IC passing chips which are defective chips
4. LOC-IC failing chips which are defective chips

Excess delays of the above categories are presented in Figure 5. Note that ELF13 chips in category 3 do not exist. Histogram is presented as the percentage of the occurrence out of total population of each category.

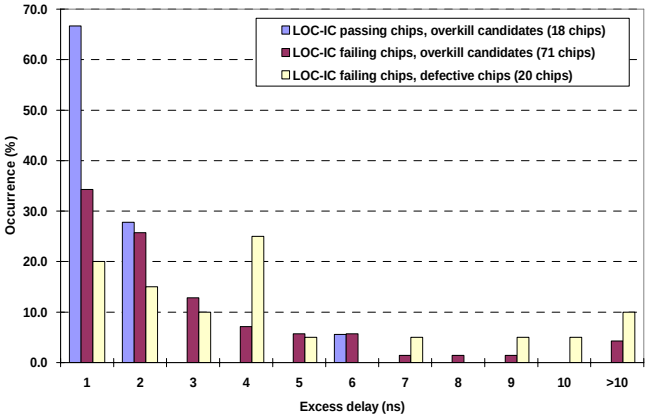


Figure 5 Histogram of excess delay

All the overkill candidates that pass any LOC-IC test sets have less than 2ns of excess delay except one chip. Due to the smaller delay size of the chips in this category compared to the other categories, IR-drop during shifting procedure can be critical to them. If a chip has large delay defect size, it could fail the LOC-IC test set because the amount of compensated delay size can be negligible compared to the large delay size. However, chips with small delay size do not necessarily pass LOC-IC test sets because delay defects may be located where IR-drop is not severe.

Minimum supply voltage that a chip passes the test is called V_{min}. We used the base LOC test sets to find V_{min} values. Supply voltage is decreased by 0.02V from 1.555V to the nominal voltage (1.355V) and pass/fail results are logged for each chip. Figure 6 presents the histogram of V_{min} values for three categories.

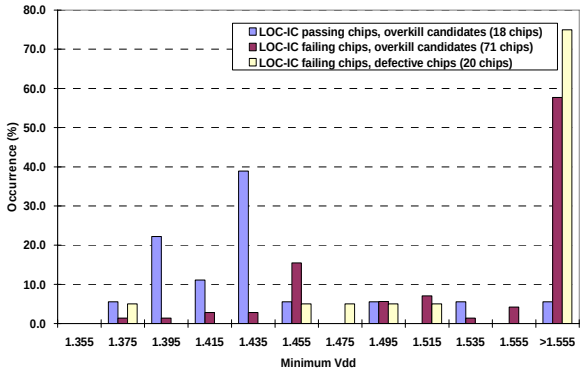


Figure 6 Histogram of minimum V_{min} values

More than 77% of LOC-IC passing chips operate at 1.435V of supply voltage. On the other hand, more than 90% of the LOC-IC failing chips (91.5% from overkill candidates and 95.5% from defective chips) should be operated above 1.455V to pass the test. The V_{min} values of LOC-IC passing chips are distributed towards nominal supply voltage, but V_{min} values LOC-IC failing chips are distributed towards higher supply voltage.

Figure 7 presents the distribution of V_{min} values and delay size of three categories.

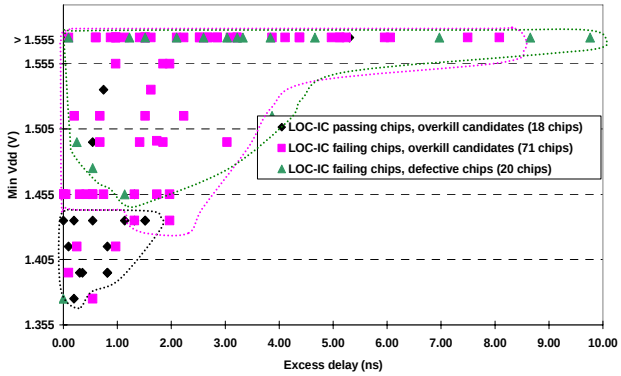


Figure 7 Excess delay vs. V_{min} values

Each data point refers to the excess delay and the V_{min} value of each chip. As can be seen from Figure 7, LOC-IC passing chips are clustered in the region of smaller excess delays and smaller V_{min} values compared to the other two categories. Clustered region of LOC-IC passing chips are separated from that of other two categories.

6. Potential cause of overkill

Idle cycles between scan enable signal transition and the launch cycle provide chips with time to settle down in two ways: (1) during idle cycles, temperature increase due to shifting procedure could vanish away such that exacerbated delays due to temperature increase can be recovered, (2) during idle cycles, IR-drop due to shifting procedure recover the original power supply voltage such that exacerbated delays due to IR-drop can be recovered.

In order to further analyze the potential cause of overkill, LOC-IC test sets were implemented in two ways: (1) idle cycles before scan enable transition and (2) idle cycles after scan enable transition. As long as the number of inserted idle cycles is the same, LOC-IC test sets implemented in the above two ways have the same amount of relaxation time. The only difference between the two test sets is the position of idle cycles. If a chip passes an idle cycle test set because idle cycles introduce time for a chip to be cooled down, the position of idle cycles should not make any difference as long as the number of inserted idle cycles is the same. However, no chips pass LOC-IC test sets when idle cycles are inserted before scan enable signal transition. Therefore, we can rule out the possibility that idle cycle test set reduces overkill caused by the temperature increase.

From Figure 7, we found that LOC-IC passing chips are clustered in the smaller excess delays and smaller V_{min} values. This implies that idle cycles inserted after scan enable transition may compensate for the IR-drop due to scan enable signal transition, hence chips with small V_{min} could pass the idle cycle test set. Note that scan enable signal is fed to all scan flip-flops at the same time. Therefore, it is possible that there exist current peaks due to scan enable signal transition such that a chip suffers from IR-drop, which may cause overkill.

7. Conclusions

This paper investigates how overkill could be reduced by inserting idle cycles between the last shift cycle and the launch cycle without increasing the number of test escapes.

The proposed technique was applied to ELF13 test chips manufactured in 0.13µm technology. With the proposed technique, 18 out of 89 overkill candidates pass the structural test, but no test escapes occur. In addition, proposed method is easy to implement and commercial ATPG tools can be directly used.

Potential cause of overkill is also presented based on the experimental results.

8. Acknowledgements

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