Defective Chip Classes and Test Metrics

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Abstract

This paper shows data related to choosing a pair of test sets for Digital IC production test. This data demonstrates that the choice of the second set of the pair should take into account the test metric used for the first test set. An approach for making this choice by taking defect coverage and total test length into account is presented.

1. Introduction

Previous work [Maxwell 93] [Nigh 97] has shown the importance of using different metrics to test integrated circuits. Production testing of digital ICs often applies two test sets. These sets are derived using two different test metrics: single-stuck fault and N-Detect, for example. This paper addresses the question of how to choose the pairs of test metrics.

Defective chips are classified according to their sensitivity to the sequence or speed of pattern application. Those chips whose response to an applied test set depends on the sequence in which the patterns are applied are called *sequence dependent chips*. If, in addition, the response depends on the speed of application, they are called *sequence and timing dependent.* The remaining chips are called *timing independent combinational chips* or *TICs* for short. Figures 1 and 2 show the classification for the two chips studied here.

These two chips comprise multiple combinational cores, each of which can be directly accessed from the chip pins. A follow-on study is planned with test chips that provide only full-scan access to the cores. We expect the data to vary from that presented here, but that the direct access results represent a limiting case.

Not too surprisingly, the effectiveness of test metrics varies according to the defective class of the chip being tested. The single-stuck fault metric is very effective in detecting TIC chips but less effective for sequence-dependent chips. The transition fault test metric is worse than the single-stuck fault metric for TIC defects, better for sequence-dependent defects.

In [McCluskey 04] the authors compare the effectiveness of different test metrics by applying different test sets and comparing the number of escapes. In this paper we compare their effectiveness for different defective chip classes by taking into account the defective behavior of the escapes in addition to comparing their number.

Previous work [Hawkins 94] [Maly 03] studied the physical characteristics of defects in order to find better metrics or better tests. Defect-based testing research studies how to test integrated circuits based on those physical characteristics [Soden 95] [Baker 99] [Segura 02] [Sengupta 99]. In this paper however, we only take into account the behavior of the defective chip instead of the physical characteristics of its defect.

The paper is organized the following way: section 2 describes the experiment: the test chips and their defective classification. Section 3 presents the data

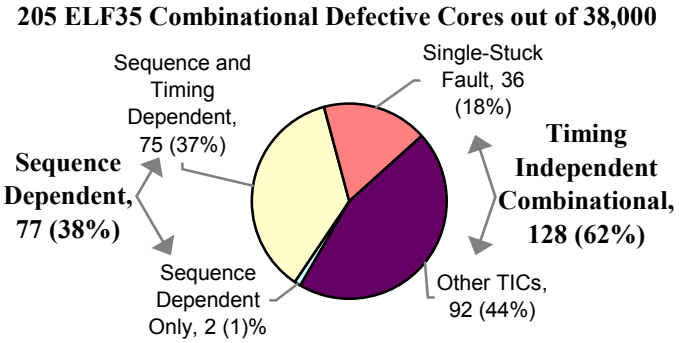


Figure 1: ELF35 Defective Chip Classification

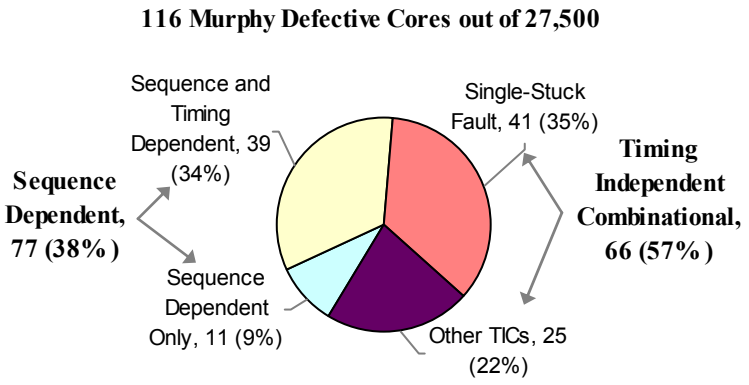


Figure 2: Murphy Defective Chip Classification

collected in the study described here.

2. Experiment

2.1. Test Chips

The Center for Reliable Computing designed the Murphy [Franco 95] and ELF35 [McCluskey 04] chips to compare the quality of different test sets. LSI Logic manufactured 5,500 Murphy chips in 0.7µm CMOS technology and 9,000 ELF35 chips in 0.35µm CMOS technology.

Murphy has 25,000 gates implementing twenty instances of five different combinational cores and ELF35 has 265,000 gates implementing forty-four instances of two sequential and four combinational cores. The sequential cores are full-scan. Their supply voltages are 5V for Murphy and 3.5V for ELF35.

We tested all cores in every chip as thoroughly as possible (e.g. we applied IDDQ, structural and exhaustive tests in different test conditions [Ma 95] [McCluskey 04]). The test conditions we varied were the supply voltage and the timing of the test. For Murphy, we applied each test at three different supply voltages (5V, 2.5V and 1.7V) and four different timings (fastest, 20% slower, three times slower and thirty times slower). For ELF35, we applied each test at two different supply voltages (3.5V and 1.4V) and three different test speeds (fastest, 20% slower and three times slower)

We identified 116 Murphy cores and 324 ELF35 failing at least one of the test sets applied. Those 440 cores are our defective cores.

2.2. Defective Chip Classes

When a test set is applied to a core, its *failure trace* is the list of patterns and observable points (flip-flops or outputs) that failed, if any.

The failure trace of some of our combinational cores depends on the timing and the sequence of the test patterns. We used this property to classify our defective combinational cores into three defective chip classes.

- The defective combinational cores whose failure trace is always the same whatever the sequence or the timing of the patterns of our test sets are called *Timing Independent Combinational* (TICs). Defects behaving like stuck-at or bridging faults can explain this behavior.
- The failure trace of another group of combinational cores depends on the sequence of the patterns but not their timing. Those are called *Sequence Dependent Only* and their behavior can be explained for example by a defect behaving like a stuck-open fault [Li 02].
- The failure trace of the remaining combinational cores depends on both the sequence and the timing of the patterns. Those are called *Timing and Sequence Dependent* and their behavior can be explained for example by a resistive open fault [Li 01].

We ran several single-stuck fault diagnosis tools to find which of the TICs behaved like single-stuck faults.

We changed the sequence and timing of our test sets [McCluskey 04] and recorded the number of failing patterns to classify our defective cores. Figures 1 and 2 show that in both ELF35 and Murphy roughly 60%, of our defective combinational cores are timing independent combinational (TIC) and that the remaining 40% are sequence dependent, of which a majority (97%for ELF35 and 79% for Murphy) is also timing dependent.

2.3. N-Detect and Gate Exhaustive Test Results

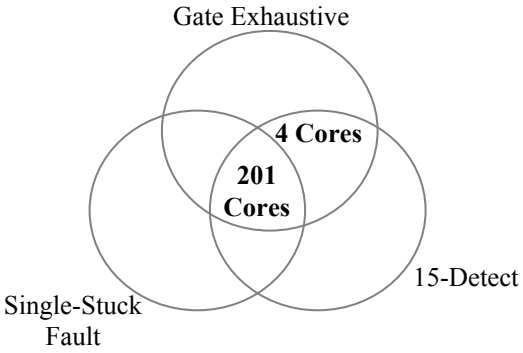
We applied N-Detect [Ma 95] [McCluskey 04] and gate exhaustive [Cho 05] test sets to the ELF35 and Murphy cores and compared their results to that of other test sets. As reported in other silicon experiments [Benware 03]

[Amyeen 04], the gate exhaustive and N-Detect test sets detected defective chips the other test sets did not.

We applied all the tests in the same conditions: room temperature, nominal voltage: 3.5V for ELF35 and 5V for Murphy, and rated speed: 20% slower than the fastest we could test good chips. To make our results independent of the test pattern generation tool, we used different tools to generate three different single-stuck test sets and three different transition test sets for ELF35.

Figures 3, 4, 5, and 6 show that for both ELF35 and Murphy, N-Detect and Gate exhaustive test sets detect cores that escape single-stuck or transition test sets.

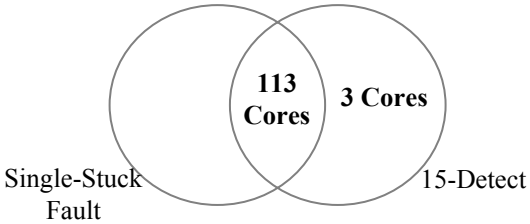
205 Defective ELF35 Combinational Cores out of 38,000



Test conditions: Room temperature, nominal voltage and rated speed

Figure 3: Comparison of ELF35 gate exhaustive, N-Detect and single-stuck fault tests results

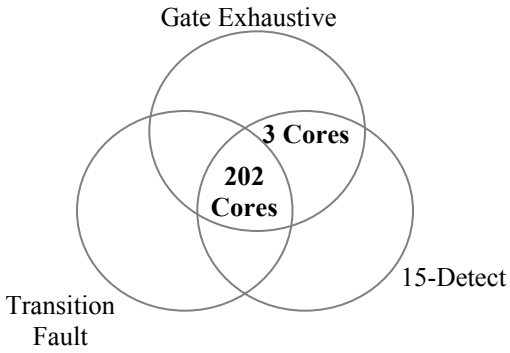
116 Murphy Defective Cores out of 27,500



Test conditions: Room temperature, nominal voltage and rated speed

Figure 4: Comparison of Murphy N-Detect and single-stuck fault tests results

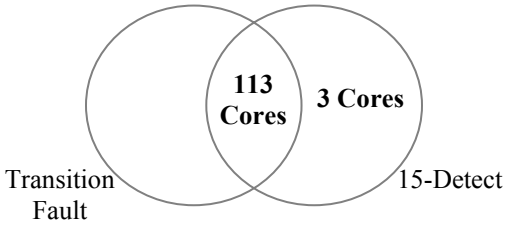
205 Defective ELF35 Combinational Cores out of 38,000



Test conditions: Room temperature, nominal voltage and rated speed

Figure 5: Comparison of ELF35 gate exhaustive, N-Detect and transition tests results

116 Murphy Defective Cores out of 27,500



Test conditions: Room temperature, nominal voltage and rated speed

Figure 6: Comparison of Murphy N-Detect and transition fault tests results

This paper will show the defective behavior of the cores only detected by N-Detect or gate exhaustive test sets.

3. Experimental Results

3.1. Defective Chip Class of Escapes

To compare the effectiveness of various test metrics on different defective chip classes, we generated test sets with them and compared the defective chip class and test results of their escapes.

This paper compares the single-stuck, transition, Gate Exhaustive [McCluskey 93] [Cho 05], N-Detect [Ma 95] and TARO [Park 05] fault coverage metrics. We applied to our ELF35 and Murphy cores one or more test sets generated with these metrics. We applied all the tests in the same conditions: room temperature, nominal voltage: 3.5V for ELF35 and 5V for Murphy, and rated speed: 20% slower than the fastest we could test good chips. Figures 9 and 10 compare the test results and defective chip class of the escapes. They show the 14 ELF35 combinational cores and the 20 Murphy cores that escape at least one of these test sets. The escapes are sorted

according to their defective chip class and for each test set the presence or absence of the thick black line shows whether it detects it or not.

Those figures show that the single-stuck fault test sets detected all our TICs. Figures 7 and 8 also show that single-stuck fault test sets with less than 100% coverage escaped some TICs.

Therefore, in our experiment, most of the cores that only gate exhaustive and N-Detect test sets detect are sequence dependent. When compared to a single-stuck fault test set, as in Figures 3 and 4, all are sequence dependent and when compared to a transition test set, as in Figures 5 and 6, two out of three cores are sequence dependent.

We tried different values of N-Detect: 15, 5 and 2. Figures 9 and 10 show that for all those values of N, all the escapes are sequence dependent.

The gate exhaustive and N-Detect test sets therefore did better than the single-stuck and transition fault test sets because they found more sequence dependent chips.

3.2. Sequence Dependent Coverage

To understand why N-Detect and gate exhaustive do so well with sequence dependent chips, we fault graded our test sets using different metrics and compared the results. Two metrics take into account the sequence of patterns: transition and TARO. Tables 1 and 2 show that N-Detect and gate exhaustive test sets have higher TARO coverage than the transition and single-stuck fault test sets. They cannot have a higher transition coverage since the transition test set already has the highest possible such coverage. TARO seems to be a better metric than the other three to detect sequence dependent chips. Table 1 also shows that the gate exhaustive test's high TARO coverage is not due to its longer length since it has higher TARO coverage than other test sets of similar length.

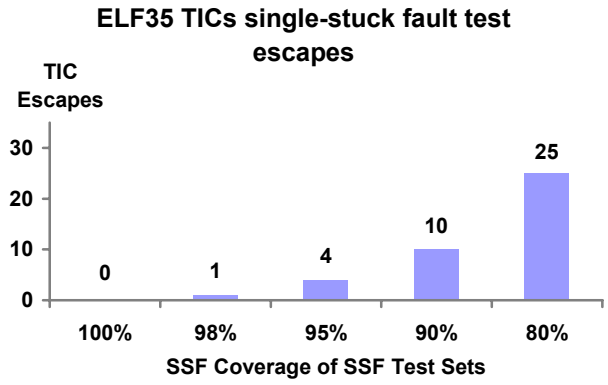


Figure 7: TIC escapes vs. single-stuck coverage for ELF35

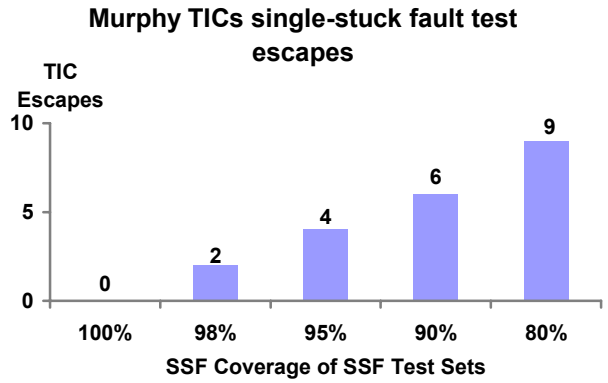


Figure 8: TIC escapes vs. single-stuck coverage for Murphy

Table 1: Fault coverage of ELF35 test sets for different metrics

Test Sets	Fault Coverages				Test Length
	TARO	Transition Fault	Single-Stuck Fault	Bridging Fault	
15-Detect	**79%**	**99%**	**99%**	**86%**	**43,035**
TARO	**90%**	**99%**	**99%**	**87%**	**29,208**
5-Detect	**77%**	**99%**	**99%**	**87%**	**14,727**
Bridging Fault	**73%**	**95%**	**98%**	**87%**	**7,105**
2-Detect	**73%**	**97%**	**99%**	**86%**	**6,099**
Transition Fault	**75%**	**99%**	**99%**	**86%**	**5,888**
Gate Exhaustive	**78%**	**95%**	**99%**	**87%**	**4,027**
Single-Stuck Fault	**67%**	**93%**	**99%**	**86%**	**3,165**
Single-Stuck Fault 98%	**64%**	**90%**	**98%**	**86%**	**2,840**
Single-Stuck Fault 95%	**59%**	**86%**	**95%**	**84%**	**2,065**

Defective chip class of ELF35 single-stuck, transition, gate exhaustive N-Detect and TARO escapes
(14 defective cores out of 205 escape at least one of these test sets)
Test Conditions: Room Temperature, Nominal Voltage and Rated Speed

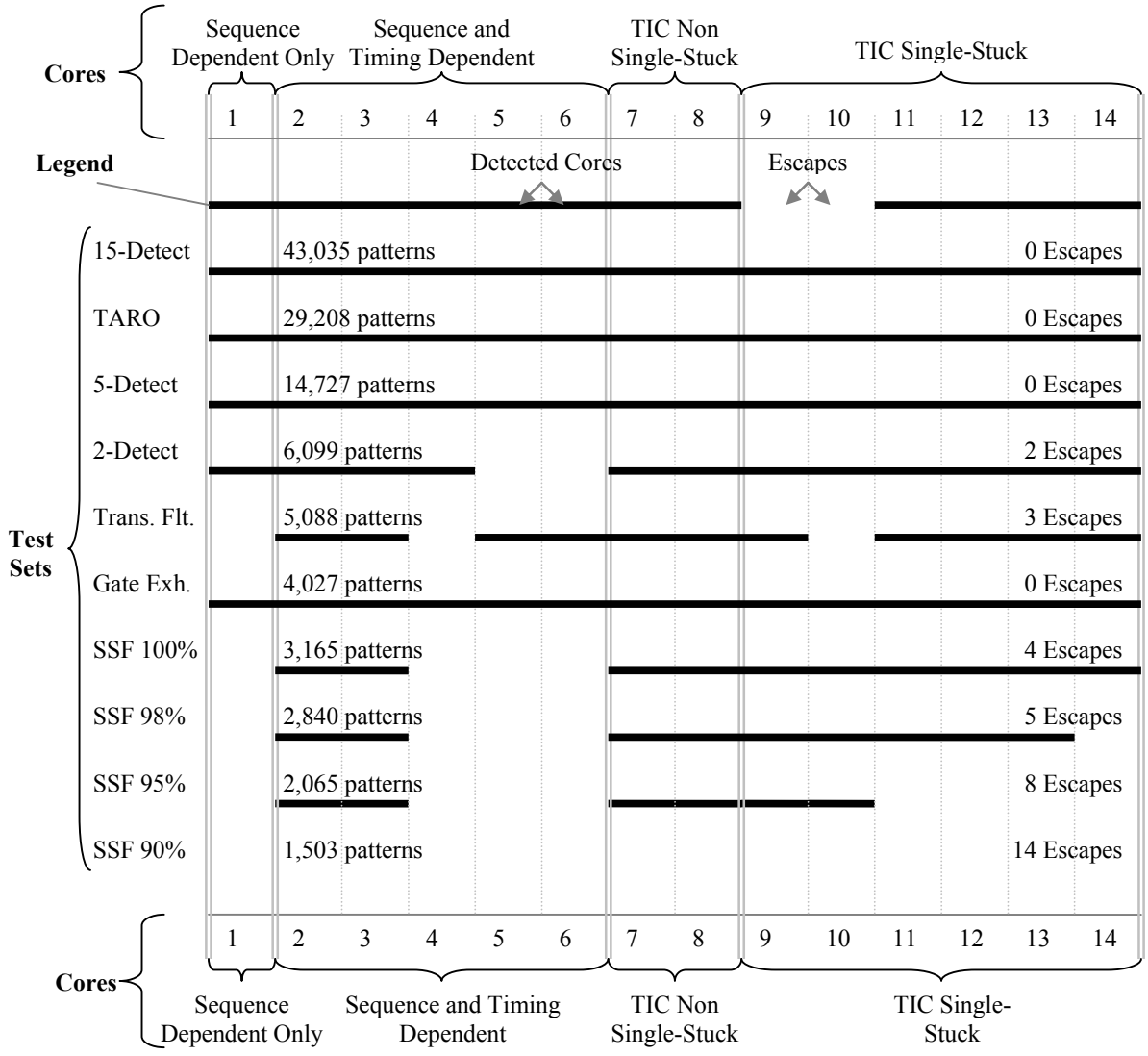


Figure 9: Defective chip class of ELF35 escapes

Table 2: Fault coverage of Murphy test sets for different metrics

Test Sets	Fault Coverages				Test Length
	TARO	Transition Fault	Single-Stuck Fault	Bridging Fault	
15-Detect	**89%**	**100%**	**100%**	**86%**	**7,186**
5-Detect	**83%**	**99%**	**100%**	**85%**	**2,403**
Bridging Fault	**69%**	**91%**	**98%**	**85%**	**1,062**
Transition Fault	**75%**	**100%**	**100%**	**83%**	**957**
Single-Stuck Fault	**65%**	**89%**	**100%**	**85%**	**547**
Single-Stuck Fault 98%	**56%**	**82%**	**98%**	**80%**	**395**
Single-Stuck Fault 95%	**53%**	**80%**	**95%**	**79%**	**351**

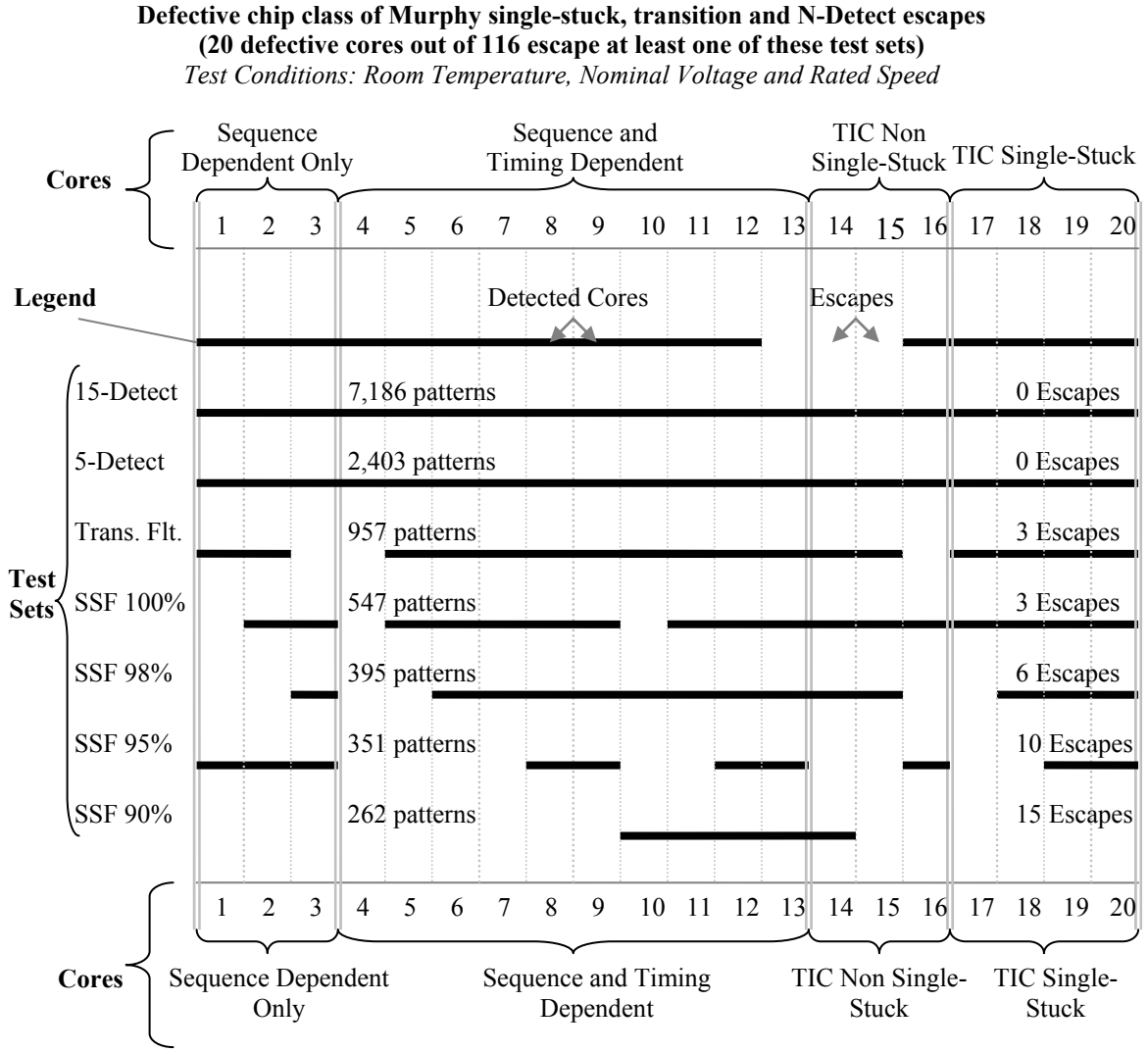


Figure 10: Defective chip class of Murphy escapes

4. Conclusion

The choice of test set metric or metrics for Digital IC test should be made on the basis of data such as that shown in Figures 9 and 10 of this paper. Such an approach allows the test engineer to make informed tradeoffs between test length and fault coverage. The choice of the second test set of a pair used for testing cannot be optimized without taking into account the nature of the first test set of the pair.

5. Acknowledgements

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