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<p>Abstract:</p> <p>This Technical Note contains a preprint of a paper submitted to the 15th IEEE VLSI Test Symposium to be held on April 27-30, 1997 at Monterey, CA.</p>	
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SHOrt Voltage Elevation (SHOVE) Test for Weak CMOS ICs

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ABSTRACT

A stress procedure for reliability screening, SHOrt Voltage Elevation (SHOVE) test, is analyzed here. During SHOVE, test vectors are run at higher-than-normal supply voltage for a short period. Functional tests and IDDQ tests are then performed at the normal voltage. This procedure is effective in screening oxide thinning, which occurs when the oxide thickness of a transistor is less than expected, and via defects. The stress voltage of SHOVE testing should be set such that the electrical field across an oxide is approximately 6MV/cm. The stress time can be calculated by using “effective oxide thinning” model. We will also discuss the requirement of input vectors for stressing complementary CMOS logic gates and CMOS domino logic gates efficiently.

1. INTRODUCTION

SHOVE testing aims at screening early-life failures and intermittent failures so that we can improve the quality level of CMOS ICs at low cost. In conjunction with other testing techniques, such as IDDQ testing [Levi 81] and Very-Low-Voltage (VLV) Testing [Hao 93] [Chang 96a] [Chang 96b], we can ensure CMOS ICs' quality without performing burn-in. During SHOVE, test sets, such as single stuck-at or pseudo stuck-at test sets, are run at higher-than-normal supply voltage for a short period. Some defects occurred after SHOVE can only be detected by functional tests and some can only be detected by IDDQ tests. Thus, functional tests and IDDQ tests should be performed at normal operating voltage after SHOVE. Figure 1 shows the procedure of SHOVE testing. It has been found that IDDQ values of some CUTs increase significantly after SHOVE [Duey 93] [Josephson 95]. SHOVE testing is useful at wafer sort. It can screen out weak parts during a wafer-level test and remove the cost of packaging them. This procedure has been widely practiced in industry [Kowalczyk 90] [Duey 93] [Josephson 95]. Some data which showed the correlation between the effectiveness of burn-in and SHOVE testing were reported recently [Barrette 96] [Kawahara 96]. However, no detailed analysis has been found in any published literature. This paper will provide a theoretical study of SHOVE testing.

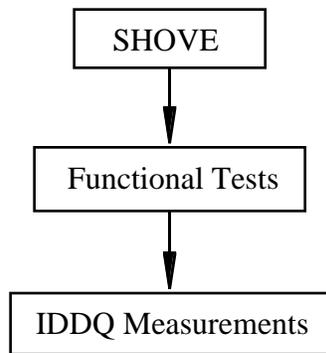


Figure 1 SHOVE testing procedure

Although burn-in can provoke various defects and improve the reliability of CMOS ICs [Hnatek 95], it increases the production cost and lengthens the test time. IDDQ testing can detect weak parts, which are ICs with low mean-time-to-failure (MTTF) [McCluskey 91], by measuring their quiescent currents. On the other hand, VLV testing can make weak parts fail functional tests at very low voltage. Both IDDQ testing and VLV testing do not change the characteristics of a circuit-under-test (CUT).

Unlike IDDQ testing and VLV testing, SHOVE testing detects weak parts by changing their intrinsic characteristics.

Oxide defects are one of the major causes for the reliability problems for CMOS ICs [Hnatek 95]. Particulate contamination, crystalline defects in the substrate, spot defects, localized thin regions, or surface roughness can cause localized weak spots in an oxide [Syrzycki 87] [Lee 88]. Moreover, the quality and lifetime of a gate oxide strongly depend on its thickness [Lee 88]. *Oxide thinning* occurs when the oxide thickness of a transistor is physically or effectively thinner than expected. Oxide thinning can be due to localized thin spots, traps in the oxide, surface asperity, or locally reduced tunneling barrier height [Schuegraf 94]. It can shorten the lifetime of a gate oxide, increase oxide leakage current, or cause time-dependent dielectric breakdown. As a result, it can cause early-life failures and must be detected. We investigated the device behavior during and after SHOVE. It is found that oxide thinning can cause stress-induced oxide leakage or become a gate oxide short after SHOVE and thus increase the IDDQ values of the defective CUT.

SHOVE can also make some via defects become opens, which can then be detected by either IDDQ measurements or functional tests depending on the characteristics of the resulting opens [Barrette 96] [Kawahara 96]. SHOVE, however, is less effective in stressing electromigration. Instead of using SHOVE tests, temperature stress is more effective to stress metalization because electromigration has bigger temperature activation energy [Hnatek 95]. On the other hand, temperature stress has less effects on oxide defects because of their low temperature activation energy [Hnatek 95].

To stress defective oxides effectively and still avoid damaging flawless oxides or causing latchup, the electrical field across the oxides, E_{ox} , must be carefully controlled. Fowler-Nordheim tunneling currents may occur across flawless oxides if E_{ox} is larger than a critical value. The excess tunneling currents flowing through gate oxides can damage the oxides. The damage can cause increased oxide leakage currents even after the supply voltage is reduced to the normal operating voltage. Based on various published measurement data, the critical E_{ox} to avoid the Fowler-Nordheim tunneling current is approximately 6MV/cm [Moazzami 92] [Dumin 93] [Dumin 94] [Watanabe 94] [Depas 96]. E_{ox} at the normal operating voltage for different technologies is always well below this critical value [Schutz 94] [Charnas 95] [Sanchez 96] [Montanaro 96]. By applying the critical E_{ox} across the flawless oxide during SHOVE, we can maximize the stress effects on the defective oxides and also minimize the stress time.

In a CMOS IC, each transistor must be stressed for enough time during SHOVE. To effectively stress an NMOS transistor, the gate of the transistor should be held at the stress voltage and the drain and source of the transistor at 0V. Similarly, to effectively stress a PMOS transistor, the gate of the transistor should be held at 0V and the drain and source of the transistor at the stress voltage. Both single stuck-at and pseudo stuck-at test sets can be the stress vectors for SHOVE testing for fully

complementary static CMOS logic. We also investigated the toggle probability of various test sets in a CUT. For pseudo stuck-at test sets, some nodes were in logical one or zero for one or two vectors only. Thus, each vector must be held for at least the stress time for a transistor to make sure all transistors in a CMOS IC are stressed for enough time. For domino-type dynamic CMOS logic, only an all-one vector is required to stress all the transistors within each functional block. The stress speed should be the reciprocal of the stress time for a transistor in this case. The stress time of a transistor is the time to effectively stress an oxide.

This paper is organized as follows. Section 2 examines the behavior of oxide thinning via defects during and after SHOVE. Section 3 discusses the stress voltage. Section 4 investigates the stress vectors. Section 5 analyzes the stress time and stress speed. Section 6 concludes this paper.

2. OXIDE THINNING AND VIA DEFECTS

SHOVE testing can increase the leakage current or cause oxide breakdown in a defective oxide whose thickness is less than expected. Oxide thinning shortens the lifetime of an oxide. As the oxide thickness is decreased in advanced technologies [Charnas 96] [Gronowski 96] [Montanaro 96] [Sanchez 96], oxide thinning becomes a more serious problem. Furthermore, as the number of metal layers increases in most advanced technologies, via defects are more likely to occur. SHOVE testing can make some via defects become permanent opens.

Several models have been proposed to predict the lifetime of an oxide and the onset criteria of oxide breakdown. Lee *et al.* proposed using “effective oxide thinning” to characterize time-dependent-dielectric-breakdown [Lee 88]. Sune *et al.* proposed a statistical description of oxide breakdown based on neutral trap generation in the oxide during wearout [Sune 90]. Dumin *et al.* found out that breakdown occurred locally when the local density of traps exceeded a critical value and the product of the electric field and the higher leakage currents through the traps exceeded a critical energy density [Dumin 94]. We use the “effective oxide thinning” model to estimate the lifetime of an oxide in this paper because this model shows the relationship among the voltage across an oxide, effective oxide thickness, and oxide lifetime more directly than other models. Equation 1 shows the relationship among these parameters. X_{eff} is the effective oxide thickness, V_{ox} is the voltage across the oxide, t_{BD} is the time-to-breakdown of the oxide, τ_0 is determined by the intrinsic breakdown time under an applied voltage of V_{ox} , and G is the slope of $\log(t_{BD})$ versus $1 / E_{ox}$.

$$t_{BD} = \tau_0 \exp\left(\frac{GX_{eff}}{V_{ox}}\right) \quad (1)$$

Figure 2 shows the lifetime of a defective oxide at different voltages for three different technologies. The oxide thickness of the 2V technology is 6.5nm, that of the 3.3V technology is 9nm, and that of the 5V technology is 15nm. The thickness of the defective oxide is assumed to be half that of a flawless oxide. We assumed that the voltage across the oxide is approximately the same as the supply voltage. t_{BD} was calculated by using Equation 1. G is 350 MV/cm and τ_0 is 10 picoseconds [Lee 88].

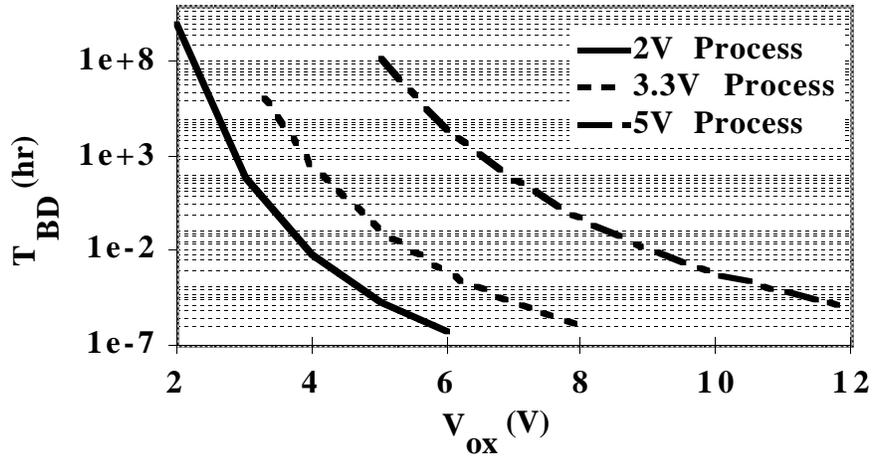


Figure 2 Lifetime of defective oxides for three different technologies

Figure 2 shows that the lifetime of a defective oxide decreases significantly as the supply voltage is increased. Moreover, the amount of supply voltage increment is relative to the normal operating voltage for each technology. The stress time at high voltage is much shorter than that at normal voltage. SHOVE testing should stress CUTs without affecting the property of flawless oxides significantly. Although the lifetime of a flawless oxide is shortened at high voltage, SHOVE test does not affect the lifetime of a flawless oxide due to the short stress period.

Researchers have reported the existence of stress-induced leakage current in a thin oxide film [Naruke 88] [Rofan 91] [Moazzami 92] [Dumin 93] [Patel 94]. It is found that the oxide leakage at low voltage increased in a thin oxide after the thin film was stressed at high voltage. The leakage current occurs before oxide breakdown and can be one of the major failure mechanisms in thin oxides.

The poly gate and channel region of a MOS transistor are highly doped. The energy barrier width is very thin at the defective site. Consequently, tunneling current occurs at the thin spot when an electrical field is applied across the oxide. The magnitude of the tunneling current increases significantly as the supply voltage increases over its normal value [Moazzami 92] [Dumin 93] [Lee 94]. Large tunneling currents can cause damage in an oxide layer and thus increase oxide leakage current. The failure mechanisms that cause the stress-induced oxide leakage can be localized defects [Olivo 88],

localized positive charges [Maserjian 82], or trap states near the injecting surface [Rofan 91] [Moazzami 92]. These mechanisms further make X_{eff} in Equation 1 smaller and thus shorten the lifetime of an oxide. If the oxide thickness at the defect spot is very thin or the CUT is stressed for enough time, oxide breakdown may occur. Both stress-induced oxide leakage and oxide breakdown can significantly increase the quiescent current of a defective CUT.

Via defects can cause high leakage, timing failure, or functional failure depending on the failure modes [Hnatek 95]. Missing vias between two metal layers can cause functional failure. On the other hand, via undercut can cause a short circuit between two metal layers and thus increase the leakage. The short can also cause timing or functional failure depending on the resistance of the short.

The transient current during SHOVE can make some via defects become opens and thus cause functional failure or leakage. These via defects have high resistance before becoming opens. These defects increase the propagation delay of the signals passing through the vias. They can cause intermittent failure or early-life failure. Therefore, they need to be detected to ensure IC quality. Because the resulting open vias after SHOVE may either cause functional failure or high leakage, both IDDQ tests and functional tests should be performed after SHOVE to be able to catch these defects.

SHOVE could burn off unexpected shorts between two metal layers and heal the CUTs if the shorts are thin wires or spot defects. These shorts have high resistance. Thus, it is more likely that the heat generated by the transient or static current across the shorts during SHOVE can burn off the shorts.

We only consider the characteristics of an oxide to determine the parameters for SHOVE tests because the lifetime of an oxide is more sensitive to voltage than that of a via.

3. STRESS VOLTAGE

To stress CUTs effectively, the stress voltage should be set such that it can only cause damage in the defective CUTs and avoid damaging flawless CUTs. Because the damage to an oxide at high voltage is mainly due to the tunneling current flowing through the oxide, the stress voltage should be selected so that the oxide tunneling current is very small in a flawless oxide but large in a defective oxide. Two types of tunneling mechanisms, Fowler-Nordheim tunneling and direct tunneling, can appear across an oxide. For most 3.3V and 5V technologies, the oxide thickness of a MOS transistor is larger than 6nm [Schutz 94] [Charnas 95] [Montanaro 96] [Sanchez 96]. Moreover, direct tunneling currents exist in a thin SiO₂ film whose thickness is less than 6nm [Schuegraf 92]. Consequently, Fowler-Nordheim tunneling currents dominates in the flawless oxide at high voltages for most 3.3V and 5V technologies. On the other hand, direct tunneling currents may exist at the thin spot in a defective oxide.

The magnitude of Fowler-Nordheim tunneling current strongly depends on E_{ox} [Schuegraf 92]. Based on various published measurement data, the magnitude of the Fowler-Nordheim tunneling current across an oxide becomes significant when E_{ox} is larger than 6MV/cm [Moazzami 92] [Dumin 93] [Dumin 94] [Watanabe 94] [Depas 96]. Figure 3 shows the qualitative relationship between the Fowler-Nordheim tunneling current and E_{ox} . If the stress voltage is selected so that E_{ox} is approximately 6MV/cm in a flawless oxide, E_{ox} across a defective oxide will be much larger than this value. Thus, the tunneling current can flow through the defective site and increase the trap density at the thin spot during SHOVE. Table 1 shows the lifetime of a flawless oxide for the 3.3V technology used in Fig. 1 based on Equation 1. The lifetime of an oxide decreases significantly when the oxide is constantly stressed by an electric field stronger than 6 MV/cm. On the other hand, slight increment on E_{ox} does not threaten the lifetime of an oxide too much. Moreover, due to the short stress time, SHOVE testing almost does not affect the oxide quality of a defect-free CUT. Table 2 lists E_{ox} at normal operating voltages for several technologies. For these technologies, E_{ox} at the normal operating voltage is well below 6MV/cm. In Table 2, V_{dd} is the supply voltage and X_{ox} is the oxide thickness.

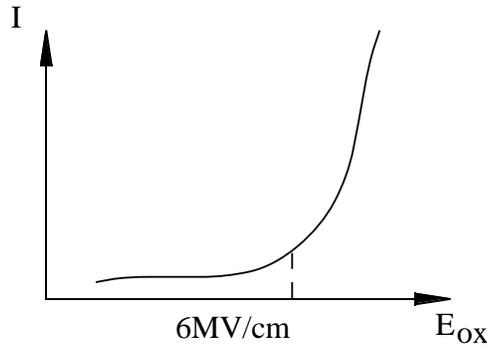


Figure 3 Fowler-Nordheim tunneling current vs. E_{ox}

Table 1 Lifetime of a flawless oxide for a 3.3V technology

V_{ox}	E_{ox} (MV/cm)	t_{BD}
3.3	3.67	9.04×10^{22} yrs
4.0	4.44	5.04×10^{15} yrs
5.0	5.56	7.26×10^8 yrs
6.0	6.67	20,041 yrs
7.0	7.78	11.1 yrs
8.0	8.89	14.6 days

Table 2 Maximum E_{ox} at normal operating voltages

Technologies	V_{dd} (V)	X_{ox} (nm)	E_{ox} (MV/cm)
[Schutz 94]	5	15	3.33
[Charnas 95]	3.3	8.5	3.88
[Sanchez 96]	2.5	7	3.57
[Montanaro 96]	2	6.5	3.08

Based on Equation 1, the higher the stress voltage is used, the shorter the stress time will be. Consequently, to shorten the stress time, the stress voltage should be selected so that it can maximize the effect of the stress on the oxide layers of CUTs. The stress time can be reduced significantly by using the maximum allowed voltage during SHOVE.

Consequently, depending on the oxide thickness of a technology, the stress voltage for SHOVE testing can be determined. Equation 2 shows the maximum stress voltage for SHOVE testing. The unit of X_{ox} is nm.

$$V_{stress} = X_{ox} \times 0.6V / nm \quad (2)$$

4. STRESS VECTORS

To thoroughly stress all the transistors in a CMOS IC and avoid long stress time, stress vectors must be selected so that the voltage across the oxide layer of a transistor is maximized. For an NMOS transistor, its source, drain, and substrate should be held at 0V, at the same time, the gate of the transistor is held at the stress voltage. For a PMOS transistor, its source, drain, and substrate should be held at the stress voltage and the gate of the transistor is held at 0V. Consequently, to effectively stress an NMOS transistor in a fully complementary CMOS logic gate, the stress vector should connect the logic gate output of and ground through the pull-down path that contains the target NMOS transistor. Similarly, to effectively stress a PMOS transistor in a fully complementary CMOS logic gate, the stress vector should connect the logic gate output and the supply voltage through the pull-up path that contains the target PMOS transistor.

To provoke a stuck-at-1 fault at the input of a complementary CMOS logic gate and propagate the fault effect to the output of the logic gate, the stuck-at vector will place logical 0 at the input of a PMOS transistor whose gate is connected to the faulty input node. In this way, the vector connects the output of the logic gate to the supply voltage through the PMOS transistor whose input gate is connected to the faulty input node. Thus, the PMOS transistor is put into the stress condition described in the previous paragraph. To provoke a stuck-at-0 fault at the input of a complementary CMOS logic gate and

propagate the fault effect to the output of the logic gate, the stuck-at vector will place logical 1 at the input of an NMOS transistor whose gate is connected to the faulty input node. Similar to the vector for a stuck-at-1 fault at the input of the logic gate, the vector connects the output of the logic gate to ground through the NMOS transistor whose gate is connected to the faulty input node. As a result, the NMOS transistor is put into the stress condition mentioned in the previous paragraph. Moreover, a 100% single stuck-at test of a complementary CMOS logic gate can toggle all input nodes of the logic gate. Thus, a 100% stuck-at test set for a complementary CMOS logic gate can put each transistor in the required stress condition at least once. Thus, both 100% single stuck-at test sets and pseudo stuck-at test sets can be used as the stress vectors for SHOVE. The latter are more suitable than the former because of their shorter test lengths. On the other hand, 100% toggle test sets may still miss some transistors. IDDQ test sets that target inter-gate bridging faults are not suitable for SHOVE testing. Figure 4 shows a fully complementary CMOS gate. Table 3 shows how transistors are stressed by stress vectors. The four italicized rows include a set of 100% stuck-at test set. All transistors are stressed by this stuck-at test set.

Because not all transistors are stressed by each test vector, some transistors may be stressed longer than others. Table 3 shows that all-zero vectors can stress all PMOS transistors and all-one vectors can stress all NMOS transistors at once. To stress all transistors evenly and reduce the stress time for fully complementary CMOS logic gates, all-one and all-zero vectors can perform better than stuck-at test sets as the stress vectors.

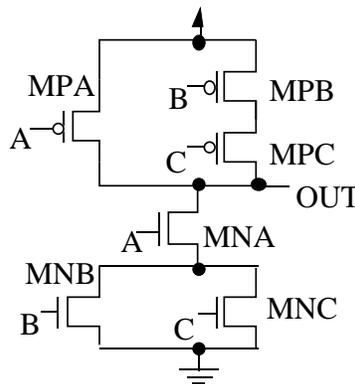


Figure 4 Fully complementary CMOS logic gate

We can modify the algorithm for line justification used in existing ATPG programs to generate all-zero and all-one vectors. To justify the output value of a logic gate, the inputs of the logic gate should be set to either all ones or zeros. For example, if we want to set the output of a 2-input OR gate to be logical one, we should put logical ones on both inputs of the gate. In existing ATPG programs, only one of the two inputs will be set to logical one.

Table 3 Stress vectors and the stressed transistors for a fully complementary CMOS logic gate

A	B	C	MPA	MPB	MPC	MNA	MNB	MNC
0	0	0	X*	X	X			
0	0	1	X					X
0	1	0	X				X	
0	1	1	X				X	X
1	0	0		X	X			
1	0	1				X		X
1	1	0				X	X	
1	1	1				X	X	X

* the transistor is stressed when the vector is applied

For CMOS domino logic, an all-one vector is sufficient to put all transistors in a domino logic gate in the stress condition. Moreover, we can stress all the transistors in a logic block that is built by domino logic by using only the all-one vector at the primary inputs of the domino logic block. Figure 5 shows a CMOS domino logic gate. Keepers can be put at proper internal nodes to ensure enough noise margin and avoid charge sharing problems [Colwell 95]. To simplify the discussion, the keepers do not appear in the domino logic gate we use in this paper. However, the conclusion can be extended to the domino logic gate which has keepers implemented.

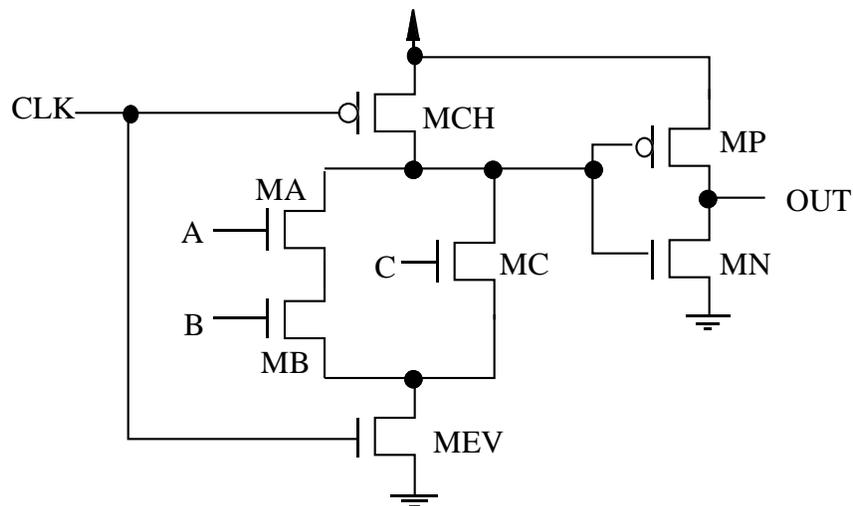


Figure 5 CMOS domino logic

During the precharge phase, the precharge PMOS transistor (transistor MCH in Fig. 5) and the NMOS transistor in the output inverter of a domino logic gate (transistor MN in Fig. 5) are stressed. During the evaluation phase, if all the inputs are logic one, all transistors in the evaluation branches (transistor MA, MB, MC, and MEV in Fig. 5) and the PMOS transistor in the output inverter of a domino logic gate (transistor MP in Fig. 5) are in the stress condition. Moreover, the output of the domino logic is logic one during the evaluation phase. Consequently, we can set the inputs of all domino gates within a logic block to be logic one by putting all primary inputs of the logic block to be logic one. Thus, only one vector is required to put all transistors within a logic block that is built by domino logic in the stress condition. Table 4 summarizes the discussion of the stress vectors for CMOS domino logic.

Table 4 Stress vectors for CMOS domino logic

Input Condition	MCH	MEV	MP	MN	MA	MB	MC
Precharge Phase	X*			X			
Evaluation Phase with All-one at the Inputs		X	X		X	X	X

* the transistor is stressed during the described input condition

5. STRESS TIME AND STRESS SPEED

Each transistor in a CMOS IC must be stressed for long enough to make sure the defective oxide deteriorates significantly so that either oxide breakdown or stress-induced oxide leakage occurs in the defective oxide. To optimize the stress effect of each stress vector and thus reduce the total stress time, each signal should be held at its full-swing signal level for enough time. In this way, transistors can be in the condition mentioned in Sec. 4 and thus be stressed efficiently by the stress vectors.

If a transistor can be stressed more than once during SHOVE by different stress vectors, we can reduce the overall stress time for a CMOS IC. Equation 3 shows the stress time of a CMOS IC. In Equation 3, T_{sl} is the overall stress time of a CMOS IC, n is the number of stress vectors, T_{st} is the stress time for each transistor at the applied stress voltage, and m is the minimum number of vectors that stress a transistor for all transistors in the CUT. T_{st} can be calculated by using Equation 1.

$$T_{sl} = n \times T_{st} / m \quad (3)$$

To determine an appropriate value for m , we investigated a CUT which was used in an experiment [Franco 95]. The CUT was implemented by using only elementary CMOS logic gates. It

has 380 gates, 24 inputs, 12 outputs, and 283 internal nodes. Seven 100% single stuck-at test sets and two pseudo stuck-at test sets were used in this study. We simulated all test sets and recorded how each node toggled.

For the two pseudo stuck-at test sets, there was at least one node that was in the logic zero state only once for all test vectors. Thus, m should be 1 for these two test sets. The stress speed for this CUT should be the reciprocal of the stress time for a transistor if pseudo stuck-at test sets are used. For 5 out of the 7 100% single stuck-at test sets, each node was in logic zero or logic one state at least twice among all test vectors. As a result, m can be set at 2 for these test sets. Nevertheless, 97% of the nodes were in logic zero or logic one more than 4 times among all vectors in all 7 100% single stuck-at test sets.

As explained in the previous section, only one vector is sufficient to put all the transistors in the stress condition for CMOS domino logic. Consequently, for CMOS domino logic, we can hold the logic block in the precharge phase for the stress time of a transistor and then hold the primary inputs of the logic block in logic one state for the same amount of stress time during the evaluation phase.

6. SUMMARY AND CONCLUSION

We have described the IC failures that can be detected by SHOVE testing. SHOVE testing can detect most oxide defects and some via defects. Both defects can cause early-life failures and intermittent failures and thus reduce IC quality. Pseudo stuck-at test sets or stuck-at test sets can put all transistors of CUTs in the suggested stress conditions. The stress time can be determined by using the “effective oxide thinning” model and analyzing the test sets. The stress time can be shortened if multiple vectors can put transistors in their stress conditions more than once.

SHOVE testing, VLV testing, IDDQ testing, and burn-in all aim at improving the quality level of CMOS ICs. We have shown that SHOVE testing can detect weak CMOS ICs caused by oxide defects and via defects. SHOVE testing requires shorter test time than burn-in and does not need extra instruments. Consequently, SHOVE testing is an alternative to burn-in and can be used with VLV testing and IDDQ testing to improve the quality level of CMOS ICs and reduce the production cost.

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