

BIBLIOGRAPHY OF 1988 CRC PUBLICATIONS

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ABSTRACT

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LIST OF PUBLICATIONS

JOURNAL PAPERS

Published

- [Liu 88] Liu, D.L., and E.J. McCluskey, "Design of Large Embedded CMOS PLA for Built-In Self-Test," *IEEE Trans. CAD*, Vol. 7, No. 1, pp. 50-59, Jan. 1988.(DARPA)
- [Mahmood 88] Mahmood, A., and E.J. McCluskey, "Concurrent Error Detection Using Watchdog Processors - A Survey," *IEEE Trans. Comput.*, Vol. 37, No. 2, pp. 160-174, Feb. 1988.(NSF & Rolm)
- [McCluskey 88] McCluskey, E.J., S. Makar, S. Mourad, and K.D. Wagner, "Probability Models for Pseudorandom Test Sequences," *IEEE Trans. CAD*, Vol. 7, No. 1, pp. 68-74, Jan. 1988.(ONR)
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- [Saxena 88] Saxena, N.R., and J.P. Robinson, "Syndrome and Transition Count are Uncorrelated," *IEEE Trans. on Info. Theory*, Vol. 34, No. 1, pp. 64-69, Jan. 1988.
- [Wang 88] Wang, L.T., and E.J. McCluskey, "Hybrid Designs Generating Maximum Length Sequences," *IEEE Trans. CAD*, Vol. 7, No. 1, pp. 91-99, Jan. 1988.(NSF)
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- [Wang 88] Wang, L.T., and E.J. McCluskey, "Circuits for Pseudo-Exhaustive Test Pattern Generation Using Cyclic Codes," *IEEE Trans. CAD*, Vol 7, No. 10, pp. 1068-1080, Oct. 1988.(NSF & AIDA)

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- Liu, D.L., and E.J. McCluskey, "CMOS Circuit Design for Testability," *Journ. of Semicustom IC's* .(DARPA)
- McCluskey, E.J., and F. Buelow, "IC Quality and Test Transparency," *IEEE Trans. on Industrial Electronics*. (ONR & NSF)
- Mourad, S., J.L.A. Hughes, J.G. Udell JR., and E.J. McCluskey, "Stuck-at Fault Detection in Parity Trees," *Computer Systems Science and Engineering*. (ONR)
- Mourad, S., and E.J. McCluskey, "Testability of Parity Checkers," *IEEE Trans. on Industrial Electronics*.
- Wang, L.T., and S. Mourad, "Scan self-test for sequential machines," *IEE Proceedings-E Computers and Digital Techniques*, United Kingdom.(NSF)

CONFERENCE PAPERS

Published

- [Makar 88] Makar, S.R., and E.J. McCluskey, "On The Testing Of Multiplexers," *Proc. 1988 Int. Test Conf.*, Washington, DC, pp. 669-679, September 12-14, 1988. (DEC) (CRC TR 88-5)
- [McCluskey 88] McCluskey, E.J., and F. Buelow, "IC Quality and Test Transparency," *Proc. 1988 Int. Test Conf.*, Washington, DC, pp. 295-301, September 12-14, 1988.(NSF) (CRC TR 88-5)
- [McCluskey 88] McCluskey, E.J., "Practice and Theory," *Proc. 1988 Int. Test Conf.*, Washington, DC, pp. 203-204, September 12-14, 1988 (NSF) (CRC TR 88-5)
- [Millman 88] Millman, S.D., and E.J. McCluskey, "Detecting Bridging Faults With Stuck-at Test Sets," *Proc. 1988 Int. Test Conf.*, Washington, DC, pp. 773-783, September 12-14, 1988. (ONR) (CRC TR 88-5)
- [Mourad 88] Mourad, S., and E.J. McCluskey, "On Benchmarking Digital Testing Systems," *Proc. 1988 Int. Test Conf., Poster Session*, Washington, DC, pp. 997, September 12-14, 1988.(NSF) (CRC TR 88-5)
- [Mourad 88] Mourad, S. "Digital Testing: Theory and Practice," *Proc. 1988 Int. Test Conf.*, Washington, DC, pp. 205-206, September 12-14, 1988. (NSF) (CRC TR 88-5)
- [Nanya 88] Nanya, T., S. Mourad, and E.J. McCluskey, "Multiple Stuck-at Fault Testability of Self-testing Checkers," *Dig. 18th Annu. Int. Symp. Fault-Tolerant Comput. (FTCS-18)*, Tokyo, Japan, June 27-30, 1988.(ONR)
- [Udell 88] Udell, J.G. Jr., "Reconfigurable Hardware for Pseudo-Exhaustive Test," *Proc. 1988 Int. Test Conf.*, Washington, DC, pp. 522-530, September 12-14, 1988. (Tektronix) (CRC TR 88-5)
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- [Mourad 88] Mourad, S., and E.J. McCluskey, "Fault Analysis Using Signature Analyzers," *1989 International Conference on Circuits and Systems*, Nanjing, China, July 6-8, 1989.
- [Wang 88] Wang, L.T., M. Marhofer, and E.J. McCluskey, "A Self-Test and Self-Diagnosis Architecture for Boards Using Boundary Scans," *European Test Conference*, Paris, France, April 12-14, 1989. (NSF & FRG)

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- (CRC TR 88-3) Goosen, H. A., and T. Nanya, "The Byzantine Hardware Fault Model," May 1988.(ONR)
- (CRC TR 88-4) McCluskey, E.J., "Design Techniques for Testable Embedded Error Checkers," May 1988.(NSF)
- (CRC TR 88-5) McCluskey, E.J., "Preprints of the 1988 IEEE International Test Conference, Washington, D.C., September 12-14, 1988, and the Fault-Tolerant Computing Symposium-18, Tokyo, Japan, June 27-30, 1988."
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- (CRC TR 88-8) Amer, H.A., and E.J. McCluskey, "Safe and Unsafe faults in CMOS Exclusive-Or Gates with Gate Oxide Shorts," Sept. 1988. (ONR).
- (CRC TR 88-9) Saxena, N., and E.J. McCluskey, "Analysis of Checksums, Extended-Precision Checksums and Cyclic Redundancy Checks," Sept. 1988. ((NSF & HP).
- (CRC TR 88-10) Udell, J.G. Jr., and E.J. McCluskey, "Circuit Reduction for Efficient Segmentation," Dec. 1988. (Tektronix, NSF & ONR).
- (CRC TR 88-11) Udell, J.G. Jr., and E.J. McCluskey, "An Efficient Segmentation Program for Pseudo-Exhaustive Test," Dec. 1988. (Tektronix, NSF & ONR).
- (CRC TR 88-12) Udell, J.G. Jr., and E.J. McCluskey, "Pseudo-Exhaustive Test and Segmentation: Formal Definitions and Extended Fault Coverage Results," Dec. 1988. (Tektronix, NSF & ONR).

PRESENTATIONS

- Marhoefer, M., "Structuring Circuit Descriptions for Testing Applications," *IEEE Design Automation Workshop*, Apache Junction, AZ, Jan. 13-15, 1988.
- McCluskey, E.J., "IC Quality and Test Transparency," *University of California at Berkeley, Seminar*, Feb. 29, 1988.
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- McCluskey E.J., "IC Quality and Test Transparency," *Computer Science & EE Colloquium*, Oregon State University, May 9, 1988.
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- Saxena, N.R., "Arithmetic Checksums and Cyclic Redundancy checks are Almost Orthogonal," *1988 International Symposium on Information Theory, Recent Result Session II*, Kobe, Japan, June 21, 1988.
- Saxena, N.R., "Syndromes and Transition Count are Uncorrelated," *1988 International Symposium on Information Theory, Session Coding IV*, Kobe, Japan, June 23, 1988.
- McCluskey, E.J., "Pseudorandom Test Sequences," *Stanford Computer Forum Presentation*, Rolm Mil-Spec Computers, Aug. 10, 1988.
- McCluskey, E.J., "Undetected Bad Chips," *USSR Academy of Science Institute of Information Transmission Problems*, Moscow, USSR, Sept. 20, 1988.
- McCluskey, E.J., "Required Fault Coverage," *Institute of Electronics and Computer Science of Latvian Academy of Science*, RIGA, Latvia, Sept. 24, 1988.
- McCluskey, E.J., "Required Fault Coverage," *The Institute of Control Problems, USSR Academy of Science*, Moscow, USSR, Sept. 28, 1988.
- McCluskey, E.J., "Invited Keynote," *Creating Reliable Products Conference*, Palo Alto, CA., Oct. 11-14, 1988.
- McCluskey, E.J., "Production Testing of Digital Integrated Circuits," *Coordinated Science Lab Seminar*, University of Illinois, Oct. 31, 1988.
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- McCluskey, E.J., "Production Testing of Digital Integrated Circuits," *The Louisiana Distinguished Lecture Series*, Lafayette, Louisiana, Nov. 4, 1988.
- McCluskey, E.J., "High Yield and Reliability at 10^8 Devices/Chip-What Does It Mean, and How Do We Achieve It?," *IEDM*, San Francisco, CA, Dec. 11-14, 1988.

1988 VISITORS

- Dr. Balaji Krishnamurthy, Tektronix, Inc., Beaverton, Oregon, Jan. 1988.
- Ed Scott, NCR, Jan. 1988.
- Prof. Vladimir G. Lazarev, The Academy of Sciences of the USSR, March 1988.
- Prof. Ivars Bilinskis, Latvian SSR Academy of Sciences, March 1988.
- Prof. Jan M. Torin, Chalmers University of Technology, Sweden, May 1988.
- Mats Svenningsson, SAAB Space, Sweden, May 1988.
- Dr. Edward Eichelberger, IBM, Kingston, New York, May 1988.
- Prof. Wojciech Maly, Carnegie Mellon University, Pittsburgh, PA, May 1988.
- Peter P. Schirling, IBM, Essex Junction, VT, June 1988.
- J.R. Turnbull, Jr., IBM, Essex Junction, VT, June 1988.
- Dr. Ulrich Finger, Centre National D'Etudes Des Telecommunications, Issy Les Moulinaux, France, June 1988.

Jean-Emmanuel Hanne, Centre National D'Etudes Des Telecommunications, Issy Les Moulinaux, France, June 1988.
Akira Motohara, Matsushita Electric Industrial Co., Ltd., Japan, June 1988.
Dr. John F. Cassidy, Jr., GE Corporate Research and Development, Schenectady, NY, Aug. 1988.
Alain Jeneveau, Dean of Studies and Research, Ecole Polytechnique Febrinine, Seaux, France, Nov. 1988
Dr. Yutaka Ohno, President ASTEM RI/Kyoto, Advanced Software Technology & Mechatronics Research Institute of KYOTO, Kyoto, Japan, Nov. 1988

1988 SCHOLARS VISITING CRC

Dr. Michael Marhofer, Universitaet Karlsruhe, West Germany.
Prof. Kishor S. Trivedi, Duke University, Durham, North Carolina, CA.
Prof. John P. Shen, Carnegie Mellon, Pittsburgh, PA.
Mr. Toyokazu Tatsuta, Hitachi, Ltd. Yokohama, Japan.
Mr. Katsunobu Muroi, Mitsubishi Electric Corporation, Kanagawa Prefecture 247, Japan

CRC PhDs GRANTED

J. Udell, "Pseudo-Exhaustive Testing of Digital Integrated Circuits," 1988 (CRC)

TECHNICAL FACILITIES CENTER FOR RELIABLE COMPUTING

- AIDA Design System:** Apollo 550-based design and testing workstation with 65M hard disk and printer. Includes software for design verification, timing analysis, logic and fault simulation, automatic test pattern generation, SPICE-like analog simulation, etc.
- Daisy MegaLogician Design System:** Intel 286-based workstation with 80M hard disk, printer, graphics accelerator, and hardware accelerator for fast fault simulation. Includes software for schematic capture, (batch or interactive) logic and fault simulation, testability analysis, etc., and also includes cell libraries for various integrated circuit technologies.
- Tektronix 4404 Artificial Intelligence Workstation:** Motorola 68010-based workstation with 4M internal memory, 35M hard disk, and Ethernet capability. Runs Smalltalk, C, and LISP.
- Tektronix Design Analysis System (DAS 9200):** Motorola 68010-based test system with 2M memory, 20M hard disk, and color display. Equipped with a 32-channel 50 MHz pattern generation card, two 16-channel 200MHz data acquisition cards, 92 DV device verification software, and TF 100 test fixture.
- Apple II Personal Computers:** One Apple II, two Apple II+, and one Apple IIe personal computer connected to various printers.
- Apple Macintosh Personal Computers:** Two Macintosh personal computers, each with 1M internal memory and two disk drives. An Appletalk network connects the Macs to an Apple Laserwriter printer.
- Digital Professional 350 Personal Computers:** Two Digital Professional personal computers with hard disks.
- IBM Personal Computers:** IBM PC-AT personal computer with enhanced graphics board, high-resolution color monitor, hard disk, and printer. Includes ViewLogic software for schematic capture, simulation, waveform analysis, and fault grading. IBM PC-RT reduced instruction set personal computer with high resolution color monitor, hard disk, streaming tape drive, and Ethernet capability.

VAX Computers: MicroVAX GPX II running VMS with 70M and 140M hard disks and 13M main memory. Ethernet capability . Access to a VAX 780 running Unix #WF70608 780.

Laboratory Oven: AES Model ZCK-9204 laboratory oven to be used for accelerated life testing and burn-in.

Sun 3/140 work station running Unix, with two 70M hard disks. Ethernet capability #708ES613.

Delni-aa ethernet multiplexer and a transceiver providing access to the ethernet for the Microvax, Sun, TEK 4317, and PC-RT. Capability to extend access to five more workstations.

DAS9252: 1Tester mainframe, keyboard and monitor. Includes board and accompanying flying lead set for microprocessor testing (90 channels), 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes, 18-channel 50 MHz pattern generator, Test fixture, 21x21 pin grid array fixture to fit TF100

4696: 1Color ink-jet printer.

Tektronix Lab Instruments: MHz function generator, 40 MHz function generator - very fancy, 2 Triple power supplies, 2 Digital Multimeters, 5 Coax cables for connecting FGs to boards, 2 Mainframes to hold one each of PS, DM, and FG.

2467:1350 MHz four channel portable oscilloscope with word recognizer.

1241BNO-1B: 1 Color logic analyzer mainframe, 2 18-channel cards, 1 9-channel card, 5 P6460 probes, performance analysis ROM pack, 64K RAM pack, parallel printer COMM pack, printer support ROM pack

4317: 1 Color graphics workstation

TECHNICAL FACILITIES SOFTWARE SYSTEMS

The lab houses 7 digital testing Systems: Teradyne, EDA's Aida and Lasar, Genrad's HILO, HHB's CADAT and Intelligen, and Gateway's Verilog, a Daisy system.

AIDA: A Unix-based system that consists of a logic simulator, a fault simulator, and an Automatic Test Pattern Generator (ATPG) for combinational circuit. The system also includes design rule verification and timing verification.

Lasar: This VMS-based system is hosted on a MicroVax and consists of logic and fault simulators, an ATPG for both combinational and sequential circuits. The system includes large model libraries.

Hilo: GenRad's Hilo comprises logic and fault simulators and a test pattern generation.

CADAT 6.1: CADAT is a logic and fault simulator that is suitable for combinational and sequential circuits. Intelligen is a sequential test pattern generator.

Verilog: Hardware description language and simulator.

Daisy: The Daisy system consists of logic, fault simulators testability analysis program and ATPGs. It is based on Daisy's unix (Denix). It includes an extensive layout system.

Viewlogic: This is a schematic capture and a logic simulator that is also capable of injecting same faults in the design. The system is mainly used for logic design courses.

Spice: Spice systems for analog simulation of devices and circuits: tSpice is hosted on the Tektronix and pSpice on the IBM AT.