

BIBLIOGRAPHY OF 1989 CRC PUBLICATIONS

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ABSTRACT

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Published

- [Lau 89] Lau, C., C.M. Hu, and E.J. McCluskey, "Research in Advanced Electronic System Reliability," *Naval Research Reviews*, Vol. XLI, pp. 9-19, Three/1989. (ONR)
- [McCluskey 89] McCluskey, E.J., and F. Buelow, "IC Quality and Test Transparency," *IEEE Trans. on Industrial Electronics*, Vol. 36, No. 2, pp. 197-202, May 1989. (ONR, NSF)
- [Mourad 89] Mourad, S., and E.J. McCluskey, "Testability of Parity Checkers," *IEEE Trans. on Industrial Electronics*, Vol. 36, No. 2, pp. 254-262, May 1989. (ONR, NSF)
- [Wang 89] Wang, L.-T., and S. Mourad, "SST: Scan self-test for sequential machines," *IEE Proceedings-E Computers and Digital Techniques*, Vol. 136, pt. E, No. 6, pp. 569-574, Nov. 1989. United Kingdom. (NSF)

Accepted

- Saxena, N.R., and E.J. McCluskey, "Analysis of Checksums, Extended-Precision Checksums and Cyclic Redundancy Checks," *IEEE Trans. Comput.* (NSF, ONR, HP)
- Saxena, N.R., and E.J. McCluskey, "Control-Flow Checking Using Watchdog Assists and Extended-Precision Checksums," *IEEE Trans. Comput.* (NSF, ONR, HP)

CONFERENCE PAPERS

Published

- [Makar 89] Makar, S., and E.J. McCluskey, "The Critical Path for Multiple Faults," *1989 IEEE Int. Conf. on Computer-Aided Design*, Santa Clara, CA, pp. 162-165, Nov. 6-9, 1989. (ONR, NSF)(CRC TR 89-3)
- [Millman 89] Millman, S.D., and E.J. McCluskey, "Detecting Stuck-Open Faults with Stuck-At Test Sets," *IEEE Custom Integrated Circuits Conference*, San Diego, CA, May 15-18, 1989.(ONR)(CRC TR 89-2)
- [Mourad 89] Mourad, S., and E.J. McCluskey, "Fault Analysis Using Signature Analyzers," *1989 International Conference on Circuits and Systems*, Nanjing, China, July 6-9, 1989.(CRC TR 89-3)
- [Saxena 89] Saxena, N., and E.J. McCluskey, "Control-Flow Checking Using Watchdog Assists and Extended-Precision Checksums," *Dig. 19th Annu. Int. Symp. Fault-Tolerant Comput. (FTCS-19)*, Chicago, IL, pp. 428-435, June 21-23, 1989.(CRC TR 89-2)
- [Saxena 89] Saxena, N., and E.J. McCluskey, "Arithmetic and Galois Checksums," *1989 IEEE Int. Conf. on Computer-Aided Design*, Santa Clara, CA, pp. 570-573, Nov. 6-9, 1989. (ONR, NSF)(CRC TR 89-3)
- [Udell 89] Udell, J., and E.J. McCluskey, "Pseudoexhaustive Test and Segmentation; Formal Definitions and Extended Fault Coverage Results," *Dig. 19th Annu. Int. Symp. Fault-Tolerant Comput. (FTCS 19)*, Chicago, IL, pp. 292-298, June 21-23, 1989.(CRC TR 89-2)
- [Wang 89] Wang, L.-T., M. Marhofer, and E.J. McCluskey, "A Self-Test and Self-Diagnosis Architecture for Boards Using Boundary Scans," *European Test Conference*, Paris, France, pp. 119-126, April 12-14, 1989.(NSF & FRG)(CRC TR 89-2)

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- Avra, L., and E.J. McCluskey, "Behavioral Synthesis of Testable Systems with VHDL," *COMPCON Spring '90*, San Francisco, CA, Feb. 26 - Mar. 2, 1990. (DEC, ONR, NSF)(CRC TR 89-10)

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- (CRC TR 89-0) Munda, S. V., "Bibliography of 1988 CRC Publications," Feb. 1989. (NSF & ONR)
- (CRC TR 89-1) Udell, J.G. Jr., "Pseudo-Exhaustive Testing of Digital Integrated Circuits," Apr. 1989. (NSF, ONR, Tektronix)
- (CRC TR 89-2) Center for Reliable Computing Staff, "Preprints of the Custom Integrated Circuits Conference, San Diego, CA, May 15-18, 1989, 1st European Test Conference, Paris France, Apr. 11-14, 1989, and the Fault-Tolerant Computing Symposium-19, Chicago, IL, Jun. 21-23, 1989." (NSF, ONR, Tektronix, FRG)
- Millman, S.D., and E.J. McCluskey, "Detecting Stuck-Open Faults with Stuck-At Test Sets," CICC'89.
- Saxena, N.R., and E.J. McCluskey, "Control-Flow Checking Using Watchdog Assists and Extended-Precision Checksums," FTCS 19.
- Udell, J.G. Jr., and E.J. McCluskey, "Pseudo-Exhaustive Test and Segmentation: Formal Definitions and Extended Fault Coverage Results," FTCS 19
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- Makar, S., and E.J. McCluskey, "The Critical Path for Multiple Faults," ICCAD'89.
- Mourad, S., and E.J. McCluskey, "Fault Analysis Using Signature Analyzers," 1989 International Conference on Circuits and Systems.
- Saxena, N.R., and E.J. McCluskey, "Arithmetic and Galois Checksums," ICCAD'89.
- (CRC TR 89-4) Hao, H., and E.J. McCluskey, "Survey of Combinational Shifter Implementations," Oct. 1989.(ONR, NSF)
- (CRC TR 89-5) Millman, S.D., and E.J. McCluskey, "Detecting Stuck-Open Faults with Stuck-At Test Sets," Dec. 89.(ONR, NSF)
- (CRC TR 89-6) Millman, S.D., and E.J. McCluskey, "Bridging, Transition, and Stuck-Open Faults in Self-Testing CMOS Checkers," Dec. 89.(ONR, NSF)
- (CRC TR 89-7) Millman, S.D., and E.J. McCluskey, "Pseudorandom Test for Bridging Faults," Dec. 89.(ONR, NSF)
- (CRC TR 89-8) Millman, S.D., J.M. Acken, and E.J. McCluskey, "Diagnosing CMOS Bridging Faults with Stuck-At Fault Dictionaries," Dec. 89.(ONR, NSF)
- (CRC TR 89-9) Millman, S., "Nonclassical Faults in CMOS Digital Integrated Circuits," Dec. 89. (ONR, NSF)
- (CRC TR 89-10) "Preprint of *COMPCON Spring '90*," San Francisco, CA, Feb. 26 - Mar. 2, 1990. (DEC, ONR, NSF)
- Avra, L., and E.J. McCluskey, "Behavioral Synthesis of Testable Systems with VHDL,"

PRESENTATIONS

- McCluskey, E.J., "Testing Requirements, Fault Models, Required Fault Coverage," *Tutorial at COMPCON Spring '89*, Stanford University, Feb. 25, 1989.
- McCluskey, E.J., "Testability Measures, Ad Hoc, SFT, Scan, BIST," *COMPCON Spring '89*, Stanford University, Feb. 25, 1989.
- McCluskey, E.J., L.-T. Wang, M. Marhoefer, "A Self-Test and Self-Diagnosis Architecture for Boards Using Boundary Scans," *Built-In Self-Test Workshop*, Charleston, SC, Mar. 29-31, 1989.
- McCluskey, E.J., "Design for Testability - Why and How," Sun Microsystems, Mt. View, CA, Mar. 23, 1989.
- McCluskey, E.J., "Digital Test Principles," *Tutorial, International Test Conference 1989*, Washington, DC, Aug. 28-31, 1989.
- Mourad, S., "Statistical Evaluation, Automatic Test Pattern Generation," *Tutorial at COMPCON Spring '89*, Stanford University, Feb. 25, 1989.

1989 VISITORS

- Rene Micolet, CEA-IRDI, Leti Division, France, Jan. 1989
- Dr. Shanker Singh, IBM, Tucson, AZ. Jan. 1989
- Charles Rosenthal, Mentor Graphics, Beaverton, OR, Feb. 1989
- David Giramma, Mentor Graphics, Beaverton, OR, Feb. 1989
- Kiyoshi Emi, NEC Corporation, Minato-Ku, Tokyo, Japan, Mar. 1989
- Xavier Flinois, Schlumberger Technologies, San Jose, CA, Mar. 1989
- Johan Karlsson, Chalmers University of Technology, Göteborg, Sweden, Aug. 1989
- Ulf Gunneflo, Chalmers University of Technology, Göteborg, Sweden, Aug. 1989

1989 SCHOLARS VISITING CRC

- Toyokazu Tatsuta, Hitachi, Ltd. Yokohama, Japan
- Katsunobu Muroi, Mitsubishi Electric Corporation, Kanagawa Prefecture 247, Japan
- Hideho Yamamura, Hitachi, Ltd., Yokohama, Japan
- Tomoo Fukazawa, NTT Laboratories, Kanagawa Prefecture, Japan
- Hisashi Yamauchi, NEC Corporation, Kanagawa Prefecture, Japan

CRC PhDs GRANTED

- S. Millman, "Nonclassical Faults in CMOS Digital Integrated Circuits," 1989. (CRC)

TECHNICAL FACILITIES CENTER FOR RELIABLE COMPUTING

Apple Macintosh Personal Computers: Four Macintosh personal computers, each with 1M internal memory and two disk drives. An Appletalk network connects the Macs to an Apple Laserwriter printer.

IBM Personal Computers: IBM PC-AT personal computer with enhanced graphics board, high-resolution color monitor, hard disk, and printer. Includes ViewLogic software for schematic capture, simulation, waveform analysis, and fault grading. IBM PC-RT reduced instruction set personal computer with high resolution color monitor, hard disk, streaming tape drive, and Ethernet capability.

VAX Computers: MicroVAX GPX II running VMS with 70M and 140M hard disks and 13M main memory. Ethernet capability. Access to a VAX 780 running Unix #WF70608 780. Vaxstation 2000 running VMS with 40M and 70M hard disks.

Laboratory Oven: AES Model ZCK-9204 laboratory oven to be used for accelerated life testing and burn-in.

Sun 3/140 work station running Unix, with two 64M hard disks, 8M main memory and streaming tape drive. Ethernet capability #708ES613.

Delni-aa ethernet multiplexer and a transceiver providing access to the ethernet for the Microvax, Sun, TEK 4317, and PC-RT. Capability to extend access to four more workstations.

Tektronix Lab Instruments: MHz function generator, 40 MHz function generator - very fancy, 2 Triple power supplies, 2 Digital Multimeters, 5 Coax cables for connecting FGs to boards, 2 Mainframes to hold one each of PS, DM, and FG.

Tektronix Design Analysis System (DAS 9200): Motorola 68010-based test system with 2M memory, 20M hard disk, and color display. Equipped with a 32-channel 50 MHz pattern generation card, two 16-channel 200MHz data acquisition cards, 92 DV device verification software, and TF 100 test fixture.

DAS9200: 1 Tester mainframe, keyboard and monitor. 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes. 36 Channel 50MHZ sequence pattern generator.

DAS9252: 1 Tester mainframe, keyboard and monitor. Includes board and accompanying flying lead set for microprocessor testing (90 channels), 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes, 18-channel 50 MHz pattern generator, Test fixture, 21x21 pin grid array fixture to fit TF100

1241BNO-1B: 1 Color logic analyzer mainframe, 2 18-channel cards, 1 9-channel card, 5 P6460 probes, performance analysis ROM pack, 64K RAM pack, parallel printer COMM pack, printer support ROM pack

2467: 1350 MHz four channel portable oscilloscope with word recognizer.

4317: 1 Color graphics workstation running Utek (Tektronix Unix) with 60M and 35M hard drives, and 4M main memory. Ethernet capability.

4696: 1Color ink-jet printer.

TECHNICAL FACILITIES SOFTWARE SYSTEMS

The lab houses 7 digital testing Systems: Teradyne, EDA's Laser, Genrad's HILO, HHB's CADAT and Intelligen, and Gateway's Verilog.

Lasar: This VMS-based system is hosted on a MicroVAX and consists of logic and fault simulators, and ATPG for both combinational and sequential circuits. The system includes large model libraries.

Hilo: GenRad's Hilo comprises logic and fault simulators and a test pattern generation.

CADAT 6.1: CADAT is a logic and fault simulator that is suitable for combinational and sequential circuits. Intelligen is a sequential test pattern generator.

Verilog: Hardware description language and simulator.

Viewlogic: This is a schematic capture and a logic simulator that is also capable of injecting some faults in the design. The system is mainly used for logic design courses. The version hosted on the Vaxstation also has the capacity to simulate VHDL behavioral models.

Spice: Spice systems for analog simulation of devices and circuits: tSpice is hosted on the Tektronix and pSpice on the IBM AT.