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by S.V. Munda

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CENTER FOR RELIABLE COMPUTING
Computer Systems Laboratory
Depts. of Electrical Engineering and Computer Science
Stanford University
Stanford, CA 94305-4055 USA

ABSTRACT

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Published

[McCluskey 90] McCluskey, E.J., "Design Techniques for Testable Embedded Error Checkers," *Special Issue on Fault-Tolerant Systems, Computer,* pp. 84-88, July 1990. (NSF, ONR)

[Saxena 90] Saxena, N.R., and E.J. McCluskey, "Control-Flow Checking Using Watchdog Assists and Extended-Precision Checksums," *IEEE Trans. Comput.,* Vol. 39, No. 4, pp. 554-559, April 1990. (NSF, ONR, HP)

[Saxena 90] Saxena, N.R., and E.J. McCluskey, "Analysis of Checksums, Extended-Precision Checksums and Cyclic Redundancy Checks," *IEEE Trans. Comput.,* Vol. 39, No. 7, pp. 969-975, July 1990. (NSF, ONR, HP)

CONFERENCE PAPERS

Published

[Avra 90] Avra, L., and E.J. McCluskey, "Behavioral Synthesis of Testable Systems with VHDL," *COMPCON Spring '90,* San Francisco, CA, pp. 410-415, Feb. 26 - Mar. 2, 1990. (DEC, ONR, NSF)(CRC TR 89-10)

[McCluskey 90] McCluskey, E.J., "Half a century of Logic Synthesis," *EURO ASIC 90,* Paris, France, May 29-31, 1990. (ONR, NSF)

[McCluskey 90] McCluskey, E.J., "Design for Test Overview," *Microelectronic System Education Conference & Exposition,* San Jose, CA , July 29 - August 1, 1990. (ONR, NSF)

[Millman 90] Millman, S.D., E.J. McCluskey, and J.M. Acken, "Diagnosing CMOS Bridging Faults with Stuck-At Fault Dictionaries," *Proc. 1990 Int. Test Conf.,* Washington, DC, pp. 860-870, Sep. 10-12, 1990. (ONR, NSF)

[Norman 90] Norman, R.H., and E.J. McCluskey, "Design for Integrity," *Advanced Microelectronics Technology Qualification, Reliability and Logistics Workshop,* San Diego, CA, Aug. 28-30, 1990. (ONR, NSF)

[Saxena 90] Saxena, N.R., and E.J. McCluskey, "Bounds on Aliasing Probabilities under Bernoulli Error Model for Signature Analysis," *Proc. 1990 Int. Test Conf., Poster Session,* Washington, DC, Sep. 10-12, 1990. (HP, ONR, NSF)

Accepted

[McCluskey 91] McCluskey, E.J., "Who Needs Design for Testability?," *Dig. 1991 IEEE Int. Solid-State Circuits Conf.,* San Francisco, Feb. 13-17, 1991.

BOOK CONTRIBUTIONS

[McCluskey 90] McCluskey, E.J.,"Foreword" in *Structured Logic Testing,* Prentice-Hall Inc., Englewood Cliffs, NJ, 1990.

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McCluskey, E.J., "Logic Design," *The Encyclopedia of Computer Science and Engineering, Third Ed.,* 1991. (ONR & NSF)

McCluskey, E.J., "Switching Theory," *The Encyclopedia of Computer Science and Engineering, Third Ed.,* 1991. (ONR & NSF)

CRC TECHNICAL REPORTS

(CRC TR 90-0) Munda, S. V., "Bibliography of 1989 CRC Publications," Feb. 1990. (NSF & ONR)

(CRC TR 90-1) Yamamura, H., and E.J. McCluskey, "Fault Analysis of ECL Gates with Device Defects using SPICE," March 1990. (NSF, ONR & Hitachi, Ltd.)

(CRC TR 90-2) Avra, L., and E.J. McCluskey, "On the Behavioral Synthesis of Testable Systems with VHDL," May 1990. (DEC, NSF & ONR)

(CRC TR 90-3) Makar, S.R., and E.J. McCluskey, "Minimal Single Stuck-at Tests For Multiplexers," June 1990. (DEC, NSF & ONR)

(CRC TR 90-4) "Preprint of a paper from the *IFIP Working Conference on Logic and Architecture Synthesis*," Paris, France, May 31-June 1, 1990. (ONR & NSF)
McCluskey, E.J., "Half a Century of Logic Synthesis, (The First Two Decades, Anyway)".

(CRC TR 90-5) Fukazawa, T., and E.J. McCluskey, "Assertions for Dynamic Error Detection on a Parallel Processor," November 1990. (NTT, ONR & NSF)

(CRC TR 90-6) Yamamura, H., "A Scheme to Detect Non-Functional Faults in ECL Circuits," November 1990. (NSF, ONR & Hitachi, Ltd.)

(CRC TR 90-7) Makar, S.R., and E.J. McCluskey, "Implementing Fault Models in Verilog," November 1990. (NSF & ONR)

(CRC TR 90-8) "Preprint of a paper from the *Dig. 1991 IEEE Int. Solid-State Circuits Conf.*," San Francisco, CA, Feb. 13-17, 1991. (ONR & NSF)
McCluskey, E.J., "Who Needs Design-For-Testability".

(CRC TR 90-9) Avra, L., "Allocation and Assignment in High-Level Synthesis for Self-Testable Data Paths," December 1990. (DEC, ONR & NSF)

(CRC TR 90-10) Yamauchi, H., "Mixed Level and High Level ATPG," December 1990. (NEC, ONR & NSF)

(CRC TR 90-11) Saxena, N.R., E.J. McCluskey, and P. Franco, "Bounds on Signature Analysis Aliasing for Random Testing," December 1990. (HP, ONR & NSF)

OTHER TECHNICAL REPORTS

(Numerical Analysis Project, Manuscript NA-89-12) Boley, D., G.H. Golub, S. Makar, N. Saxena, and E.J. McCluskey, "Backward Error Assertions for Checking Solutions to Systems of Linear Equations," Nov. 1989.

PRESENTATIONS

McCluskey, E.J., "Pseudo-exhaustive Testing and why synthesis should account for multifaults," *NSF-DARPA Synthesis Workshop,* Boulder, CO, Jan. 26-29, 1990.
McCluskey, E.J., "Reliable Advanced Electronic Systems," *SDI/IST/ONR Reliable Advanced Electronic Systems Program*, Stanford University, Stanford, CA, July 12-14, 1990.
McCluskey, E.J., "Boundary Scan," *Cirrus Logic*, Milpitas, CA, Sep. 25, 1990
McCluskey, E.J., "Signature Analysis Design," *Coordinated Science Lab Seminar,* University of Illinois, Oct. 30, 1990.

AWARDS

McCluskey, E.J., "Annual Award for Outstanding Contributions to Computer Science Education, Curriculum 68 Committee," *21st SIGCSE Technical Symposium,* Washington, DC, Feb. 22-23, 1990
McCluskey, E.J., "EURO ASIC 90 Prize for Fundamental Outstanding Contribution to Logic Synthesis," *EURO ASIC 90,* Paris, France, May 29-31, 1990

1990 VISITORS

Prof. Vyacheslav N. Yarmolik, Minsk Radioengineering Institute Candidate of Sciences, USSR, Jan. 1990
Dr. Isaak Veystman, Jan. 1990
Ken Parker, Hewlett-Packard Company, Loveland, CO, Mar. 1990
Victor Grimblatt, VLSI Technology, Sophia-Antipolis, June 1990
Roger L. Howell, McGraw Hill, Watsonville, CA, July 1990
Shigeo Aono, Nissan Motor Co., Ltd., Kanagawa, Japan, Oct. 1990
Norio Fujiki, Nissan Motor Co., Ltd., Kanagawa, Japan, Oct. 1990
Yoshitaka Hata, Nissan Motor Co., Ltd., Kanagawa, Japan, Oct. 1990
Prof. Prith Banerjee, University of Illinois at Urbana-Champaign, Nov. 1990
Prof. Sudkahar M. Reddy, University of Iowa, Nov. 1990
Prof. Yong Deak Kim, Ajou University, Suwon, Korea, Nov. 1990
Prof. Gabrielle Saucier, Institut National Polytechnic de Grenoble, France, Nov. 1990
Prof. Jacob Savir, IBM, Poughkeepsie, NY, Nov. 1990
Dr. Tushar Gheewala, CrossCheck Technology Inc., San Jose, CA, Dec. 1990
Dr. Ken Parker, Hewlett Packard, Loveland, CO, Dec. 1990

1990 SCHOLARS VISITING CRC

Mr. Hideho Yamamura, Hitachi, Ltd., Yokohama, Japan
Dr. Tomoo Fukazawa, NTT Laboratories, Kanagawa Prefecture, Japan
Mr. Hisashi Yamauchi, NEC Corporation, Kanagawa Prefecture, Japan
Prof. Hiroshi Masuyama, Miyazaki University, Miyazaki, Japan
Prof. Kiyoshi Furuya, Chuo University, Tokyo, Japan
Dr. Francoise Matrinolle, INSA, France

TECHNICAL FACILITIES
CENTER FOR RELIABLE COMPUTING

Apple II Personal Computer: One Apple II personal computer.

Apple Macintosh Personal Computers: One Mac IIcx with 1 Meg memory and 40 Meg hard disk, one Mac SE30 with 1 Meg memory and 40 Meg hard disk, one Mac SE with 2 Meg memory and 20 Meg hard disk, and one Mac SE with 1 meg memory and 20 Meg hard disk. An Appletalk network connects the Macs to an Apple Laserwriter IINT printer.

IBM Personal Computers: IBM PC-AT personal computer with enhanced graphics board, high-resolution color monitor, hard disk, and printer. Includes ViewLogic software for schematic capture, simulation, waveform analysis, and fault grading. IBM PC-RT reduced instruction set personal computer with high resolution color monitor, hard disk, streaming tape drive, and Ethernet capability.

VAX Computers: MicroVAX GPX II running VMS with 70MB and 140MB hard disks and 13M main memory. Ethernet capability . Access to a VAX 780 running Unix #WF70608 780. Vaxstation 2000 running VMS with 40MB and 70MB hard disks.

Laboratory Oven: AES Model ZCK-9204 laboratory oven to be used for accelerated life testing and burn-in.

Sun 3/140 work station running Unix, with two 64MB hard disks, 8M main memory and streaming tape drive. Ethernet capability #708ES613.

Delni-aa ethernet multiplexer and a transceiver providing access to the ethernet for the Microvax, Sun, TEK 4317, and PC-RT. Capability to extend access to four more workstations.

Tektronix Lab Instruments: MHz function generator, 40 MHz function generator - very fancy, 2 Triple power supplies, 2 Digital Multimeters, 5 Coax cables for connecting FGs to boards, 2 Mainframes to hold one each of PS, DM, and FG.

Tektronix Design Analysis System (DAS 9200): Motorola 68010-based test system with 2MB memory, 20MB hard disk, and color display. Equipped with a 32-channel 50 MHz pattern generation card, two 16-channel 200MHz data acquisition cards, 92 DV device verification software, and TF 100 test fixture.

DAS9200: 1 Tester mainframe, keyboard and monitor. 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes. 36 Channel 50MHZ sequence pattern generator.

DAS9252: 1 Tester mainframe, keyboard and monitor. Includes board and accompanying flying lead set for microprocessor testing (90 channels), 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes, 18-channel 50 MHz pattern generator, Test fixture, 21x21 pin grid array fixture to fit TF100

1241BNO-1B: 1 Color logic analyzer mainframe, 2 18-channel cards, 1 9-channel card, 5 P6460 probes, performance analysis ROM pack, 64K RAM pack, parallel printer COMM pack, printer support ROM pack

Tektronix 2467: 1350 MHz four channel portable oscilloscope with word recognizer.

Tektronix 4317: 1 Color graphics workstation running UTek (Tektronix Unix) with 60MB and 35MB hard drives, and 4MB main memory. Ethernet capability.

Tektronix 4696: 1Color ink-jet printer.

Sony NWS-1930: News workstation running UNIX BSD4.3 with 16 MBytes of memory and two 256 MB-hard drives.

Sun Sparcstation SLC: Running Unix, with 389MB Fujitsu hard disk, and 8MB main memory.

TECHNICAL FACILITIES
SOFTWARE SYSTEMS

The lab houses 7 digital testing Systems: Teradyne, EDA's Lasar, Genrad's HILO, HHB's CADAT and Intelligen, Cadence's Verilog, and VHDL design and simulation tools from Vantage and Viewlogic.

Lasar: This VMS-based system is hosted on a MicroVAX and consists of logic and fault simulators, and ATPG for both combinational and sequential circuits. The system includes large model libraries.

Hilo: GenRad's Hilo comprises logic and fault simulators and a test pattern generation.

CADAT 6.1: CADAT is a logic and fault simulator that is suitable for combinational and sequential circuits. Intelligen is a sequential test pattern generator.

Vantage: VHDL simulator and intermediate format access tools.

Verilog, Verifault: Hardware description language and simulator, and fault simulator.

Viewlogic: This is a schematic capture and a logic simulator that is also capable of injecting some faults in the design. The system is mainly used for logic design courses. The version hosted on the Vaxstation also has the capacity to simulate VHDL behavioral models.

Spice: Spice systems for analog simulation of devices and circuits: tSpice is hosted on the Tektronix and pSpice on the IBM AT.