

## **1992 CRC ACTIVITIES**

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CRC Technical Report No. 93-0

(CSL TN No. 93-391)

January 1993

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### **ABSTRACT**

This report lists the 1992 CRC Activities.

This report was supported in part by the Innovative Science and Technology Office of the Strategic Defense Initiative Organization and administered through the Office of Naval Research under Contract No. N0001492-J-1782, and in part by the National Science Foundation under Grant No. MIP-9107760.

## TABLE OF CONTENTS

LIST OF PUBLICATIONS.....	3
JOURNAL PAPERS .....	3
CONFERENCE PAPERS .....	4
BOOK CONTRIBUTIONS.....	4
CRC TECHNICAL REPORTS .....	4
PRESENTATIONS.....	5
AWARDS .....	5
1992 VISITORS.....	5
1992 VISITING SCHOLARS.....	5
TECHNICAL FACILITIES .....	6

## LIST OF PUBLICATIONS

### JOURNAL PAPERS

#### Published

- [Furuya 92] Furuya, K., and E.J. McCluskey, "A Method and the Effect of Shuffling Compactor Inputs in VLSI Self-Testing," *Special Issue on PRFTS, Trans. on Information and Systems of IEICE*, pp. 842-846, Nov. 1992.
- [Saxena 92] Saxena, N.R., P. Franco, and E.J. McCluskey, "Simple Bounds on Signature Analysis Aliasing for Random Testing," *Special Issue on Fault-Tolerant Computing, IEEE Trans. Comput.*, pp. 638-645, May 1992. (ONR, NSF, HP)

#### Accepted

- [Hao 92] Hao, H., and E.J. McCluskey, "Analysis of Gate Oxide Shorts in CMOS Circuits," *IEEE Trans. Comput.* (ONR, NSF)
- [Saxena 92] Saxena, N.R. and E.J. McCluskey, "Linear Complexity Assertions for Sorting Algorithms," *IEEE Trans. Software Eng.* (HP, ONR, NSF)

#### Submitted

- [Furuya 92] Furuya, K., and E.J. McCluskey, "Two-Pattern Test Capabilities of Autonomous TPG Circuits," *Trans. on Information and Systems of IEICE*, 1993.

## CONFERENCE PAPERS

### Published

- [Avra 92] Avra, L., "Orthogonal Built-In Self-Test," *COMPCON Spring '92*, San Francisco, CA, pp. 452-457, Feb. 24-28, 1992. (DEC, ONR, NSF)
- [Furuya 92] Furuya, K., S. Seki, and E.J. McCluskey, "Synthesis of Autonomous TPG Circuits Oriented for Two-Pattern Testing," *1<sup>st</sup> Asian Test Symposium*, Hiroshima, Japan, pp. 235-240, Nov. 26-27, 1992.
- [Ma 92] Ma, S., and E.J. McCluskey, "Non-Conventional Faults in BiCMOS Digital Circuits," *Proc. 1992 Int. Test Conf.*, Baltimore, MD, pp. 882-891, Sep. 20-24, 1992. (ONR, NSF)

## BOOK CONTRIBUTIONS

### Accepted

- McCluskey, E.J., "Logic Design," *Reference Data for Engineers: Radio, Electronics, Computer, and Communications*, 8th Ed., Chapter 43, Howard W. Sams & Co., Inc., Indianapolis, 1993. (ONR, NSF)
- McCluskey, E.J., "Logic Design," *Encyclopedia of Computer Science and Engineering*, 3rd Ed., Van Nostrand Reinhold, New York, 1993. (ONR & NSF)
- McCluskey, E.J., "Switching Theory," *Encyclopedia of Computer Science and Engineering*, 3rd Ed., Van Nostrand Reinhold, New York, 1993. (ONR & NSF)

## CRC TECHNICAL REPORTS

- (CRC TR 92-0) Munda, S.V., "Bibliography 1991 CRC Activities," Jan. 1992. (NSF, ONR)
- (CRC TR 92-1) Hao, H., and E.J. McCluskey, "Analysis of Gate Oxide Shorts in CMOS Circuits," Jan. 1992. (NSF, ONR)
- (CRC TR 92-2) "Preprint of a paper from the 1992 International Test Conference," Baltimore, MD, Sep. 20-24, 1992. (NSF, ONR)
- Ma, S., and E.J. McCluskey, "Non-Conventional Faults in BiCMOS Digital Circuits."
- (CRC TR 92-3) Touba, N., "Reducing Synchronization in Concurrent Behavioral Descriptions," Aug. 1992. (NSF, ONR)

## **PRESENTATIONS**

- McCluskey, E.J., "Why Computers Fail or Who Needs Design-for-Testability?"  
*Departments of Computer Science and Electrical and Computer Engineering, University of Arizona, Mar. 26, 1992.*
- McCluskey, E.J., "Who Needs Design-for-Testability?" *Systems Day on Campus, Stanford Computer Forum, Stanford University, June 11, 1992.*
- McCluskey, E.J., "An Experiment to Evaluate Test Techniques," *CRHC Special Lecture Series, University of Illinois, Sep. 17, 1992.*

## **AWARDS**

- McCluskey, E.J., "1991 Taylor L. Booth Education Award," *ITC92, Baltimore, MD, Sep. 20-24, 1992.*

## **1992 VISITORS**

- Prof. Ray Mercer, University of Texas at Austin, Jan. 1992  
Prof. Takashi Nanya, Tokyo Institute of Technology, Japan, Mar. 1992  
Dr. Niraj Jha, Princeton University, May 1992

## **1992 VISITING SCHOLARS**

- Mr. Yukio Koguchi, Hitachi, Ltd., Japan  
Prof. Han Seok-Bung, Gyeonsang National University, Korea  
Prof. Jacob Abraham, University of Texas at Austin, Austin, TX  
Prof. Florinel Balteanu, University of Pitesti, Romania

## TECHNICAL FACILITIES CENTER FOR RELIABLE COMPUTING

### TEST EQUIPMENT:

**Laboratory Oven:** AES Model ZCK-9204 laboratory oven to be used for accelerated life testing and burn-in.

**Tektronix Lab Instruments:** MHz function generator, 40 MHz function generator - very fancy, 2 Triple power supplies, 2 Digital Multimeters, 5 Coax cables for connecting FGs to boards, 2 Mainframes to hold one each of PS, DM, and FG.

**Tektronix Design Analysis System (DAS 9200):** Motorola 68010-based test system with 2MB memory, 20MB hard disk, and color display. Equipped with a 32-channel 50 MHz pattern generation card, two 16-channel 200MHz data acquisition cards, 92 DV device verification software, and TF 100 test fixture.

**DAS9200:** 1 Tester mainframe, keyboard and monitor. 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes. 36 Channel 50MHZ sequence pattern generator.

**DAS9252:** 1 Tester mainframe, keyboard and monitor. Includes board and accompanying flying lead set for microprocessor testing (90 channels), 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes, 18-channel 50 MHz pattern generator, Test fixture, 21x21 pin grid array fixture to fit TF100

**1241BNO-1B:** 1 Color logic analyzer mainframe, 2 18-channel cards, 1 9-channel card, 5 P6460 probes, performance analysis ROM pack, 64K RAM pack, parallel printer COMM pack, printer support ROM pack

**Tektronix 2467:** 1350 MHz four channel portable oscilloscope with word recognizer.

**Tektronix 4696:** 1Color ink-jet printer.

### WORKSTATIONS:

**Sun Sparcstation SLC:** Running Unix, with 389MB Fujitsu hard disk, and 8MB main memory.

**Sun 3/140 work station** running Unix, with two 64MB hard disks, 8M main memory and QIC-24 tape drive. Ethernet capability #708ES613.

**Sony NWS-1930:** News workstation running UNIX BSD4.3 with 16 MBytes of memory, two 256 MB-hard drives, QIC-120 tape drive, and 3.5" floppy disk drive.

**IBM PC-RT** reduced instruction set personal computer with high resolution color monitor, hard disk, streaming tape drive, and Ethernet capability.

**Tektronix 4317:** 1 Color graphics workstation running UTek (Tektronix Unix) with 60MB and 35MB hard drives, and 4MB main memory. Ethernet capability.

**VAX Computers:** MicroVAX GPX II running VMS with 70MB and 140MB hard disks and 13M main memory. Ethernet capability . Access to a VAX 780 running Unix #WF70608 780. VAXstation 2000 running VMS with 40MB and 70MB hard disks.

**Delni-aa ethernet** multiplexer and a transceiver providing access to the ethernet for the MicroVAX, Sun, TEK 4317, and PC-RT. Capability to extend access to four more workstations.

## PERSONAL COMPUTERS:

**Apple Macintosh Personal Computers:** One Mac IIcx with 5 Meg memory and 40 Meg hard disk, one Mac SE30 with 5 Meg memory and 40 Meg hard disk, one Mac SE with 4 Meg memory and 20 Meg hard disk, and one Mac SE with 1 Meg memory and 20 Meg hard disk. An Appletalk network connects the Macs to an Apple Laserwriter IINT printer.

**IBM Personal Computers:** IBM PC-AT personal computer with enhanced graphics board, high-resolution color monitor, hard disk, and printer. Includes ViewLogic software for schematic capture, simulation, waveform analysis, and fault grading.

## TECHNICAL FACILITIES SOFTWARE SYSTEMS

The lab houses 8 digital testing Systems: Teradyne, EDA's Lasar, Genrad's HILO, HHB's CADAT and Intelligen, Cadence's Verilog and Verifault, VHDL design and simulation tools from Vantage and Viewlogic, and Picasso.

**CADAT 6.1:** CADAT is a logic and fault simulator that is suitable for combinational and sequential circuits. Intelligen is a sequential test pattern generator.

**Hilo:** GenRad's Hilo comprises logic and fault simulators and a test pattern generation.

**Lasar:** This VMS-based system is hosted on a MicroVAX and consists of logic and fault simulators, and ATPG for both combinational and sequential circuits. The system includes large model libraries.

**Picasso:** A complete gate level sequential test pattern generation, logic and fault simulation system for VLSI designs.

**Spice:** Spice systems for analog simulation of devices and circuits: tSpice is hosted on the Tektronix and pSpice on the IBM AT.

**Vantage:** VHDL simulator and intermediate format access tools.

**Verilog, Verifault:** Hardware description language and simulator, and fault simulator.

**Viewlogic:** This is a schematic capture and a logic simulator that is also capable of injecting some faults in the design. The system is mainly used for logic design courses. The version hosted on the VAXstation also has the capacity to simulate VHDL behavioral models.