1993 CRC ACTIVITIES

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ABSTRACT

This report lists the 1993 CRC Activities.

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LIST OF PUBLICATIONS

JOURNAL PAPERS

Published

[Hao 93] Hao, H., and E.J. McCluskey, "Analysis of Gate Oxide Shorts in CMOS Circuits," *IEEE Trans. Comput.,* Vol. 42, No. 12, pp. 1510-1516, Dec. 1993. (ONR, NSF)

[Furuya 93] Furuya, K., and E.J. McCluskey, "Two-Pattern Test Capabilities of Autonomous TPG Circuits," *Trans. on Information and Systems of IEICE*, Vol. E76-D, No. 7, pp. 800-808, July 1993.

Accepted

[Saxena 94] Saxena, N.R. and E.J. McCluskey, "Linear Complexity Assertions for Sorting Algorithms," *IEEE Trans. Software Eng*. (HP, ONR, NSF)

Submitted

[Boley 94] Boley, D., G.H. Golub, S. Makar, N. Saxena, and E.J. McCluskey, "Floating Point Fault-Tolerance with Backward Error Assertions," *IEEE Trans. Comput., Special Issue on Fault-Tolerant Computing.*

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CONFERENCE PAPERS

Published

[Avra 93] Avra, L.J., and E.J. McCluskey, "Synthesizing for Scan Dependence in Built-In Self-Testable Designs," *Proc. 1993 Int. Test Conf.*, Baltimore, MD, pp. 734-743, Oct. 17-21, 1993. (ONR, NSF)

[Hao 93] Hao, H., and E.J. McCluskey, "Very-Low-Voltage Testing for Weak CMOS Logic IC's," *Proc. 1993 Int. Test Conf.*, Baltimore, MD, pp. 275-284, Oct. 17-21, 1993. (ONR, NSF)

[McCluskey 93] McCluskey, E.J., "Quality and Single-Stuck Faults," *Proc. 1993 Int. Test Conf.*, Baltimore, MD, p. 597, Oct. 17-21, 1993. (ONR, NSF)

Accepted

[Franco 94] Franco, P., and E.J. McCluskey, "On Line Delay Testing of Digital Circuits," *12th IEEE VLSI Test Symposium*, Cherry Hill, NJ, Apr. 25-28, 1994. (ONR, NSF)

[Franco 94] Franco, P., and E.J. McCluskey, "3-Pattern Delay Fault Tests," *12th IEEE VLSI Test Symposium*, Cherry Hill, NJ, Apr. 25-28, 1994. (ONR, NSF)

[Ma 94] Ma, S., and E.J. McCluskey, "Open Faults in BiCMOS Gates," *12th IEEE VLSI Test Symposium*, Cherry Hill, NJ, Apr. 25-28, 1994. (ONR, NSF)

BOOK CONTRIBUTIONS

Published

McCluskey, E.J., "Logic Design," in *Reference Data for Engineers: Radio, Electronics, Computer, and Communications*, 8th Ed., Chapter 43, Van Valkenburg, ed., Howard W. Sams & Co., Inc., Indianapolis, 1993. (ONR, NSF)

McCluskey, E.J., "Logic Design," in *Encyclopedia of Computer Science and Engineering*, 3rd Ed., Anthony Ralston and Edwin D. Reilly, eds., Van Nostrand Reinhold, New York, pp. 775-778, 1993. (ONR & NSF)

McCluskey, E.J., "Switching Theory," in *Encyclopedia of Computer Science and Engineering*, 3rd Ed., Anthony Ralston and Edwin D. Reilly, eds., Van Nostrand Reinhold, New York, pp. 1332-1336, 1993. (ONR & NSF)

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CRC TECHNICAL REPORTS

(CRC TR 93-0) Munda, S.V., "Bibliography 1992 CRC Activities," Jan. 1993. (NSF, ONR)

(CRC TR 93-1) Hao, H., and E.J. McCluskey, “Very-Low-Voltage Testing for Weak CMOS Logic IC’s,” Apr. 1993. (NSF, ONR)

(CRC TR 93-2) “Preprint of papers accepted for presentation at the 1993 International Test Conference,” Baltimore, MD, Oct. 17-21, 1993. (NSF, ONR)

Avra, L.J., and E.J. McCluskey, “Synthesizing for Scan Dependence in Built-In Self-Testable Design.”

Hao, H., and E.J. McCluskey, “Very-Low-Voltage Testing for Weak CMOS Logic ICs.”

McCluskey, E.J., “Quality and Single-Stuck Faults.”

(CRC TR 93-3) Munda, S.V., “Bibliography of 1969-1992 CRC Publications,” July 1993. (NSF, ONR)

(CRC TR 93-4) Ma, S., and E.J. McCluskey, “Open Faults in BiCMOS Gates,” Nov. 1993. (NSF, ONR)

(CRC TR 93-5) Pan, R., N.A. Touba, and E.J. McCluskey, “The Effect of Fault Dropping on Fault Simulation Time,” Nov. 1993. (NSF, ONR)

(CRC TR 93-6) Touba, N.A., and E.J. McCluskey, “Logic Synthesis for Concurrent Error Detection,” Nov. 1993. (NSF, ONR)

(CRC TR 93-7) Franco, P., and E.J. McCluskey, “On-Line Delay Testing of Digital Circuits,” Nov. 1993. (NSF, ONR)

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PRESENTATIONS

McCluskey, E.J., "Why Computers Fail or Who Needs Design for Testability?" *Tandem*, Austin, TX, Jan. 11, 1993.

McCluskey, E.J., "Reducing the Performance Penalty of BIST," *Office of Naval Research First Annual Workshop on Embedded Systems*, Austin, TX, Jan. 11-13, 1993.

McCluskey, E.J., "Retrospective of the Computer Forum's Twenty-five Years," *Computer Forum 25th Annual Meeting*, Stanford, CA, Feb. 23-25, 1993.

Franco, P., "Testing Digital Circuits by Output Waveform Analysis," *Computer Forum 25th Annual Meeting*, Stanford, CA, Feb. 23-25, 1993.

McCluskey, E.J., “Why Computers Fail or Who Needs Design-for-Testability?” *Distinguished Lecturer Series*, Texas A&M University, College Station, TX, April 23, 1993.

McCluskey, E.J., “Very-high-level Synthesis and Built-in Self Test,” *CRHC Special Lecture Series*, University of Illinois, Sep. 23, 1993.

McCluskey, E.J., “Fads and Ethics in Test Research,” *AT&T Conference on Electronic Testing (ACET 93)*, Princeton, NJ, Sep. 27-28, 1993.

AWARDS

Franco, P., “A Night in the Life of . . .,” First Place Winner, Student Essay Competition, NCR, Computerworld and Computer Society of IEEE, 1993.

1993 VISITORS

Dr. Edward Eichelberger, IBM Corporation, Kingston, NY, Feb. 1993
Prof. Takashi Nanya, Tokyo Institute of Technology, Japan, Mar. 1993
Robert Khamashta, Raytheon, Mountain View, CA, Apr. 1993
Dr. Winfrid Schneeweiss, Apr. 93

1993 VISITING SCHOLARS

Prof. Han Seok-Bung, Gyeonsang National University, Korea
Prof. Jacob Abraham, University of Texas at Austin, Austin, TX
Prof. Florinel Balteanu, University of Pitesti, Romania
Prof. Xingning Xu, Beijing University of Posts and Telecommunications, China
Prof. Teruhiko Yamada, Meiji University, Japan

1993 CRC PhDs GRANTED

Hong Hao, “Electrical Failure Modes in CMOS Logic Integrated Circuits,” 1993 (CRC)

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TECHNICAL FACILITIES
CENTER FOR RELIABLE COMPUTING

TEST EQUIPMENT:

Laboratory Oven: AES Model ZCK-9204 laboratory oven to be used for accelerated life testing and burn-in.
Tektronix Lab Instruments: MHz function generator, 40 MHz function generator - very fancy, 2 Triple power supplies, 2 Digital Multimeters, 5 Coax cables for connecting FGs to boards, 2 Mainframes to hold one each of PS, DM, and FG.
Tektronix Design Analysis System (DAS 9200): Motorola 68010-based test system with 2MB memory, 20MB hard disk, and color display. Equipped with a 32-channel 50 MHz pattern generation card, two 16-channel 200MHz data acquisition cards, 92 DV device verification software, and TF 100 test fixture.
DAS9200: 1 Tester mainframe, keyboard and monitor. 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes. 36 Channel 50MHZ sequence pattern generator.
DAS9252: 1 Tester mainframe, keyboard and monitor. Includes board and accompanying flying lead set for microprocessor testing (90 channels), 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes, 18-channel 50 MHz pattern generator, Test fixture, 21x21 pin grid array fixture to fit TF100
1241BNO-1B: 1 Color logic analyzer mainframe, 2 18-channel cards, 1 9-channel card, 5 P6460 probes, performance analysis ROM pack, 64K RAM pack, parallel printer COMM pack, printer support ROM pack
Tektronix 2467: 1350 MHz four channel portable oscilloscope with word recognizer.
Tektronix 4696: 1Color ink-jet printer.

WORKSTATIONS:

Sun Sparcstation Classic running Solaris with 200MB and 1.2GB hard disks, 16MB main memory, 3.5" floppy disk drive, and Ethernet capability.
Sun Sparcstation SLC running SunOs with 389MB hard disk, 8MB main memory, and Ethernet capability.
Sun 3/140 work station running SunOs with two 64MB hard disks, 8M main memory, QIC-24 tape drive, and Ethernet capability.
Sony NWS-1930 workstation running UNIX BSD4.3 with 16 MBytes of memory, two 256 MB-hard drives, QIC-120 tape drive, 3.5" floppy disk drive, and Ethernet capability.
IBM PC-RT reduced instruction set personal computer running AIX with high resolution color monitor, hard disk, streaming tape drive, and Ethernet capability.
Tektronix 4317 color graphics workstation running UTek (Tektronix Unix) with 60MB and 35MB hard drives, 4MB main memory, and Ethernet capability.
MicroVAX GPX II running VMS with 70MB and 140MB hard disks 13M main memory, and Ethernet capability.
VAXstation 2000 running VMS with 40MB and 70MB hard disks. Access to a VAX 780 running Ultrix.
Delni-aa ethernet multiplexer and a transceiver providing access to the Ethernet for the MicroVAX, Sun, Sony, TEK 4317, and PC-RT workstations.

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PERSONAL COMPUTERS:

Apple Macintosh Personal Computers: One Mac Centris 650 with 8 MB RAM 230 MB hard disk, CD-ROM drive and basic color monitor; one Mac IIcx with 5 MB RAM and 40 MB hard disk, one Mac SE30 with 5 MB RAM and 40 MB hard disk, and one Mac SE with 4 MB RAM and 40 MB hard disk. An Appletalk network connects the Macs together that allow file sharing through System 7.1 and printing on an Apple Laserwriter IINT printer.

IBM Personal Computers: IBM PC-AT personal computer with enhanced graphics board, high-resolution color monitor, hard disk, and printer. Includes ViewLogic software for schematic capture, simulation, waveform analysis, and fault grading.

TECHNICAL FACILITIES
SOFTWARE SYSTEMS

The lab houses 7 digital testing Systems: Teradyne, EDA's Lasar, Genrad's HILO, HHB's CADAT and Intelligen, VHDL design and simulation tools from Vantage and Viewlogic, and Picasso.

CADAT 6.1: CADAT is a logic and fault simulator that is suitable for combinational and sequential circuits. Intelligen is a sequential test pattern generator.
Hilo: GenRad's Hilo comprises logic and fault simulators and a test pattern generation.
Lasar: This VMS-based system is hosted on a MicroVAX and consists of logic and fault simulators, and ATPG for both combinational and sequential circuits. The system includes large model libraries.
Picasso: A complete gate level sequential test pattern generation, logic and fault simulation system for VLSI designs.
Spice: Spice systems for analog simulation of devices and circuits: tSpice is hosted on the Tektronix and pSpice on the IBM AT.
Vantage: VHDL simulator and intermediate format access tools.
Viewlogic: This is a schematic capture and a logic simulator that is also capable of injecting some faults in the design. The system is mainly used for logic design courses. The version hosted on the VAXstation also has the capacity to simulate VHDL behavioral models.

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