1994 CRC ACTIVITIES

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ABSTRACT

This report lists the 1994 CRC Activities.

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LIST OF PUBLICATIONS

JOURNAL PAPERS

Published

[Saxena 94] Saxena, N.R. and E.J. McCluskey, "Linear Complexity Assertions for Sorting Algorithms," *IEEE Trans. Software Eng.,* Vol. 20, No. 6, pp. 424-431, June 1994. (HP, ONR, NSF)

Accepted

[Boley 94] Boley, D., G.H. Golub, S. Makar, N. Saxena, and E.J. McCluskey, "Floating Point Fault-Tolerance with Backward Error Assertions," *IEEE Trans. Comput., Special Issue on Fault-Tolerant Computing.*

[Ma 94] Ma, S.C., and E.J. McCluskey, "Open Faults in BiCMOS Gates," *IEEE Trans. Computer-Aided Design*, Feb. 1995.

Submitted

[Saxena 94] Saxena, N.R., and E.J. McCluskey, "Counting Transition-Tour Sequences," *IEEE Trans. Comput.*

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CONFERENCE PAPERS

Published

[Avra 94] Avra, L.J., and E.J. McCluskey, "High-Level Synthesis of Testable Designs: An Overview of University Systems," *Proc. 1994 Int. Test Conf.*, Test Synthesis Seminar, Washington, D.C., TS Paper 1.1, Oct. 2-6, 1994. (ONR, NSF)

[Franco 94] Franco, P., and E.J. McCluskey, "On Line Delay Testing of Digital Circuits," *12th IEEE VLSI Test Symposium*, Cherry Hill, NJ, pp. 167-173, Apr. 25-28, 1994. (ONR, NSF)

[Franco 94] Franco, P., and E.J. McCluskey, "3-Pattern Delay Fault Tests," *12th IEEE VLSI Test Symposium*, Cherry Hill, NJ, pp. 452-456, Apr. 25-28, 1994. (ONR, NSF)

[Ma 94] Ma, S., and E.J. McCluskey, "Open Faults in BiCMOS Gates," *12th IEEE VLSI Test Symposium*, Cherry Hill, NJ, pp. 434-439, Apr. 25-28, 1994. (ONR, NSF)

[Touba 94] Touba, N.A., and E.J. McCluskey, "Logic Synthesis of Random Pattern Testable Circuits Using Algebraic Transformations," *First Int. Test Synthesis Workshop*, Poster Session, Santa Barbara, CA, May 18-20, 1994. (ONR, NSF)

[Touba 94] Touba, N.A., and E.J. McCluskey, "Automated Logic Synthesis of Random Pattern Testable Circuits," *Proc. 1994 Int. Test Conf.*, Washington, D.C., pp. 174-183, Oct. 2-6, 1994. (ONR, NSF)

[Touba 94] Touba, N.A., and E.J. McCluskey, "Logic Synthesis Techniques for Reduced Area Implementation of Multilevel Circuits with Concurrent Error Detection," *ICCAD-94*, San Jose, CA, pp. 651-654, Nov. 6-10, 1994.

Accepted

[Makar 95] Makar, S., and E.J. McCluskey, "Checking Experiments to Test Latches," *13th IEEE VLSI Test Symp., Princeton, NJ*, Apr. 30 - May 3, 1995.

[Mukund 95] Mukund, S.K., E.J. McCluskey, and T.R.N. Rao, "An Apparatus for Pseudo-Deterministic Testing," *13th IEEE VLSI Test Symp., Princeton, NJ*, Apr. 30 - May 3, 1995.

[Touba 95] Touba, N.A., and E.J. McCluskey, "Transformed Pseudo-Random Patterns for BIST," *13th IEEE VLSI Test Symp., Princeton, NJ*, Apr. 30 - May 3, 1995.

Submitted

[Ma 95] Ma, S., and E.J. McCluskey, "Scan Cells for Dynamic Latches," *ISSCC'95*, San Francisco, CA, Feb. 15-17, 1995.

[Yamada 95] Yamada, T., K. Yamazaki, and E.J. McCluskey, "A Simulation-Based Diagnosis of Single Faults in CMOS Combinational Circuits," *13th IEEE VLSI Test Symp., Princeton, NJ*, Apr. 30 - May 3, 1995.

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CRC TECHNICAL REPORTS

(CRC TR 94-0) Munda, S.V., “Bibliography 1993 CRC Activities,” Jan. 1994. (NSF, ONR)

(CRC TR 94-1) “Preprints of papers from the *12th IEEE VLSI Test Symposium*,” Cherry Hill, NJ, Apr. 25-28, 1994.

Franco, P., and E.J. McCluskey, “On Line Delay Testing of Digital Circuits.”

Franco, P., and E.J. McCluskey, “3-Pattern Delay Fault Tests.”

Ma, S., and E.J. McCluskey, “Open Faults in BiCMOS Gates.”

(CRC TR 94-2) Avra, L.J., and E.J. McCluskey, “Synthesis for Scan Dependence in Built-In Self-Testable Designs,” May 1994. (ONR, NSF)

(CRC TR 94-3) Avra, L.J., L. Gerbaux, J.-C. Giomi, F. Martinolle, and E.J. McCluskey, “A Synthesis-for-Test Design System,” May 1994. (ONR, NSF)

(CRC TR 94-4) Franco, P., and E.J. McCluskey, “WSIM: A Symbolic Waveform Simulator,” June 1994. (ONR, NSF)

(CRC TR 94-5) Franco, P., R.L. Stokes, W.D. Farwell, and E.J. McCluskey, “An Experimental Chip to Evaluate Test Techniques Part 1: Description of Experiment,” June 1994. (Hughes, ONR, NSF)

(CRC TR 94-6) Preprints of papers from the “*1994 International Test Conference*,” Washington, DC, Oct. 2-6, 1994 and “*International Conference on CAD-94*,” San Jose, CA, Nov. 6-10, 1994.

Touba, N.A., and E.J. McCluskey, “Automated Logic Synthesis of Random Pattern Testable Circuits,” ITC’94.

Touba, N.A., and E.J. McCluskey, “Logic Synthesis Techniques for Reduced Area Implementation of Multilevel Circuits with Concurrent Error Detection,” ICCAD’94.

(CRC TR 94-7) Avra, L.J., “Synthesis Techniques for Built-In Self-Testable Designs,” July 1994. (DEC, ONR, NSF)

(CRC TR 94-8) Preprint of paper from the “*1994 International Test Conference*,” Washington, DC, Oct. 2-6, 1994.

Avra, L.J., and E.J. McCluskey, “High-Level Synthesis of Testable Designs: An Overview of University Systems.”

(CRC TR 94-9) Franco, P., “Testing Digital Circuits for Timing Failures by Output Waveform Analysis,” September 1994. (Hughes, ONR, NSF)

(CRC TR 94-10) Touba, N.A., and E.J. McCluskey, “Transformed Pseudo-Random Patterns for BIST,” Oct. 1994. (ONR, NSF)

(CRC TR 94-11) Makar, S., and E.J. McCluskey, “Using Checking Experiments To Test D-Latches,” In preparation. (ONR, NSF, Cirrus)

(CRC TR 94-12) Mukund, S.K., E.J. McCluskey, and T.R.N. Rao, “An Apparatus for Pseudo-Deterministic Testing,” Oct. 1994. (ONR, NSF, Cirrus)

(CRC TR 94-13) Ma, S.C., and E.J. McCluskey, “Design-for-Current-Testability (DFCT) for Dynamic CMOS Logic,” Nov. 1994. (ONR, NSF)

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AWARDS

McCluskey, E.J., "ACM Fellow," *Association for Computing Machinery*, Phoenix, AZ, Mar. 8, 1994.

McCluskey, E.J., "Doctor Honoris Causa," *Institut National Polytechnique de Grenoble* (I.N.P.G.), Grenoble, France, Apr. 15, 1994.

1994 VISITORS

Dr. Wolfgang Kunz, University of Potsdam, June 1994
Dr. Ravi Iyer, University of Illinois, June 1994
Dr. Ram Chillarege, IBM New York, August 1994
Dr. Hiroshi Yokoyama, Akita University, August 1994
Dr. Yervant Zorian, AT&T, August 1994

1994 VISITING SCHOLARS

Dr. Qingfang Chen, IC Testing Technology Center, China
Prof. Okihiko Ishizuka, Miyazaki University, Japan
Prof. Xingning Xu, Beijing University of Posts and Telecommunications, China

1994 CRC PhDs GRANTED

L. Avra, "Synthesis Techniques for Built-in Self-Testable Designs," June 1994

P. Franco, "Testing Digital Circuits for Timing Failures by Output Waveform Analysis," June 1994

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TECHNICAL FACILITIES
CENTER FOR RELIABLE COMPUTING

TEST EQUIPMENT:

Tektronix Lab Instruments: MHz function generator, 40 MHz function generator - very fancy, 2 Triple power supplies, 2 Digital Multimeters, 5 Coax cables for connecting FGs to boards, 2 Mainframes to hold one each of PS, DM, and FG.
Tektronix Design Analysis System (DAS 9200): Motorola 68010-based test system with 2MB memory, 20MB hard disk, and color display. Equipped with a 32-channel 50 MHz pattern generation card, two 16-channel 200MHz data acquisition cards, 92 DV device verification software, and TF 100 test fixture.
DAS9200: 1 Tester mainframe, keyboard and monitor. 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes. 36 Channel 50MHZ sequence pattern generator.
DAS9252: 1 Tester mainframe, keyboard and monitor. Includes board and accompanying flying lead set for microprocessor testing (90 channels), 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes, 18-channel 50 MHz pattern generator, Test fixture, 21x21 pin grid array fixture to fit TF100
1241BNO-1B: 1 Color logic analyzer mainframe, 2 18-channel cards, 1 9-channel card, 5 P6460 probes, performance analysis ROM pack, 64K RAM pack, parallel printer COMM pack, printer support ROM pack
Tektronix 2467: 1350 MHz four channel portable oscilloscope with word recognizer.
Tektronix 4696: 1Color ink-jet printer.

WORKSTATIONS:

Sun Sparcstation Classic running SunOS with 200MB and 1.2GB hard disks, 16MB main memory, 3.5" floppy disk drive.
Sun Sparcstation SLC running SunOS with 389MB and 2.0 GB hard disks, 16MB main memory.
Sony NWS-1930 workstation running UNIX BSD4.3 with 16 MBytes of memory, two 256 MB-hard drives, QIC-120 tape drive, 3.5" floppy disk drive.
IBM PC-RT reduced instruction set personal computer running AIX with high resolution color monitor, hard disk, streaming tape drive.
Tektronix 4317 color graphics workstation running UTek (Tektronix Unix) with 60MB and 35MB hard drives, 4MB main memory.
Delni-aa ethernet multiplexer and a transceiver providing access to the Ethernet for the MicroVAX, Sun, Sony, TEK 4317, and PC-RT workstations.
Ethernet for the Sun, Sony, TEK 4317, and PC-RT workstations.

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PERSONAL COMPUTERS:

Apple Macintosh Personal Computers: One Mac Centris 650 with 16 MB RAM 230 MB hard disk, CD-ROM drive and basic color monitor; one Mac IIcx with 8 MB RAM and 345 MB hard disk, one Mac SE30 with 8 MB RAM and 40 MB hard disk, and one Mac SE with 4 MB RAM and 40 MB hard disk. An Appletalk network connects the Macs together that allow file sharing through System 7.1 and printing on an Apple Laserwriter IINT printer, the Centris 650 is connected to Internet through Ethernet.

IBM Personal Computers: IBM PC-AT personal computer with enhanced graphics board, high-resolution color monitor, hard disk, and printer. Includes ViewLogic software for schematic capture, simulation, waveform analysis, and fault grading.

TECHNICAL FACILITIES
SOFTWARE SYSTEMS

The lab houses the following computer-aided design tools:

CADAT 6.1: CADAT is a logic and fault simulator that is suitable for combinational and sequential circuits. Intelligen is a sequential test pattern generator.
COMPASS: COMPASS Design Automation Tools including a data path compiler, synthesis tools for data path logic, combinational logic, state machines, and BIST logic, a logic simulation tool, and a timing verification tool.
Hilo: GenRad's Hilo comprises logic and fault simulators and a test pattern generation.
LSI Logic: VLSI design tools for the Suns. Includes VHDL and Verilog libraries.
Picasso: A complete gate level sequential test pattern generation, logic and fault simulation system for VLSI designs.
Spice: Spice systems for analog simulation of devices and circuits. tSpice is hosted on the Tektronix, pSpice on the IBM AT, and hspice on the Suns.
Vantage: VHDL simulator and intermediate format access tools.
Viewlogic: This is a schematic capture and a logic simulator that is also capable of injecting some faults in the design. The system is mainly used for logic design courses. The version hosted on the VAXstation also has the capacity to simulate VHDL behavioral models.

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