1995 CRC ACTIVITIES

by S.V. Munda

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ABSTRACT

This report lists the 1995 CRC Activities.

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LIST OF PUBLICATIONS

JOURNAL PAPERS

Published

[Boley 95] Boley, D., G.H. Golub, S. Makar, N. Saxena, and E.J. McCluskey, "Floating Point Fault-Tolerance with Backward Error Assertions," *IEEE Trans. Comput., Special Issue on Fault-Tolerant Computing*, pp. 302-311, Feb. 1995.

[Ma 95] Ma, S.C., and E.J. McCluskey, "Open Faults in BiCMOS Gates," *IEEE Trans. Computer-Aided Design*, pp. 567-575, May 1995.

Accepted

[Saxena 96] Saxena, N.R., and E.J. McCluskey, "Counting Transition-Tour Sequences," *IEEE Trans. Comput.*

[Saxena 96] Saxena, N.R., and E.J. McCluskey, "Parallel Signature Analysis Design with Bounds on Aliasing," *IEEE Trans. Comput.*

Submitted

[Touba 96] Touba, NA., and E.J. McCluskey, "Logic Synthesis of Multilevel Circuits with Concurrent Error Detection," *IEEE Trans. CAD.*

CONFERENCE PAPERS

Published

[Franco 95] Franco, P., W.D. Farwell, E.J. McCluskey, R.L. Stokes, "An Experimental Chip to Evaluate Test Techniques: Chip and Experiment Design," *Proc.1995 Int.Test. Conf.*, pp. 653-662, Washington, DC, Oct. 23-25, 1995.

[Ma 95] Ma, S., and E.J. McCluskey, "An Experimental Chip to Evaluate Test Techniques: Experimental Results," *Proc.1995 Int.Test. Conf.*, pp. 663-672, Washington, DC, Oct. 23-25, 1995.

[Makar 95] Makar, S., and E.J. McCluskey, "Checking Experiments to Test Latches," *13th IEEE VLSI Test Symp.*, pp. 196-201, Princeton, NJ, Apr. 30 - May 3, 1995.

[Makar 95] Makar, S.R., and E.J. McCluskey, "Functional Tests for Scan Chain Latches," *Proc.1995 Int.Test. Conf.*, pp. 606-615, Washington, DC, Oct. 23-25, 1995.

[Mukund 95] Mukund, S.K., E.J. McCluskey, and T.R.N. Rao, "An Apparatus for Pseudo-Deterministic Testing," *13th IEEE VLSI Test Symp.*, pp. 125-131, Princeton, NJ, Apr. 30 - May 3, 1995.

[Touba 95] Touba, N.A., and E.J. McCluskey, "Transformed Pseudo-Random Patterns for BIST," *13th IEEE VLSI Test Symp.*, pp. 410-416, Princeton, NJ, Apr. 30 - May 3, 1995.

[Touba 95] Touba, N.A., and E.J. McCluskey, "Synthesis of Mapping Logic for Generating Transformed Pseudo-Random Patterns for BIST," *Proc.1995 Int.Test. Conf.*, pp. 674-682, Washington, DC, Oct. 23-25, 1995.

Accepted

[Chang 96] Chang, T.Y.J., and E.J. McCluskey, "Quantitative Analysis of Very-Low-Voltage Testing," *14th IEEE VLSI Test Symp.*, Princeton, NJ, Apr. 28-May 1, 1996. (ONR, NSF)

[Norwood 96] Norwood, R.B., and E.J. McCluskey, "Synthesis-for-Scan and Scan Chain Ordering," *14th IEEE VLSI Test Symp.*, Princeton, NJ, Apr. 28-May 1, 1996. (ONR, NSF, ARPA)

[Touba 96] Touba, N.A., and E.J. McCluskey, "Applying Two-Pattern Tests Using Scan-Mapping," *14th IEEE VLSI Test Symp.*, Princeton, NJ, Apr. 28-May 1, 1996. (ONR, NSF, ARPA)

[Touba 96] Touba, N.A., and E.J. McCluskey, "Test Point Insertion Based on Path Tracing," *14th IEEE VLSI Test Symp.*, Princeton, NJ, Apr. 28-May 1, 1996. (ONR, NSF, ARPA)

CRC TECHNICAL REPORTS

(CRC TR 95-0) Munda, S.V., “Bibliography 1994 CRC Activities,” Feb. 1995. (NSF, ONR, ARPA)

(CRC TR 95-1) Ma, S., “Testing BiCMOS and Dynamic CMOS Logic,” June 1995. (NSF, ONR)

(CRC TR 95-2) “Preprints of papers accepted for presentation at the 1995 International Test Conference, Oct. 23-25, 1995, Washington, D.C.” (ONR, NSF, ARPA)

Franco, P., W.D. Farwell, R.L. Stokes, and E.J. McCluskey, “An Experimental Chip to Evaluate Test Techniques Chip and Experiment Design.”

Ma, S.C., P. Franco, and E.J. McCluskey, “An Experimental Chip to Evaluate Test Techniques Experiment Results.”

Makar, S.R., and E.J. McCluskey, “Functional Tests for Scan Chain Latches.”

Touba, N.A., and E.J. McCluskey, “Synthesis for Mapping Logic for Generating Transformed Pseudo-Random Patterns for BIST.”

CRC TECHNICAL NOTE

(CRC TN 95-1) "Preprints of papers submitted to the 1995 International Test Conference to be held on Oct. 23-25, 1995 at Washington, DC." (ONR, NSF)

Farwell, W.D., P. Franco, E.J. McCluskey, R.L. Stokes, and F. Zarrinfar, "An Experimental Chip to Evaluate Test Techniques, Part 1: Concepts & Objectives."

Franco, P., W.D. Farwell, E.J. McCluskey, and R.L. Stokes, "An Experimental Chip to Evaluate Test Techniques, Part 2: Chip Design."

Ma., S.C., P. Franco, and E.J. McCluskey, "An Experimental Chip to Evaluate Test Techniques, Part 3: Data Analysis and Experimental Results."

PRESENTATIONS

[Avra 95] Avra, L., "Synthesis for Scan Dependency in BIST Design," *1995 CRC-IEEE BAST Workshop*, Bodega Bay, CA, Feb. 15-18, 1995.
[Franco 95] Franco, P., "Three-Pattern Delay Tests," *1995 CRC-IEEE BAST Workshop*, Bodega Bay, CA, Feb. 15-18, 1995.
[Ma 95] Ma, S., "Scan Cells for Dynamic Latches," *1995 CRC-IEEE BAST Workshop*, Bodega Bay, CA, Feb. 15-18, 1995.
[McCluskey 95] McCluskey, E.J., "Tools for Dependable System Design and Evaluation," *IFIP Working Group 10.4 Workshop*, South Lake Tahoe, CA, June 23-16, 1995.
[McCluskey 95] McCluskey, E.J., "Tops Synthesis Tool: A Design Framework for Dependable Computing Systems," *Sun Microsystems*, Menlo Park, CA, July 12, 1995.
[Touba 95] Touba, N.A., "Logic Synthesis of Random Pattern Testable Circuits," *1995 CRC-IEEE BAST Workshop*, Bodega Bay, CA, Feb. 15-18, 1995.
[Touba 95] Touba, N.A., and E.J. McCluskey, "Transformed Pseudo-Random Patterns for BIST," *Built-In Self-Test/Design for Testability Workshop*, Charleston, SC, Mar. 15-17, 1995.
[Touba 95] Touba, N.A., and E.J. McCluskey, "Synthesis of Mapping Logic for Generating Transformed Pseudo-Random Patterns for BIST," *2nd Int. Test Synthesis Workshop*, Santa Barbara, CA, May 8-10, 1995.

AWARDS

McCluskey, E.J., IEEE Emanuel R. Piore Award.

1995 VISITORS

Dr. Farzad Zarrinfar, LSI Logic, January 1995
Dr. R. Chandramouli, Mentor Graphics, February 1995
Dr. Ying-Hua Min, February 1995
Dr. Lutz Volkel, Berkeley, April 1995
Dr. Pierre Barnabe, Thomson-CSF, France, May 1995
Dr. Christian Girardeau, Thomson-CSF, France, May 1995
Dr. Bernd K. Koenemann, IBM, June 1995
Dr. Robert Grafton, National Science Foundation, June 1995
Dr. A.J. van de Goor, Delft University of Technology, The Netherlands, August 1995

1995 VISITING SCHOLARS

Dr. Qingfang Chen, IC Testing Technology Center, China
Dr. Irith Pomeranz, University of Iowa
Dr. Hans-Joachim Wunderlich, Institut fuer Rechnerstrukturen, Germany
Prof. Xingning Xu, Beijing University of Posts and Telecommunications, China

1995 CRC PhDs GRANTED

Ma, S., "Testing BiCMOS and Dynamic CMOS Logic," June 1995.

TECHNICAL FACILITIES
CENTER FOR RELIABLE COMPUTING

TEST EQUIPMENT:

Tektronix Lab Instruments: MHz function generator, 40 MHz function generator - very fancy, 2 Triple power supplies, 2 Digital Multimeters, 5 Coax cables for connecting FGs to boards, 2 Mainframes to hold one each of PS, DM, and FG.

Tektronix Design Analysis System (DAS 9200): Motorola 68010-based test system with 2MB memory, 20MB hard disk, and color display. Equipped with a 32-channel 50 MHz pattern generation card, two 16-channel 200MHz data acquisition cards, 92 DV device verification software, and TF 100 test fixture.

DAS9200: 1 Tester mainframe, keyboard and monitor. 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes. 36 Channel 50MHZ sequence pattern generator.

DAS9252: 1 Tester mainframe, keyboard and monitor. Includes board and accompanying flying lead set for microprocessor testing (90 channels), 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes, 18-channel 50 MHz pattern generator, Test fixture, 21x21 pin grid array fixture to fit TF100

1241BNO-1B: 1 Color logic analyzer mainframe, 2 18-channel cards, 1 9-channel card, 5 P6460 probes, performance analysis ROM pack, 64K RAM pack, parallel printer COMM pack, printer support ROM pack

Tektronix 2467: 1350 MHz four channel portable oscilloscope with word recognizer.

Tektronix 4696: 1Color ink-jet printer.

WORKSTATIONS:

Sun SparcStation 20 MP: Running Solaris, with 1GB hard disk and 4GB disk, 128MB main memory, CDROM drive, and 3.5" floppy disk drive.

Sun SparcStation 20 MP: Running Solaris, with 1GB hard disk and 4GB disk, 128MB main memory, CDROM drive, and 3.5" floppy disk drive.

Sun SparcStation 20: Running Solaris, with 1GB hard disk, 128MB main memory, CDROM drive, and 3.5" floppy disk drive.

Sun SparcStation 1+: Running SunOS, with 328MB hard disk, 40MB main memory, and 3.5" floppy disk drive.

Sun SparcStation 1+: Running SunOS, with 328MB hard disk, 40MB main memory, and 3.5" floppy disk drive.

Sun SparcClassic: Running SunOS, with 128MB and 1GB hard disks, 16MB main memory, and 3.5" floppy disk drive.

Sun Sparcstation SLC: Running SunOS, with 389MB hard disk, and 16MB main memory.

Sony NWS-1930: Running UNIX BSD4.3, two 256MB hard disks, 16MB main memory, QIC-120 tape drive, and 3.5" floppy disk drive.

Intel 120MHz Pentium: Running Lynix, with 1MB hard disk, 24MB main memory, CDROM drive, and 3.5" floppy disk drive.

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Intel 120MHz Pentium: Running Lynix, with 1MB hard disk, 24MB main memory, CDROM drive, and 3.5" floppy disk drive.

PERSONAL COMPUTERS:

Apple Macintosh Personal Computers: Two Power Macintosh 8100s/100 with 16 MB RAM 1 GB hard disk, double-speed CD ROM drive and 17" Multiple Scan Display, one Power Macintosh 7500/100 with 16MB RAM, 1GB hard drive, quad-speed CD ROM drive and 17" Multiple Scan Display, one Mac Centris 650 with 16 MB RAM 230 MB hard disk, double-speed CD-ROM drive and basic color monitor; one Mac IIcx with 8 MB RAM and 345 MB hard disk, one Mac SE30 with 8 MB RAM and 40 MB hard disk, and one Mac SE with 4 MB RAM and 40 MB hard disk. The two Power Macintosh 8100s, one Power Macintosh 7500, one Centris 650, and an Apple Laserwriter IINT is connected to Internet through Ethernet. All three Power Macintoshes use System 7.5. An Appletalk network connects the other Macs together that allow file sharing through System 7.1.

IBM Personal Computers: IBM PC-AT personal computer with enhanced graphics board, high-resolution color monitor, hard disk, and printer. Includes ViewLogic software for schematic capture, simulation, waveform analysis, and fault grading.

TECHNICAL FACILITIES
SOFTWARE SYSTEMS

The lab houses the following computer-aided design tools:

COMPASS: COMPASS Design Automation Tools including a data path compiler, synthesis tools for data path logic, combinational logic, state machines, and BIST logic, a logic simulation tool, and a timing verification tool.
Hilo: GenRad's Hilo comprises logic and fault simulators and a test pattern generation.
LSI Logic: VLSI design tools. Includes VHDL and Verilog libraries.
Spice: Spice is an analog simulator for devices and circuits.
Syntest: A test pattern generation, and logic and fault simulation system for VLSI designs.
Vantage: VHDL simulator and intermediate format access tools.
Viewlogic: This is a schematic capture and a logic simulator that is also capable of injecting some faults in the design. The system is mainly used for logic design courses, and is hosted on the IBM PC-ATs.