1996 CRC ACTIVITIES

by S.V. Munda

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CENTER FOR RELIABLE COMPUTING
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ABSTRACT

This report lists the 1996 CRC Activities.

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TABLE OF CONTENTS

LIST OF PUBLICATIONS

JOURNAL PAPERS

Published

[Saxena 96] Saxena, N.R., and E.J. McCluskey, "Counting Two-State Transition-Tour Sequences," *IEEE Trans. Comput.*, Vol. 45, No. 11, pp. 1337-1342, Nov. 1996.

Accepted

[Saxena 97] Saxena, N.R., and E.J. McCluskey, "Parallel Signature Analysis Design with Bounds on Aliasing," *IEEE Trans. Comput.*
[Touba 97] Touba, N.A., and E.J. McCluskey, "Logic Synthesis of Multilevel Circuits with Concurrent Error Detection," *IEEE Trans. CAD.*

Submitted

[Chang 97] Chang, T.Y.J., and E.J. McCluskey, "Quantitative Analysis of Very-Low-Voltage Testing," *IEEE Trans. CAD of Integrated Circuits and Systems, Special Section*, Mar. 1997.
[Touba 97] Touba, N.A., and E.J. McCluskey, "RP-SYN: Synthesis of Random Pattern Testable Circuits with Test Point Insertion," *IEEE Trans. CAD.*
[Touba 97] Touba, N.A., and E.J. McCluskey, "Test Point Insertion Based on Path Tracing," *IEEE Trans. CAD of Integrated Circuits and Systems, Special Section*, Mar. 1997.

CONFERENCE PAPERS

Published

[Chang 96] Chang, T.Y.J., and E.J. McCluskey, "Quantitative Analysis of Very-Low-Voltage Testing," *14th IEEE VLSI Test Symp.*, pp. 332-337, Princeton, NJ, Apr. 28-May 1, 1996. (ONR, NSF)

[Chang 96] Chang, T.-Y.J., and E.J. McCluskey, "Detecting Delay Flaws by Very-Low-Voltage Testing," *Proc. 1996 Int. Test. Conf.*, pp. 367-376, Washington, DC, Oct. 22-24, 1996.

[Chang 96] Chang, T.-Y.J., and E.J. McCluskey, "SHOrt Voltage Elevation (SHOVE) Testing," *1996 IEEE Int. Workshop on IDDQ Testing*, pp. 45-49, Washington, DC, Oct. 24-25, 1996. (NSF, LSI)

[Franco 96] Franco, P., S. Ma, J. Chang, Y. Chu, S. Wattal, R. Stokes, W. Farwell, and E.J. McCluskey, "Analysis and Detection of Timing Failures in an Experimental Test Chip," *Proc. 1996 Int. Test. Conf.*, pp. 691-700, Washington, DC, Oct. 22-24, 1996. (NSF)

[Makar 96] Makar, S.R., and E.J. McCluskey, "Some Faults need an I_{ddq} Test," *1996 IEEE Int. Workshop on IDDQ Testing*, pp. 102-103, Washington, DC, Oct. 24-25, 1996. (ARPA, NSF, ONR)

[Norwood 96] Norwood, R.B., and E.J. McCluskey, "Synthesis-for-Scan and Scan Chain Ordering," *14th IEEE VLSI Test Symp.*, pp. 87-91, Princeton, NJ, Apr. 28-May 1, 1996. (ONR, NSF, ARPA)

[Norwood 96] Norwood, R.B., and E.J. McCluskey, "Orthogonal Scan Path Architectures," *Proc. 1996 Int. Test. Conf.*, pp. 659-668, Washington, DC, Oct. 22-24, 1996.

[Touba 96] Touba, N.A., and E.J. McCluskey, "Applying Two-Pattern Tests Using Scan-Mapping," *14th IEEE VLSI Test Symp.*, pp. 393-397, Princeton, NJ, Apr. 28-May 1, 1996. (ONR, NSF, ARPA)

[Touba 96] Touba, N.A., and E.J. McCluskey, "Test Point Insertion Based on Path Tracing," *14th IEEE VLSI Test Symp.*, Princeton, NJ, pp. 2-8, Apr. 28-May 1, 1996. (ONR, NSF, ARPA)

[Touba 96] Touba, N.A., and E.J. McCluskey, "Altering a Pseudo-Random Bit Sequence for Scan-Based BIST," *Proc. 1996 Int. Test. Conf.*, pp. 167-175, Washington, DC, Oct. 22-24, 1996. (ARPA, NSF, ONR)

Accepted

[Chang 97] Chang, T.Y.J., and E.J. McCluskey, "SHOrt Voltage Elevation (SHOVE) Test for Weak CMOS ICs," *submitted to the 15th IEEE VLSI Test Symposium*, Monterey, CA, Apr. 27-30, 1997. (CRC TN 96-2) (LSI, NSF)

[Makar 97] Makar, S.R., and E.J. McCluskey, "ATPG For Scan Chain Latches and Flip-Flops," *submitted to the 15th IEEE VLSI Test Symposium*, Monterey, CA, Apr. 27-30, 1997. (CRC TN 96-3) (ARPA, NSF, ONR)

[Norwood 97] Norwood, R.B., and E.J. McCluskey, "High-Level Synthesis for Scan," *submitted to the 15th IEEE VLSI Test Symposium*, Monterey, CA, Apr. 27-30, 1997. (CRC TN 96-4) (ARPA, NSF, ONR)

CRC TECHNICAL REPORTS

(CRC TR 96-0) “Bibliography 1995 CRC Activities,” Jan. 1996. (NSF, ONR, ARPA)

(CRC TR 96-1) Preprints of papers accepted for presentation at the *14th IEEE VLSI Test symposium (VTS 96)*, Princeton, NJ, April 28-May 1, 1996. (ONR, NSF, ARPA)

Chang, T.-Y.J., and E.J. McCluskey, "Quantitative Analysis of Very-Low-Voltage Testing."

Norwood, R.B., and E.J. McCluskey, "Synthesis-for-Scan Chain Ordering."

Touba, N.A., and E.J. McCluskey, "Applying Two-Pattern Tests Using Scan-Mapping."

Touba, N.A., and E.J. McCluskey, "Test Point Insertion Based on Path Tracing."

(CRC TR 96-2) Preprints of papers accepted for presentation at the *1996 International Test Conference (ITC’96)*, Washington, DC, Oct. 20-24, 1996. (ONR, NSF, ARPA, LSI)

Chang, T.-Y.J., and E.J. McCluskey, “Detecting Delay Flaws by Very-Low-Voltage Testing.”

Franco, P., S. Ma, J. Chang, Y. Chu, S. Wattal, R. Stokes, W. Farwell, and E.J. McCluskey, “Analysis and Detection of Timing Failures in an Experimental Test Chip.”

Norwood, R.B., and E.J. McCluskey, “Orthogonal Scan Path Architectures.”

Touba, N.A., and E.J. McCluskey, “Altering a Pseudo-Random Bit Sequence for Scan-Based BIST.”

(CRC TR 96-3) Touba, N.A., and E.J. McCluskey, “Test Point Insertion for Non-Feedback Bridging Faults,” Aug. 1996. (ARPA, NSF, ONR)

(CRC TR 96-4) Touba, N.A., “Synthesis Techniques for Pseudo-Random Built-In Self-Test,” Aug. 1996. (ARPA, NSF, ONR)

(CRC TR 96-5) Makar, S., “Checking Experiments For Scan Chain Latches and Flip-Flops,” Aug. 1996. (ARPA, NSF, ONR, Cirrus Logic)

CRC TECHNICAL NOTES

(CRC TN 96-1) Makar, S.R., and E.J. McCluskey, "Some Faults Need an IDDQ Test," Aug. 1996. (ARPA, NSF, ONR)
(CRC TN 96-2) Chang, T.Y.J., and E.J. McCluskey, "SHOrt Voltage Elevation (SHOVE) Test for Weak CMOS ICs," *submitted to the 15th IEEE VLSI Test Symposium*, Monterey, CA, Apr. 27-30, 1997. (LSI, NSF)
(CRC TN 96-3) Makar, S.R., and E.J. McCluskey, "ATPG For Scan Chain Latches and Flip-Flops," *submitted to the 15th IEEE VLSI Test Symposium*, Monterey, CA, Apr. 27-30, 1997. (ARPA, NSF, ONR)
(CRC TN 96-4) Norwood, R.B., and E.J. McCluskey, "High-Level Synthesis for Scan," *submitted to the 15th IEEE VLSI Test Symposium*, Monterey, CA, Apr. 27-30, 1997. (ARPA, NSF, ONR)

PRESENTATIONS

[Avra 96] Avra, L., and E.J. McCluskey, "An Overview of the Stanford TOPS (Totally-Optimized Synthesis) Tool," *Third Int. Test Synthesis Workshop*, Santa Barbara, CA, May 6-8, 1996. (ARPA)
[Norwood 96] Norwood, R.B., and E.J. McCluskey, "Orthogonal Scan Paths for Data Path Logic," *Third Int. Test Synthesis Workshop*, Santa Barbara, CA, May 6-8, 1996. (ARPA)
[Touba 96] Touba, N.A., and E.J. McCluskey, "Altering a Pseudo-Random Bit Sequence for Mixed-Mode Scan BIST," *3rd Int. Test Synthesis Workshop*, Santa Barbara, CA, May 6-8, 1996. (ARPA)
[Touba 96] Touba, N.A., and E.J. McCluskey, "Partial Isolation Rings for Testing Embedded Cores," *1996 IEEE Int. High Level Design Validation and Test Workshop*, San Jose, CA, Nov. 14-15, 1996. (ARPA)

AWARDS

McCluskey, E.J., IEEE Computer Society Golden Core Member, IEEE Computer Society, June 1996.

1996 VISITORS

Dr. Ken Wagner, Synopsys Inc., Mountain View, CA, July 22, 1996
Dr. Yervant Zorian, August 6, 1996
Dr. Wolfgang Kunz, University of Potsdam, Germany, November 14, 1996
Dr. Ray Mercer, Texas A&M University, November 14, 1996
Dr. Rabindra Roy, NEC, November 14, 1996
Dr. Daniel Saab, Case Western Reserve University, November 14, 1996
Dr. Nur A. Touba, University of Texas at Austin, November 14, 1996

1996 VISITING SCHOLARS

Dr. Hans-Joachim Wunderlich, Institut fuer Rechnerstrukturen, Germany
Dr. Winfrid Schneeweiss, Fern Universitat, Germany
Dr. Pinaki Mazumder, University of Michigan
Dr. Mohammed Niamat, University of Toledo

1996 CRC PhDs GRANTED

Makar, S., Checking Experiments for Scan Chain Latches and Flip-Flops, June 1996.
Touba, N., Synthesis Techniques for Pseudo-Random Built-In Self-Test, June 1996.

OTHER ACTIVITIES

University Services Other Than Teaching and Research
(Include administrative and other committee work)

EE Qualifying Examination Appeals Committee
Engineering Library Committee
CSD MSCS Committee
IEEE Student Branch Counselor
ACM Thesis Selection Committee

PROFESSIONAL ACTIVITIES OUTSIDE THE UNIVERSITY

General Chairman, IEEE BAST Workshop
FTCS-24 Advisory Committee
IEEE BIST/DFT Workshop Organizing Committee
IEEE International Computer Performance and Dependability Symposium Steering Committee
IEEE International Conference on Computer Aided Design Panel Session Moderator
IEEE International High Level Design Validation and Test Workshop Program Committee
IEEE VLSI Test Symposium Program Committee and Panel Session Moderator
IEEE Int. Test Synthesis Workshop Program Committee
IEEE International On-Line Testing Workshop Program Committee
ITC 1996, Tutorial, Digital Test Principles, Session Chair and Panel Session Moderator

Member Advisory Board of the IEICE Transactions on Information and Systems
Member Editorial Advisory Board of the International Journal of Computer Systems Science and Engineering
Member International Advisory Board of the Computer Science and Informatics, Computer Society of India

TECHNICAL FACILITIES
CENTER FOR RELIABLE COMPUTING

TEST EQUIPMENT:

Tektronix Lab Instruments: MHz function generator, 40 MHz function generator - very fancy, 2 Triple power supplies, 2 Digital Multimeters, 5 Coax cables for connecting FGs to boards, 2 Mainframes to hold one each of PS, DM, and FG.

Tektronix Design Analysis System (DAS 9200): Motorola 68010-based test system with 2MB memory, 20MB hard disk, and color display. Equipped with a 32-channel 50 MHz pattern generation card, two 16-channel 200MHz data acquisition cards, 92 DV device verification software, and TF 100 test fixture.

DAS9200: 1 Tester mainframe, keyboard and monitor. 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes. 36 Channel 50MHZ sequence pattern generator.

DAS9252: 1 Tester mainframe, keyboard and monitor. Includes board and accompanying flying lead set for microprocessor testing (90 channels), 16-channel 200 MHz data acquisition expander, 16-channel 200 MHz data acquisition expander without probes, 18-channel 50 MHz pattern generator, Test fixture, 21x21 pin grid array fixture to fit TF100

1241BNO-1B: 1 Color logic analyzer mainframe, 2 18-channel cards, 1 9-channel card, 5 P6460 probes, performance analysis ROM pack, 64K RAM pack, parallel printer COMM pack, printer support ROM pack

Tektronix 2467: 1350 MHz four channel portable oscilloscope with word recognizer.

Tektronix 4696: 1 Color ink-jet printer.

WORKSTATIONS:

Sun UltraSPARC 2 MP: Running Solaris, with two 2.1GB hard disks, 256MB main memory.

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Sun UltraSPARC 2 MP: Running Solaris, with two 2.1GB hard disks, 256MB main memory.

Sun SparcStation 20 MP: Running Solaris, with 1GB hard disk and 4GB external disk, 128MB main memory, CDROM drive, and 3.5" floppy disk drive.

Sun SparcStation 20 MP: Running Solaris, with 1GB hard disk and 4GB external disk, 128MB main memory, CDROM drive, and 3.5" floppy disk drive.

Sun SparcStation 20 MP: Running Solaris, with 1GB hard disk, 128MB main memory, CDROM drive, and 3.5" floppy disk drive.

Sun SparcStation 1+: Running SunOS, with 328MB hard disk, 40MB main memory, and 3.5" floppy disk drive.

Sun SparcStation 1+: Running SunOS, with 328MB hard disk, 40MB main memory, and 3.5" floppy disk drive.

Sun SparcClassic: Running SunOS, with 128MB and 1GB hard disks, 16MB main memory, and 3.5" floppy disk drive.

Sun Sparcstation SLC: Running SunOS, with 389MB hard disk, and 16MB main memory.

Intel 120MHz Pentium: Running Lynix, with 1MB hard disk, 24MB main memory, CDROM drive, and 3.5" floppy disk drive.
Intel 120MHz Pentium: Running Lynix, with 1MB hard disk, 24MB main memory, CDROM drive, and 3.5" floppy disk drive.
Intel 120MHz Pentium: Running Lynix, with 1MB hard disk, 24MB main memory, CDROM drive, and 3.5" floppy disk drive.
Intel 120MHz Pentium: Running Lynix, with 1MB hard disk, 24MB main memory, CDROM drive, and 3.5" floppy disk drive.

PERSONAL COMPUTERS:

Apple Macintosh Personal Computers: Two Power Macintosh 8100s/100 with 16 MB RAM 1 GB hard disk, double-speed CD ROM drive and 17" Multiple Scan Display, one Power Macintosh 7500/100 with 16MB RAM, 1GB hard drive, quad-speed CD ROM drive and 17" Multiple Scan Display, one Mac Centris 650 with 16 MB RAM 230 MB hard disk, double-speed CD-ROM drive and basic color monitor; one Mac IIcx with 8 MB RAM and 345 MB hard disk, one Mac SE30 with 8 MB RAM and 40 MB hard disk, and one Mac SE with 4 MB RAM and 40 MB hard disk. The two Power Macintosh 8100s, one Power Macintosh 7500, one Centris 650, and an Apple Laserwriter IINT is connected to Internet through Ethernet. All three Power Macintoshes use System 7.5. An Appletalk network connects the other Macs together that allow file sharing through System 7.1.

IBM Personal Computers: IBM PC-AT personal computer with enhanced graphics board, high-resolution color monitor, hard disk, and printer. Includes ViewLogic software for schematic capture, simulation, waveform analysis, and fault grading.

TECHNICAL FACILITIES
SOFTWARE SYSTEMS

The lab houses the following computer-aided design tools:

COMPASS: COMPASS Design Automation Tools including a data path compiler, synthesis tools for data path logic, combinational logic, state machines, and BIST logic, a logic simulation tool, and a timing verification tool.
Hilo: GenRad's Hilo comprises logic and fault simulators and a test pattern generation.
LSI Logic: VLSI design tools. Includes VHDL and Verilog libraries.
Spice: Spice is an analog simulator for devices and circuits.
Synopsys: Logic synthesis tool set.
Syntest: A test pattern generation, and logic and fault simulation system for VLSI designs.
Vantage: VHDL simulator and intermediate format access tools.
Viewlogic: This is a schematic capture and a logic simulator that is also capable of injecting some faults in the design. The system is mainly used for logic design courses, and is hosted on the IBM PC-ATs.