VOLTAGE SCREENS FOR EARLY-LIFE FAILURES IN CMOS INTEGRATED CIRCUITS

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ABSTRACT

This thesis presents the results of a study of screens for detecting weak chips, and reducing intermittent failures and early-life failures. The three screens studied, both theoretically and experimentally, were VLV (Very-Low-Voltage), SHOVE (Short Voltage Elevation) and I_{DDQ}. The study aimed mainly at (1) identifying the defects for which each technique is effective and (2) determining the best parameters to be used when applying each technique.

VLV testing is a method where a test is performed at a supply voltage that is much lower than its nominal operating voltage. It can detect resistive shorts and delay flaws that are caused by degraded signals or diminished-drive gates. The supply voltage for VLV testing should be between $2V_t$ and $2.5V_t$, where V_t is the threshold voltage of a transistor. This conclusion was verified in a test chip experiment.

We also investigated the defects in CMOS domino circuits and derived the test conditions for them. VLV testing can improve the defect coverage, which we define as the maximum detectable resistance, of intra-gate and inter-gate resistive shorts for CMOS domino circuits.

SHOVE testing is a procedure of running stress vectors at higher-than-nominal supply voltage for a short period and performing Boolean or I_{DDQ} tests at nominal operating voltage afterwards. It is most effective for oxide and via defects. To stress circuits effectively without damaging good parts, the stress voltage should be 6 MV/cm $\times$ T_{ox}, where T_{ox} is the oxide thickness. Pseudo stuck-at test sets can put all transistors in a circuit in the most effective stress condition.

There are three major failure mechanisms in CMOS ICs: time-dependent dielectric breakdown (TDDB), hot carrier effects, and electromigration. SHOVE testing is effective for TDDB, VLV testing is effective for hot carrier effects and TDDB, and burn-in is effective for electromigration and TDDB.

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Introduction

1.1 Background

Integrated circuit (IC) manufacturers perform production tests to detect defective parts. We must test each IC thoroughly to guarantee the quality level of the product. Not only do field rejects require the additional cost of replacing the defective parts, they may also weaken customers' confidence in the product and eventually drive them away. Moreover, some defects may not cause circuits-under-test (CUTs) to malfunction when tested under normal operating condition. These defects may cause the circuits to malfunction early in the product's lifetime or to fail intermittently. To ensure IC quality, we must detect the defects (flaws) that cause early-life failures or intermittent failures. This thesis presents the results of a study of screens for detecting weak chips and reducing intermittent failures and early-life failures. The three screens studied, both theoretically and experimentally, were VLV (Very-Low-Voltage), SHOVE (Short Voltage Elevation) and I_{DDQ}. The study aimed mainly at (1) identifying the defects for which each technique is effective and (2) determining the best parameters to be used when applying each technique.

Weak ICs contain *flaws* [Hao 93a], defects that do not cause functional failures at some or all normal operating conditions but degrade the ICs performance, reduce noise margins, or draw excessive supply current. Hao and McCluskey showed that weak ICs cause problems with reliability and must be detected [Hao 93a]. Although weak ICs may pass production tests, they can fail to work in the field at different operating conditions, thus causing intermittent failures. Furthermore, weak ICs may consume extra power if the defect causes an abnormal static current flow, which makes them unacceptable for low-power applications. However, the detectability of these defects depends on the test conditions. A general survey of various testing techniques for detecting weak CMOS ICs appears in [Hao 93a].

Burn-in has been used to eliminate early-life failures for commercial and military ICs [Hnatek 95]. However, burn-in is very expensive because it requires burn-in equipment and delays product delivery.

Quiescent power supply current (I_{DDQ}) testing was proposed in early 1980s [Levi 81]. I_{DDQ} testing measures the quiescent power supply current of a CMOS IC. Each

circuit-under-test (CUT) must be set to a quiescent state before each current measurement. The theory of I_{DDQ} testing is straightforward. A defect-free static CMOS circuit draws large current only when it is switching. During a quiescent state, the current flowing through the CUT is mostly leakage and is usually very small. A CUT that has defects, such as resistive shorts, can have higher I_{DDQ} measurements than a defect-free CUT. Researchers have reported that I_{DDQ} testing significantly improves the quality and decreases the production cost of state-of-the-art CMOS ICs [Soden 95].

However, I_{DDQ} testing has several drawbacks. The test speed for an I_{DDQ} test is much slower than that for a Boolean test. In addition, I_{DDQ} tests require different fixtures from the ones used for Boolean tests. It is also difficult to set the threshold for I_{DDQ} testing: experimental data have shown that there is a continuous distribution for I_{DDQ} values [Sematech 97] [Chang 98]. Moreover, for deep submicron technologies, the quiescent currents of defect-free CUTs increase significantly due to high subthreshold leakage [Soden 96]. Furthermore, I_{DDQ} testing becomes ineffective if the background currents become too high. Finally, the most serious problem for I_{DDQ} testing is the yield loss associated with it. Researchers have reported 1-3% [Hnatek 95] or 3-5% [Sematech 97] yield loss for I_{DDQ} testing. Corresponding yield loss from I_{DDQ} fail-only ICs can range from millions of dollars to over a billion dollars per year for expensive, high-volume ICs [Soden 96]. Depending on the current threshold for I_{DDQ} testing, the percentage of I_{DDQ} fail-only ICs can vary from 1% to 100% of those ICs that pass all Boolean tests at normal operating voltage. Because of the continuous distribution for I_{DDQ} values, it is difficult to determine an acceptable current threshold without substantial revenue loss caused by rejecting I_{DDQ} fail-only ICs. Depending on the applications, the IC suppliers and customers determine the acceptable yield loss. For applications such as space missions that require high-reliability ICs, the rejected I_{DDQ} fail-only ICs may not be referred as yield loss. On the other hand, for consumer products such as video game stations, the rejected I_{DDQ} fail-only ICs are usually counted as yield loss because the otherwise-shipped ICs reduce the revenue.

1.2 Contributions

Two voltage screens, VLV testing and SHOVE testing, were thoroughly investigated. They can be used as alternatives to burn-in and I_{DDQ} testing or to reduce the number of parts packaged and burned in. *VLV testing* is a method where a test is performed at a supply voltage that is much lower than its nominal operating voltage. *SHOVE testing* is a procedure of running stress vectors at higher-than nominal supply

voltage for a short period and performing Boolean or I_{DDQ} tests at nominal operating voltage afterwards. VLV testing and SHOVE testing aim at screening early-life failures and intermittent failures so that we can improve the quality level of CMOS ICs at low cost. We also studied methods to detect flaws in CMOS domino circuits. Finally, we provided experimental data for VLV testing based on the test results of the final package test of the MURPHY test chip experiment.

VLV testing and SHOVE testing can be used as wafer-level reliability screens. For some applications, such as multi-chip module (MCM) designs, it is desired that we can apply reliability screens at the wafer level so that we can improve the quality level of known good dies (KGD). In addition, if we can detect the weak parts during a wafer-level test, we can avoid the cost of packaging them. However, it is very difficult and expensive to perform burn-in at the wafer level. On the other hand, VLV testing and SHOVE testing do not require special test hardware. The test conditions for VLV testing and SHOVE testing can be achieved by using the automatic test equipment (ATE) for production tests. Moreover, VLV testing and SHOVE testing do not require extensive test time.

Hao and McCluskey investigated the voltage dependence of two major causes of weak ICs, resistive shorts and threshold voltage shifts, and proposed VLV testing [Hao 93a]. Based on the difference of the electrical characteristics at different supply voltages, VLV testing can detect some flaws that are undetectable at the normal supply voltage. The experimental results in [Ma 95a] indicated that VLV testing detected some suspect dies that passed normal voltage tests and current tests. Researchers have shown that VLV testing is also valid for analog testing. Bruls applied VLV testing to test a class AB amplifier developed in a 1.0 μm double metal CMOS technology and a bipolar ring oscillator manufactured in a BiCMOS process [Bruls 94].

We analyzed the supply voltage for VLV testing by considering the flaw coverage, test time, and noise margin. We found that the supply voltage for VLV testing should be as low as $2V_t$ to $2.5V_t$, where V_t is the threshold voltage of a transistor. We also investigated the issues for determining the test speed for VLV testing. The test speed at low voltage should be characterized carefully to ensure the effectiveness of VLV testing and to avoid failing good devices. One can perform a cycle-time-to-voltage Shmoo for a good device to determine the test speed for VLV testing. Moreover, we found that VLV testing is effective in detecting delay flaws in CMOS ICs. VLV testing is most effective when the failure modes of the timing defects are either degraded signals or diminished-drive gates. However, it is not effective for high-resistance interconnects.

SHOVE testing has been widely practiced in industry [Crook 79] [Kowalczyk 90] [Duey 93] [Josephson 95]. During SHOVE, test sets such as single stuck-at or pseudo stuck-at test sets, are run at higher-than-normal supply voltage for a short period. Some defects that occur after SHOVE can only be detected by functional tests and some can only be detected by I_{DDQ} tests. Thus, both functional tests and I_{DDQ} tests should be performed at normal operating voltage after SHOVE. It has been found that I_{DDQ} values of some CUTs increase significantly after SHOVE [Duey 93] [Josephson 95]. VLV testing can be used after SHOVE if the background current is too high to perform I_{DDQ} testing. It can also detect the oxide defects accelerated by SHOVE. Some data that show the correlation between the effectiveness of burn-in and SHOVE testing were reported recently [Barrette 96] [Kawahara 96]. However, no detailed analysis has been found in any published literature. We performed a theoretical study of SHOVE testing. SHOVE testing is most effective for oxide and via defects. To stress CUT effectively without damaging the good parts, the stress voltage should be no more than 6MV/cm $\times$ T_{ox}, where T_{ox} is the oxide thickness of each technology. Pseudo stuck-at test sets can put all transistors in a CUT in the most effective stress condition.

CMOS domino circuits are popular in speed-critical designs because they switch faster and use smaller area than static CMOS circuits [Krambeck 82] [Gronowski 96a] [Choudhury 97] [Jain 97]. Researchers have studied testability of CMOS domino circuits. However, most previous work used transistor stuck-on and stuck-open models [Barzilai 84] [Oklobdzija 84] [Wunderlich 86] [Jha 88] [Jha 90] [Bruni 92]. Renovell and Figueras investigated I_{DDQ} testability of CMOS domino circuits based on the low-resistance inter-gate short model [Renovell 93]. However, they did not consider the leakage current caused by the dynamic node in a CMOS domino circuit. Ma analyzed the fault effects of intra-gate resistive shorts in CMOS domino circuits [Ma 95b]. However, Ma presented only the results for shorts with resistance less than 2 KΩ. We studied intra-gate resistive shorts, inter-gate resistive shorts, and defects in the keepers and internal prechargers that are used to ensure the correct functionality of CMOS domino circuits.

We performed several test chip experiments whose goal was to evaluate the effectiveness of different test techniques. The test results from the final package test of the MURPHY test chip experiment will be presented in Chapter 6. They include the experimental results for I_{DDQ} testing and VLV testing.

The contributions of this dissertation are summarized as follows:

- We show that VLV testing can detect delay flaws caused by either degraded signals or diminished-drive gates .
- We show that the supply voltage for VLV testing should be $2V_t$ to $2.5V_t$.
- We show methods to determine the test speed of VLV testing.
- We show that SHOVE testing can detect oxide defects.
- We derived the parameters, such as stress voltage, stress vectors, and stress time, for SHOVE testing.
- We present a new keeper design for small CMOS domino circuits.
- We present methods to detect flaws in CMOS domino circuits.
- We have performed the final package test for the MURPHY test chip experiment and shown the test results for I_{DDQ} testing and VLV testing.

1.3 Outline

This dissertation summarizes my work in testing early-life failures for CMOS ICs. Detailed descriptions and experimental results of the proposed techniques can be found in the appendices, which include the published papers.

This dissertation is organized as follows. Chapter 2 discusses the supply voltage and test speed of VLV testing for detecting resistive shorts in static CMOS ICs. The supply voltage for VLV testing should be $2V_t$ to $2.5V_t$ to detect up to 5 KΩ for resistive shorts for the technologies used in the study. The supply voltage study considers the tradeoffs among flaw coverage, test time, and noise margin.

Chapter 3 describes the effectiveness of VLV testing for detecting delay flaws in static CMOS ICs. A *delay flaw* is a defect that causes a local timing failure but this failure is not severe enough to make a circuit fail at nominal operating condition. Delay flaws caused by degraded signals and gates with lower drive capability than expected are considered. This chapter investigates the voltage dependence of the effects of delay flaws and derives the test conditions for them.

Chapter 4 investigates defects in CMOS domino circuits and derives test conditions for them. The defects include intra-gate resistive shorts, inter-gate resistive shorts, missing keepers, and missing internal prechargers. VLV testing can improve the *defect coverage*, which we define as the maximum detectable resistance of intra-gate and inter-gate resistive shorts. We can also improve the defect coverage of inter-gate

resistive shorts by increasing the supply voltage to be about 40% higher than the normal operating voltage. Missing internal prechargers can be detected by running 100% single stuck-at test sets at high voltage. We also propose a new keeper design for CMOS domino circuits. The new keeper design has low performance impact and is most useful for small CMOS domino circuits. Keepers can eliminate the floating nodes in CMOS domino logic gates. Missing keepers can be detected by testing CUTs slowly if all CMOS domino circuits in the CUTs have keepers.

A stress procedure for reliability screening, the SHOrt Voltage Elevation (SHOVE) test, is analyzed in Chapter 5. During SHOVE, test vectors are run at higher-than-normal supply voltage for a short period. Functional tests and I_{DDQ} tests are then performed at the normal voltage. This procedure is effective in screening oxide thinning, which occurs when the oxide thickness of a transistor is less than expected, as well as via defects. The issues of SHOVE testing include stress voltage, stress vectors, and stress time. Chapter 5 addresses these issues in details. We show that the stress voltage of SHOVE testing should be set such that the electric field across an oxide is approximately 6 MV/cm. The stress time can be calculated by using the "effective oxide thinning" model. The chapter also discusses the requirements on input vectors for stressing complementary CMOS logic gates and CMOS domino logic gates efficiently.

An experimental test chip was designed and manufactured to evaluate different test techniques. Based on the results obtained in the wafer probe, 309 out of 5491 dies that passed the Stage 1 tests were packaged for further investigation. Chapter 6 describes the experimental setup and the experimental results for the final package test. We focused on the correlation among various defect classes, including I_{DDQ} failures, VLV failures, timing-independent combinational (TIC) defects, and non-TIC defects. The I_{DDQ} values of all CUTs have a continuous distribution. Consequently, it is difficult to set the current threshold. We used two supply voltages for VLV tests. Two test speeds were used at each supply voltage. 9 dies failed only the VLV Boolean tests, and 7 of these were confirmed to have high I_{DDQ} measurement results. Some timing-dependent failures became TIC defects at very low voltage.

Chapter 7 concludes the dissertation.

Chapter 2

Quantitative Analysis of Very-Low-Voltage Testing

Very-Low-Voltage (VLV) testing is a technique for detecting weak CMOS ICs [Hao 93a]. However, the supply voltage and test speed for VLV testing must be carefully determined in order to minimize test escapes and type-one errors (yield loss). This chapter presents a methodology for determining the supply voltage and test speed for VLV testing. A detailed discussion and results can be found in Appendix A.

The supply voltage study investigates the tradeoffs among three items: the flaw coverage, test time, and noise margin. *Flaw coverage* is the detectable range of a defect, such as the detectable resistance of a resistive short. This chapter focuses on resistive shorts, such as gate oxide shorts and metal shorts. Chapter 3 discusses the application of VLV testing to timing failures, such as threshold voltage shifts and delay flaws. A circuit has a *delay flaw* if there is a timing failure but the circuit continues to work at the designed speed [Franco 94b].

Based on the results of a thorough analysis, we conclude that the supply voltage for VLV testing for the technologies used in this study should be set at $2V_t$ to $2.5V_t$ where V_t is the threshold voltage of a MOS transistor. The test speeds must be carefully adjusted at very low voltages in order to avoid type-one errors. We can determine the test speed at each voltage by generating cycle-time-to-voltage Shmoo plots.

This chapter describes the supply voltage study for VLV testing based on the flaw coverage of resistive shorts, the test time, and the noise margin. We also shows the application of VLV testing to low-voltage technologies.

2.1 Supply Voltage

This section shows that the supply voltage for VLV testing should be between 2 and 2.5 times the threshold voltage V_t of the transistors for the technologies used in this study, which include MOSIS HP CMOS26B 0.8 μm technology, MOSIS HP CMOS14TB 0.6 μm technology, and a 0.25 μm low-voltage technology. This section presents the tradeoffs among the flaw coverage, test time, and noise margin at various supply voltages. For other technologies, the same techniques should be used to obtain the appropriate value for the supply voltage.

2.1.1 Flaw Coverage

Researchers have shown that the resistance of a short may change with time and cause reliability problems for CMOS ICs [Hawkins 85] [Hao 91a]. This section considers two kinds of resistive shorts, gate oxide shorts and metal shorts. We discuss the application of VLV testing to timing failures in Chapter 3.

Gate Oxide Shorts

The analysis shown here is based on NMOS gate oxide shorts, which are unexpected connections between the gate and the drain, source, or channel (substrate, p-well, n-well) in an NMOS transistor that are caused by pinholes in the gate oxide layer. A detailed discussion of the voltage dependency of PMOS gate oxide shorts can be found in Appendix A.

Hao and McCluskey showed that NMOS gate oxide shorts can be modeled as resistive shorts [Hao 91b]. Figure 2-1 shows a NAND gate with a gate-to-source short in the NMOS transistor M3. Figure 2-2 shows the relationship between the resistance of a defective MOS transistor and the supply voltage for a 0.8 μm technology. The nominal supply voltage for this technology is 5V. *The resistance of a defective MOS transistor* is measured as the voltage drop between the drain and source divided by the current flowing into the drain when a short exists within a transistor and the gate voltage of the transistor is set to a high voltage. This definition can only be used to determine the resistance of a defective MOS transistor at a steady state. It cannot be used to determine the AC behavior of a defective MOS transistor.

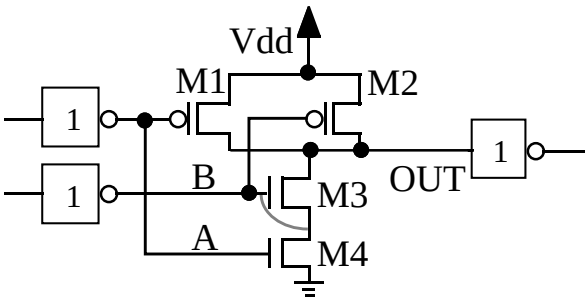

Figure 2-1 NMOS Gate Oxide Short

The supply voltage shown in Fig. 2-2 is scaled by the threshold voltage of an NMOS transistor. The transistor used in Fig. 2-2 is the NMOS transistor M3 of the NAND gate shown in Fig. 2-1. In Fig. 2-2, the resistance of the resistive short varies from 1 KΩ to 5 KΩ. A similar simulation setup and results for a 0.6 μm technology can be found in Appendix A.

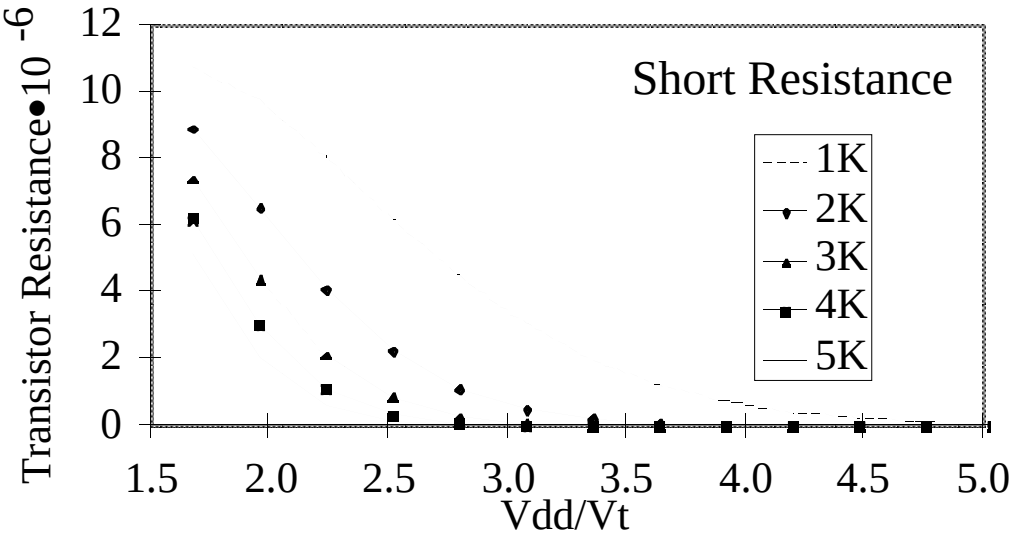

Figure 2-2 The Equivalent Resistance of a Defective NMOS Transistor for a 0.8 μm Technology

When there is an unexpected connection between gate and source (or drain) of a transistor, the gate voltage becomes an intermediate value between the supply voltage and ground. The transistor stays in either the saturation region or triode region. Therefore, the resistance of a transistor increases as the supply voltage is reduced. Moreover, the gate voltage is lower when the resistance of the short is lower, which reduces the current flowing through the transistor. On the other hand, the short's resistance remains almost the same at different voltages. Hence, we can observe the fault effect of a gate oxide short at a reduced voltage [Hao 93a] [Bruls 94]. As shown in Fig. 2-2, a MOS transistor has a nonlinear resistance, which increases monotonically as the supply voltage decreases. The improvement of the flaw coverage of the defect strongly depends on how much the resistance of a transistor increases at a reduced supply voltage. The more the resistance of a transistor increases, the more a resistive short affects the CUT. The result is that the electrical characteristics of a faulty gate change significantly at very low voltage. It is not necessary for the defect resistance to be a constant. VLV

testing can still detect a resistive short if the resistance of the short increases at a lower rate than the resistance of a transistor does as the supply voltage is reduced [Hao 93a].

Figure 2-2 shows that the resistance of an NMOS transistor with the short's resistance larger than 2 KΩ starts to increase significantly when the supply voltage is approximately between $2V_t$ and $2.5V_t$. Hence, to detect a high-resistance gate oxide short, we must reduce the supply voltage until it is low enough to make the resistance of a transistor change significantly. Table 2-1 lists the flaw coverage of the short for the circuits shown in Fig. 2-1 and an adder based on the 0.8 μm technology. The adder design can be found in Appendix A. The results in Table 2-1 show that VLV testing is effective for both basic and complex gates.

Hawkins and Soden showed that the resistance of a gate oxide short could be as high as 4.7 KΩ [Hawkins 85]. To detect an NMOS gate oxide short with resistance of 5 KΩ, the supply voltage should be as low as 1.6V, which is $2.25V_{tn}$. Detailed simulation results and discussion can be found in Appendix A.

Table 2-1 The Flaw Coverage of an NMOS Gate Oxide Short by Boolean Tests (0.8 μm Technology, V_{tn} = 0.71V)

Supply Voltage		Flaw Coverage	
V_{dd}	V_{dd} / V_{tn}	NAND Gate	Adder Cells
1.4V	1.97	≤ 10 KΩ	≤ 8 KΩ
1.6V	2.25	≤ 6 KΩ	≤ 5 KΩ
1.8V	2.53	≤ 5 KΩ	≤ 3.5 KΩ
2.0V	2.81	≤ 4 KΩ	≤ 2 KΩ
3.0V	4.22	≤ 2 KΩ	≤ 1 KΩ
5.0V	7.03	≤ 1 KΩ	≤ 0.5 KΩ

Based on these results, we suggest that the supply voltage of VLV testing be $2V_t$ to $2.5V_t$ for NMOS gate oxide shorts. The supply voltage can be adjusted within this range to accommodate other considerations. A detailed discussion for PMOS gate oxide shorts can be found in Appendix A.

Metal Shorts

Metal shorts are unexpected metal connections between two nodes. We determined the supply voltage for VLV testing based on the improvement of the flaw coverage of a metal short effected by different voltages. As in the case of gate oxide

shorts, the supply voltage for VLV testing should be set in the range in which the equivalent resistance of a transistor increases significantly.

Figure 2-3 shows the simulation setup. The gray line that connects the outputs of gates x1 and x3 represents a resistive short with resistance R_S. Two sets of simulations were done. For the first, the inverters in both inverter chains have the same size. For the second, each inverter in the bottom inverter chain was sized to be four times bigger than the corresponding inverter in the upper inverter chain. Table 2-2 shows the simulation results for the 0.8 μm technology.

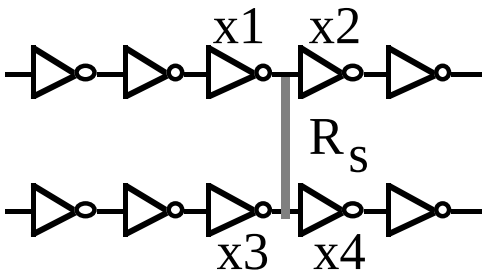

Figure 2-3 A Metal Short

Table 2-2 Flaw Coverage of a Metal Short by Boolean Tests (0.8 μm Technology, V_{tn} = 0.71V, V_{tp} = - 0.90V)

Supply Voltage			Flaw Coverage	
V_{dd}	V_{dd}/V_{tn}	$V_{dd}/\|V_{tp}\|$	Same Size	Different Size
1.4V	1.97	1.56	≤ 6 KΩ	≤ 6.5 KΩ
1.6V	2.25	1.78	≤ 4 KΩ	≤ 5 KΩ
1.8V	2.53	2.00	≤ 2 KΩ	≤ 3 KΩ
2.0V	2.81	2.22	≤ 1 KΩ	≤ 2 KΩ
3.0V	3.51	2.78	≤ 0.5 KΩ	≤ 1 KΩ
5.0V	7.03	5.55	≤ 0.5 KΩ	≤ 0.5 KΩ

The results show that the flaw coverage of a metal short that connects two gates of different sizes is larger than the flaw coverage of one that connects two gates of the same size. We will only discuss the case that has a metal short connecting gates of different sizes. Moreover, the results also show that the flaw coverage of a metal short improves to 5 KΩ when the supply voltage is 1.6V for the 0.8 μm technology, which is $2.25V_{tn}$. Researchers have shown that 98.3% of resistive shorts are below 5 KΩ [Rodriguez 92]. Consequently, the supply voltage for VLV testing should be in the

range of $2V_t$ and $2.5V_t$, where V_t is the lower of V_{tn} or $|V_{tp}|$. Appendix A includes similar results for a 0.6 μm technology.

2.1.2 Test Time

The propagation delay of a CMOS gate becomes much longer at a reduced supply voltage. While reducing the supply voltage can improve the flaw coverage, it also increases the test time. Consequently, the supply voltage should not be arbitrarily small.

Although the propagation delay increases monotonically as the supply voltage is reduced, the propagation delay of a CMOS gate does not change very much for a wide range. Figure 2-4 shows the propagation delay of an inverter at different voltages for two different technologies. If the supply voltage is selected so that it is around the value where the propagation delay starts to change significantly, not only can we improve the flaw coverage, but we can also keep the test time cost as low as possible for VLV testing. Figure 2-4 shows that the propagation delay of a CMOS inverter starts increasing significantly at around 1.5V for the 0.8 μm technology, which is $2.11V_{tn}$, and 1.3V for the 0.6 μm technology, which is 2.20 V_{tn}. As a result, the supply voltage proposed above is also valid as far as the test time is concerned.

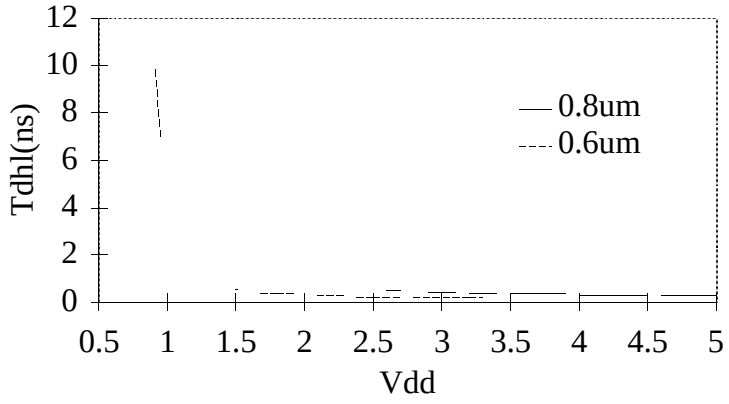

Figure 2-4 Propagation Delay of a CMOS Inverter

2.1.3 Noise Margin

Appendix A includes a detailed discussion of the noise margin. Relative noise margins improve at low voltage because V_t / V_{dd} increases [Burr 93]. As discussed in [Burr 93], internal noise scales at least as fast as the supply voltage. For long channel devices, capacitive coupling noise scales as V_{dd}, resistive coupling noise scales as V^2_{dd},

and inductive coupling noise scales as V^3_{dd}. For short channel devices, capacitive, resistive, and inductive coupling noise all scale as V_{dd}. Relatively, the internal coupling noise does not get worse at low voltage.

Unlike coupling noise, thermal noise does not scale at different voltages. Burr showed that the thermal noise is as small as 100μV [Burr 93]. Practically, thermal noise is not a concern when the supply voltage is above 1V.

However, the results of VLV testing are sensitive to external noise. Because absolute noise margins decrease at low voltage, the testing environment must be controlled so that external noise is isolated. The supply voltage must be larger than the magnitude of external noise.

2.1.4 Supply Voltage for VLV Testing

Based on previous discussions, the supply voltage for VLV testing should be set in the range of $2V_t$ to $2.5V_t$ for the technologies used in this study, where V_t is the lower of V_{tn} or $|V_{tp}|$. The supply voltage used in [Ma 95a] for VLV testing is in the range proposed in this dissertation. In [Ma 95a], the supply voltage was selected by doing a Shmoo plot on a good die, and 1.7V was chosen after both noise and test time had been considered. The results published in [Ma 95a] indicated that there were some dies that failed only VLV testing. In [Chang 98], we presented a detailed analysis of these dies.

2.2 Determining the Test Speed

The relationship between the test speed and supply voltage depends on how the critical path delay of a circuit changes as the supply voltage is changed. Some researchers have studied this relationship [Horowitz 94] [Wagner 86]. Horowitz *et al.* showed that the delay-voltage relationship of a CMOS circuit is predictable. They used circuits of various sizes to show that CMOS circuits with the same process technology have similar speed-voltage scaling ratios. The maximum deviation is within 15%. The *delay-voltage scaling ratio* is the ratio between the propagation delay at any voltage and that at the normal operating voltage.

However, because the threshold voltages of NMOS and PMOS transistors are different for some technologies, the delays of rising and falling transitions may scale differently as the supply voltage decreases. To predict the circuit speed at different voltages more accurately, the delays of rising and falling transition should be scaled by different delay-voltage scaling ratios.

As technologies scale, the interconnection delay becomes important. Wagner and McCluskey showed that, unlike the gate delay, the interconnection delay of an integrated circuit is independent of the supply voltage [Wagner 86]. Because of the difference between the delay-voltage scaling ratios of the CMOS gate delays and the interconnection delays, the critical paths may be different at different supply voltages if there are other paths whose delays are shorter but are similar to the delays of the critical paths at the normal operating voltage.

To achieve good flaw coverage, the test speed for VLV testing must be determined accurately. Because interconnect delay may become more significant for deep submicron technologies, the test speed selection should not ignore the existence of interconnect delay. In addition, as ICs become denser and more complicated, it is more difficult to predict the test speed at different voltages theoretically or by simulations. Therefore, in order to ensure test quality, more characterizations of CUTs at low voltage, such as Shmoo plots, are necessary to determine the test speed of VLV testing.

2.3 VLV Testing for Low-Voltage Technologies

One of the trends in today's IC market is to reduce the supply voltage [Burr 93] [Davari 95]. The effectiveness of VLV testing is based on the observation that the difference between the electrical characteristics of a faulty circuit and that of a fault-free circuit can be made more pronounced by reducing the supply voltage. It has been shown that this difference gets more significant as the supply voltage approaches the threshold voltage of a MOS transistor. Sec. 2.1 has shown that the supply voltage for VLV testing should be in the range of $2V_t$ to $2.5V_t$. For high-performance CMOS designs, the threshold voltage is reduced so that the designs will not have severe speed degradation [Mii 94] [Davari 95]. Mii *et al.* showed that there will be excessive delays if $V_t > V_{dd}/4$.

We studied VLV testing for a low-voltage technology, whose normal operating voltage is 1V to 1.5V. The technology has two different processes. One has a normal threshold voltage, around 0.5V. The other one has an ultra-low threshold voltage, around 0.25V. By setting the supply voltage at $2V_t$, the flaw coverage of the defects shown in Fig. 2-1 and in an adder can be summarized in Table 2-3. For an AC test, we assume that a short is detectable if the propagation delay of a defective gate is more than three times that of a defect-free gate. Table 2-3 shows that VLV testing can detect resistive shorts for a low-voltage technology. The static current of an inverter is 0.79nA for the process with a normal threshold voltage and 0.93μA for the process with a low threshold voltage.

For a million-gate chip, the background current can be as high as 0.93A for the process with a low threshold voltage.

Table 2-3 The Flaw Coverage of a Resistive Short for a Low-Voltage Technology When $V_{dd}=2V_t$

	Short in Fig. 2-1		Short in an adder	
Technology	DC Test	AC Test	DC Test	AC Test
Low V_t	≤ 1.2 KΩ	≤ 1.6 KΩ	≤ 1 KΩ	≤ 1.5 KΩ
Normal V_t	≤ 1.6 KΩ	≤ 2.6 KΩ	≤ 1 KΩ	≤ 1.5 KΩ

2.4 Summary

We have shown that the supply voltage for VLV testing should be in the range of $2V_t$ to $2.5V_t$ for the technologies used in the study presented in this chapter. The supply voltage can be adjusted within this range to accommodate practical considerations, such as the magnitude of the external noise around the test environment. We also investigated the effectiveness of VLV testing for low-voltage technologies. By using $2V_t$ as the supply voltage during testing, we found reasonable defect coverage for gate oxide shorts and metal shorts. The static current for the low-voltage technology is too high to perform a current test.

VLV testing is effective for detecting flaws that cause early-life failures and intermittent failures. It does not add to the cost of an IC in either area or performance. Furthermore, it is non-destructive to a circuit-under-test and does not require a waiting time such as is typical for burn-in.

Chapter 3

Detecting Delay Flaws by Very-Low-Voltage Testing

Timing failures occur when the delay of the manufactured component is different from the designed delay [Franco 94b]. This chapter considers the effectiveness of VLV testing in detecting timing failures. A circuit has a delay flaw (a non-operational delay fault) if it has a timing failure but continues to work at the designed speed [Franco 91] [Franco 94b]. Although delay flaws may not fail the circuits at normal operating conditions, they may cause problems if the supply voltage changes during operations due to IR drops or simultaneous switching noise [Bakoglu 90]. Some delay flaws, such as threshold voltage shifts, indicate reliability problems of CUTs. Therefore, delay flaws can cause early-life and intermittent failures, and need to be detected. This chapter will first discuss the timing failure modes and then analyze how VLV testing can help detect these timing failures.

A delay flaw is different from a *delay fault* (an operational delay fault), which is a timing failure that makes a circuit fail to work at the designed speed but to be functional at a slower speed [Franco 91] [Franco 94b]. There are several definitions for delay faults. We use the definition described above. Most studies of testing timing failures concentrate on the detection of delay faults. However, some timing failures that are embedded in short paths may not cause delay faults at normal operating conditions.

Table 3-1 lists the causes of timing failures and the possible testing techniques for detecting them. Although all of these failures may be detected by delay fault testing, the success of detection depends on the significance of the excessive delay in the defective circuit. VLV testing can enhance the significance of the excessive delays for some of the listed causes and thus improve their detectability. This chapter discusses this table in depth.

A *degraded signal* is a signal whose V_{IH} is lower than the supply voltage or whose V_{IL} is higher than the ground voltage level. A *slow-to-rise* (*slow-to-fall*) signal has a longer rise (fall) time than designed. The timing failure modes can be degraded signals, slow-to-rise signals, slow-to-fall signals, or increased propagation delays. A gate driven by a degraded signal will have an increased delay. Because most timing failures can be either directly or indirectly caused by degraded signals or by gates with lowered

driving strengths, we focused on the delay flaws caused by these two failure modes. We first investigate the voltage dependence of the propagation delay of a CMOS inverter. Weakly-driven (WD) gates have no internal defects but their inputs are driven by degraded signals. Theoretical analysis shows that the ratio of the delay of a WD gate with a degraded signal at its input to that of a fault-free gate increases significantly when the supply voltage is reduced to between $2V_t$ and $2.5V_t$. This conclusion is also valid for the case when the CUT has diminished driving capability. We verified these findings for both failure modes by investigating the delay flaws caused by transmission gate opens, threshold voltage shifts, and diminished-drive gates.

Table 3-1 Testing Techniques for Timing Failures

Causes at transistor level	Detected by		
Transmission gate opens	V*	D**	
Threshold voltage shifts	V	D	
Diminished-drive gates	V	D	
Gate oxide shorts	V	D	I***
Metal shorts	V	D	I
Defective interconnect buffers	V	D	I
High resistance interconnects, via defects		D	
Tunneling opens		D	

* VLV Testing, **Delay Fault Testing, ***IDDQ Testing

3.1 Causes and Failure Modes of Timing Failures

Table 3-1 lists the causes of timing failures. Transmission gate opens occur when one of the transistors in a CMOS transmission gate is malfunctioning and cannot pass any signals. The output of a transmission gate with a transmission gate open can be a degraded signal. The gate following this defective transmission gate is weakly driven and thus has an excessive propagation delay. Hot carrier effects and process variations can result in threshold voltage shifts, which make transistors have smaller transconductance and lower driving strengths [Hu 85] [Leblebici 93]. The propagation delays of gates with threshold voltage shifts increase. Moreover, the outputs of these gates have slow-to-fall signals because the effects of threshold voltage shifts are more serious in NMOS transistors. Some CMOS gates with high driving strength consist of

two or more smaller gates connected in parallel. These gates will have lower driving strength if one or more of the gates connected in parallel are broken and cannot pass any signals. CMOS gates can also be weakened if the gate widths become narrower due to either spot defects or process imperfections. The output of the diminished-drive gate will have slow-to-rise or slow-to-fall signals. Also, the propagation delay of the defective gate increases. Spot defects can cause gate oxide shorts [Hawkins 85], unexpected conducting shorts, or narrowed interconnects. Gate oxide shorts and unexpected conducting shorts can cause degraded signals and can increase leakage currents in CUTs.

For deep submicron technologies, the interconnect delay is no longer negligible. Buffers are sometimes added to reduce the long interconnect delay. If the buffers are defective, they may cause different failure modes depending on the type of defects. They may have internal resistive shorts, which can cause degraded signals, high leakage current, longer gate delays, or longer interconnect delays. If open faults occur in the buffers, signals may not be able to pass through the buffers and, thus, cannot pass through the long interconnects either.

Via defects, stress voids, and electromigration can increase the resistance of an interconnect and thus cause a longer RC delay along the interconnect [Hnatek 95]. The signal propagating in a higher-resistance interconnect may be slow-to-rise or slow-to-fall. Tunneling opens allow CUTs to be functional at low frequencies but cause failures at higher frequencies [Henderson 91]. Table 3-2 summarizes the failure modes of the timing failures described above.

This chapter discusses how VLV testing can improve the detectability of timing failures that are caused by degraded signals and by transistors with lowered driving capabilities. Gate oxide shorts and metal shorts have been discussed in Chapter 2. Defective buffers in long interconnects can have the same defects that occur in logic gates. Thus, depending on the failure modes, VLV testing, I_{DDQ} testing, or delay fault testing can be used to detect them. On the other hand, due to the fact that RC delays do not scale when the supply voltage is reduced [Wagner 85], VLV testing is inadequate for detecting high-resistance interconnects. Instead, high resistance interconnects must be detected by delay fault testing at normal operating voltage.

Since CUTs with tunneling opens can only be functional at very low frequencies (close to DC) [Henderson 91], they behave similarly to stuck-open faults. Thus, tunneling opens are gross delay faults and cannot cause delay flaws. This chapter focuses on the first three items in Tables 3-1 and 3-2.

Table 3-2 Failure Modes of Timing Failures

Causes	Failure Modes
Transmission gate opens	Degraded signals
Threshold voltage shifts	Increased gate delays Slow-to-fall signals
Diminished-drive gates	Increased gate delays Slow-to-rise signals Slow-to-fall signals
Gate oxide shorts	Degraded signals Increased leakage
Metal shorts	Degraded signals Increased leakage
Defective interconnect buffers	Degraded signals Increased gate delays Increased RC delays Increased leakage Opens
High resistance interconnects, via defects	Increased RC delays Slow-to-rise signals Slow-to-fall signals
Tunneling opens	CUT fails at high frequencies

3.2 Voltage Dependence of CMOS Propagation Delay

VLV testing is most effective in detecting delay flaws when the supply voltage is around the value where the propagation delay of a circuit starts to change significantly as the supply voltage is reduced. Although VLV testing can detect more flaws as the supply voltage is reduced, the test time becomes much longer and the noise margin is reduced significantly if the supply voltage is further reduced [Chang 96a]. Moreover, fault-free circuits should be still functional at the selected voltage. Hence, the supply voltage for VLV testing should be set so that the improvement of the flaw coverage is significant but the test time will not be unreasonably long and fault-free circuits can still be functional.

Appendix B presents a detailed discussion for the voltage-dependence of the propagation delay of a CMOS logic gate. Equation 3-1 is a first-order estimation of the

relation between the propagation delay T_d and the supply voltage of an inverter. This equation was also used in [Chandrakasan 92]. Appendix B also includes a comparison between the simulation result and the calculated value of the propagation delay of a CMOS logic gate. However, Equation 3-1 is not applicable if a transistor's velocity is saturated. At a much-lower-than-normal supply voltage, the velocity saturation in a transistor can disappear even though it may exist at the nominal supply voltage because the electric field in the channel of a transistor reduces when the supply voltage is lowered. Consequently, the overall conclusion of this study is also applicable if a transistor's velocity is saturated at nominal supply voltage.

$$Td = \frac{CL \times Vdd}{\mu Cox(W/L)(Vdd - Vt)^2} = K\frac{Vdd}{(Vdd - Vt)^2} \qquad \textbf{Equation 3-1}$$

If the input signal of a CMOS inverter is decreased from V_{dd} to V_{dd} / a, as shown in Fig. 3-1, the propagation delay T_{WD} of the weakly-driven inverter can be approximated by using Equation 3-2, in which a is a number greater than one, T_d (V_{dd} / a) is the propagation delay of the inverter at V_{dd} / a, and K is the same constant used in Equation 3-1.

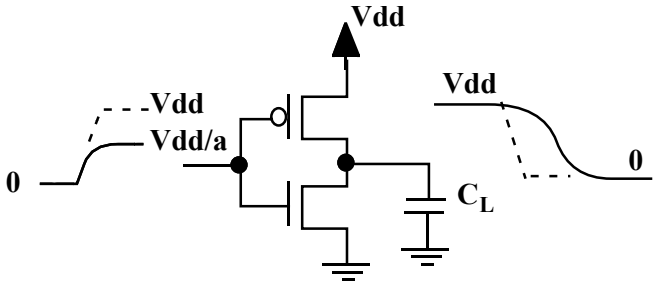

Figure 3-1 Effect of a Degraded Signal

$$T_{WD}(Vdd) = K\frac{Vdd}{(Vdd/a - Vt)^2}$$
$$= aK\frac{Vdd/a}{(Vdd/a - Vt)^2} = a \times Td(Vdd/a) \qquad \textbf{Equation 3-2}$$

In Fig. 3-1, the solid lines represent the input and output signals of a WD gate and the dashed lines represent the same information for a fault-free gate. Based on Equation 3-2, the propagation delay of the WD gate can be approximated by the propagation delay of the inverter operating at V_{dd} / a multiplied by a. The *delay ratio* of a gate is the ratio of the delay of a faulty circuit to that of a fault-free circuit. The delay ratio of a WD gate is equivalent to the ratio of the delay of a fault-free circuit at V_{dd} / a to that of the same circuit at V_{dd} multiplied by a. In this case, the WD circuit is an inverter with a degraded signal at its input. Consequently, we can observe the voltage dependence of the propagation delay of a fault-free circuit to determine how the delay ratio of a CMOS gate changes at different voltages. This chapter focuses on WD gates. The conclusion should also be valid for threshold voltage shifts. The voltage dependency of the delay ratio of a diminished-drive gate is more complicated. Appendix B includes a detailed discussion for threshold voltage shifts and diminished-drive gates.

The *change rate* of the propagation delay at a voltage is the ratio of the propagation delay at the voltage to that at a slightly lower voltage. In this study, the change rate of the propagation delay at a specified voltage is measured by the ratio of the propagation delay at the specified voltage to that at a voltage that is lowered from the specified voltage by 0.2V. If the propagation delay of a fault-free gate does not change much at some voltages, the delay ratio of a WD gate and a fault-free gate will be insignificant. On the other hand, if the supply voltage is in the range where the propagation delay of a fault-free gate changes significantly, the difference will be larger. We use the change rate of the propagation delay of a CMOS gate to quantify how significantly the propagation delay changes at each voltage. The supply voltage for VLV testing for detecting delay flaws should be set in the region where the change rate of the propagation delay is significant. In this region, a small change in the supply voltage can cause a large change in the propagation delay. Consequently, the difference between the propagation delay of a WD gate and that of a fault-free gate is much more significant.

Figure 3-2 shows the voltage dependence of the change rate of a CMOS gate's propagation delay. The change rate of the propagation delay remains almost unchanged when the supply voltage is higher than 4 V_t. It starts increasing significantly when the supply voltage is reduced to about $2V_t$ to $2.5V_t$, which is the same as the voltage range for VLV testing proposed in Chapter 2.

Table 3-3 lists the delay ratios of WD and fault-free gates at different voltages for the 0.8 μm technology. The input of the WD gate was degraded by 0.7V. We calculated

$T_d(V_{dd})$ by using Equation 3-1 and $T_{WD}(V_{dd})$ by using Equation 3-2. In these equations, a is the ratio of a normal signal to a degraded signal. Based on the results, the delay ratios increase significantly when the supply voltage is $2V_t$ to $2.5V_t$. Similar results for a 0.6 μm technology can be found in Appendix B. As shown in Appendix B, we also used more complicated circuits to verify the conclusion.

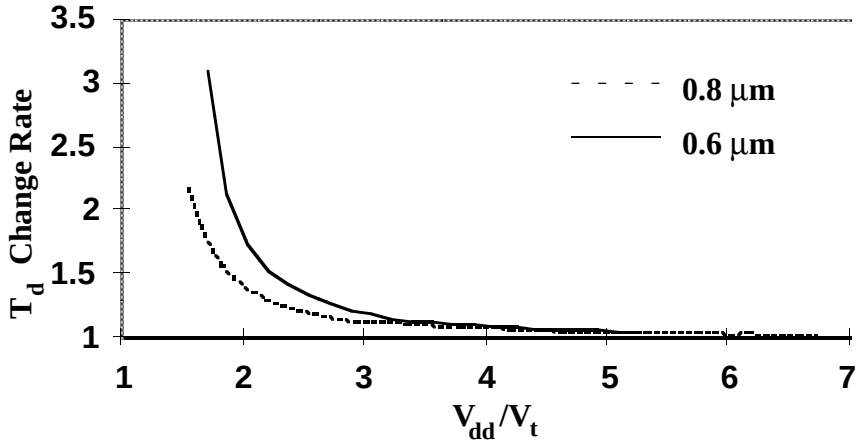

Figure 3-2 Voltage Dependence of the Change Rate of the Propagation Delay of a CMOS Inverter

Table 3-3 WD Delay Ratios for the 0.8 μm Technology

V_{dd}	V_{dd}/V_{tn}	$T_d(V_{dd})^*$	a	$T_{WD}(V_{dd})^{**}$	Delay Ratio $T_{WD}(V_{dd})/T_d(V_{dd})$
1.6V	*2.24*	*1.70ns*	*1.78*	*33.71ns*	*22.8*
1.7V	*2.38*	*1.46ns*	*1.70*	*17.37ns*	*11.9*
1.8V	*2.52*	*1.27ns*	*1.64*	*10.09ns*	*7.9*
1.9V	2.66	1.13ns	1.58	6.71ns	6.0
2V	2.80	1.01ns	1.54	4.86ns	4.8
3V	4.20	0.48ns	1.30	0.99ns	2.1
5V	7.00	0.23ns	1.16	0.32ns	1.4

* based on Equation 3-1, ** based on Equation 3-2

It is important to point out that the supply voltage for VLV testing should be set in the region where the change rate of the propagation delay, rather than the propagation delay itself, starts to increase significantly. Although CMOS devices will have severe

degradation in the speed performance if $V_{dd} < 4V_t$ [Mii 94], the change rate of the propagation delay at $4V_t$ remains similar to that at the normal operating voltage.

3.3 Delay Flaws

We studied three defects, transmission gate opens, threshold voltage shifts, and diminished-drive gates, that can cause delay flaws in a CUT. We also verified that the supply voltage for VLV testing proposed in Chapter 2 is valid for detecting these timing failures. The detailed simulation setup and results can be found in Appendix B.

3.3.1 Transmission Gate Opens

The results in Appendix B show that the effects of the delay flaws are not very serious unless the supply voltage is low enough. Depending on the operating condition, the effects of the delay flaws can be significant and cause intermittent failures. Consequently, they must be detected in order to ensure IC quality. The supply voltage for VLV testing should be as low as $2V_t$ to $2.5V_t$ to achieve reasonable improvement in the flaw coverage for delay flaws. If V_{tn} and $|V_{tp}|$ are different, V_t should be the smaller of the two to ensure flaw coverage in both PMOS and NMOS transistors.

Although transmission gate opens can increase the quiescent current, the amount of increase depends on the sizes of the transistors that are connected to the outputs of a faulty transmission gate and the difference between the threshold voltages of an NMOS and a PMOS transistor. Therefore, transmission gate opens may not be detected by I_{DDQ} testing.

3.3.2 Threshold Voltage Shifts

Threshold voltage shifts can be caused by process variations or hot carrier effects. Process variations can cause global but not local threshold voltage shifts. On the other hand, hot electrons can cause global or local threshold voltage shifts. The discussion here concentrates on finding the appropriate supply voltage for VLV testing for threshold voltage shifts.

If a transistor has a larger threshold voltage than expected, its transconductance is smaller. As a result, the transistor has lower driving capability and causes an excessive delay during a transition. However, at the normal operating voltage the magnitude of the excessive delay is insignificant if the threshold voltage is shifted by a small amount. By

reducing the supply voltage, one can make the degradation of the driving capability of a transistor more pronounced which results in a longer delay. I_{DDQ} testing is not effective for testing threshold voltage shifts since these shifts degrade only the speed performance of a CMOS gate. The static current of a faulty gate caused by threshold voltage shift does not increase.

VLV testing is effective in detecting global threshold voltage shifts. [Chang 96b] and Appendix B contain the detailed simulation setup and results for both global and local threshold voltage shifts. Only the key findings are summarized here.

Because the mobility of a hole is smaller than that of an electron, hot carrier effects are less significant for a PMOS transistor than an NMOS transistor. Consequently, threshold voltage shifts are smaller for PMOS transistors. As a result, we investigated the effects of threshold voltage shifts at different voltages only in NMOS transistors. Below, the *delay ratio* is the ratio of the propagation delay of a faulty circuit with threshold voltage shifts to that of a fault-free circuit.

For global threshold voltage shifts, we assume a defect is detectable if the delay of a faulty circuit increases by 25%. At the normal operating voltage, the simulation results in [Chang 96b] show that the delay ratio of a faulty circuit with a 0.2V global threshold voltage shift and a fault-free circuit is only 1.06, which is undetectable. The detectable range of global threshold voltage shifts does not change significantly until the supply voltage is lowered to 1.5V, which is $1.67|V_{tp}|$ or $2.11V_{tn}$. Therefore, the supply voltage of $2V_t$ to $2.5V_t$ proposed in Chapter 2 can offer reasonable flaw coverage for global threshold voltage shifts, where V_t is the smaller of V_{tn} or $|V_{tp}|$.

For a local threshold voltage shift, the slack of the path and the magnitude of the increased gate delay determine whether the defect can be detected by a delay test. Based on the results in [Chang 96b], at the normal operating voltage the delay ratios are only around 1.1 when the threshold voltage is shifted by 0.2V or 0.3V, which is undetectable. At 1.5V, which is $2.11V_{tn}$ or $1.67|V_{tp}|$, the ratios increase to 1.72 when the threshold voltage is shifted by 0.3V. Although the detectability of local threshold voltage shifts depends on the slack of the path in which the faulty gate is embedded, the effects of the defects are always more severe at low voltage.

3.3.3 Diminished-Drive Gates

In order to provide enough drive strength for either long interconnects or large loading, some gates are designed to be connected in parallel. This avoids the need to use

large components. Figure 3-3 shows an example. One of the two inverters (the one in gray) in the high-drive gate malfunctions and cannot pass any signals. We did three simulations with respectively a 100 μm, 500 μm, and 1000 μm long interconnect between the output of the high-drive gate and the 8 NAND gates. All input and output nodes were properly buffered. We measured the propagation delay from V_{A0} to V_{out1} and we found the interconnect delay to be 38% of the measured delay at the normal operating voltage for the 100 μm case, 53% for the 500 μm case, and 58% for the 1000 μm case. The signal was set so that there was a rising transition at the output of the faulty gate. Because NMOS transistors have greater driving strength than PMOS transistors, the faulty effect was more pronounced when the PMOS transistor in the faulty gate drove the output of the faulty gate. Also, because the simulation results for the 0.8 μm technology and the 0.6 μm technology are similar, only the results for the 0.6 μm technology are discussed in this dissertation.

Table 3-4 shows the simulation results for the 0.6 μm technology. The italicized rows are the simulation results of the proposed supply voltage range. The delay ratio improves from 1.11 to 1.81 when the supply voltage is reduced from 3.3V ($5.59V_{tn}$) to 1.2V ($2.03V_{tn}$) when the wire length between the output of the high-drive gate and the inputs of the NAND gates is 1000 μm. The excessive delay increases monotonically as the supply voltage is reduced.

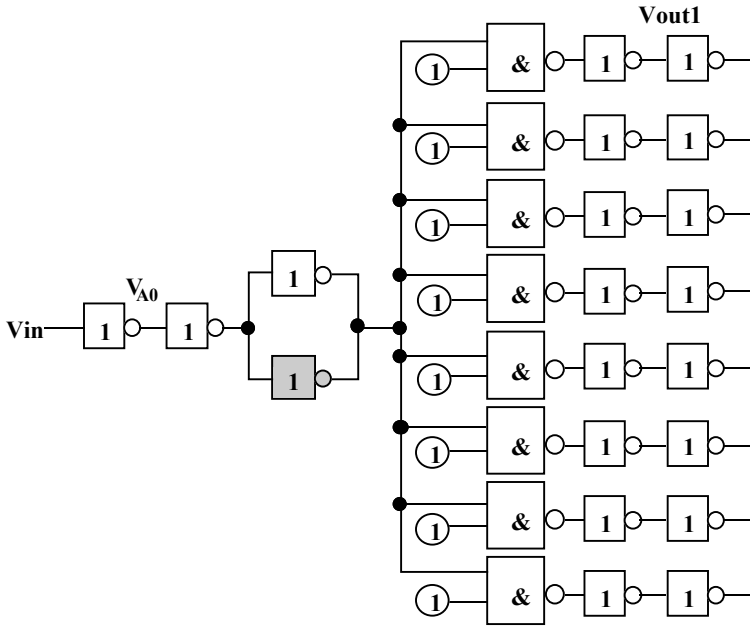

Figure 3-3 Diminished-Drive Gate

Table 3-4 Delay Ratio between Faulty and Fault-Free High-Drive Gate in Fig. 3-3 for the 0.6 μm Technology

Supply Voltage			Delay Ratio T_d (faulty) / T_d (fault-free)		
V_{dd}	V_{dd} / V_{tn}	V_{dd} / V_{tp}	wire length =100 μm	wire length =500 μm	Wire length =1000 μm
1.1	*1.86*	*1.31*	*3.23*	*2.84*	*2.30*
1.2	*2.03*	*1.43*	*3.07*	*2.43*	*1.81*
1.3	*2.20*	*1.55*	*2.93*	*2.11*	*1.56*
1.4	*2.37*	*1.67*	*2.74*	*1.85*	*1.39*
1.5	*2.54*	*1.79*	*2.66*	*1.68*	*1.30*
2.0	3.39	2.38	2.27	1.36	1.17
3.3	5.59	3.93	1.87	1.22	1.11

Weak gates with smaller gate widths caused either by spot defects or process imperfections can also have diminished driving capability. The conclusion based on the simulations done in this dissertation can also be generalized to these weak gates.

3.4 Supply Voltage for VLV Testing for Timing Failures

In summary, VLV testing can make delay flaws more detectable. It increases the significance of a gate delay fault and makes it more detectable even if the fault exists in a short path (non-critical path). Not only can VLV testing improve the detectability of the delay flaws discussed in this dissertation, but it should also be able to improve the detectability of other delay flaws that are caused by degraded signals.

Through extensive simulations, we verified that the supply voltage proposed in [Chang 96a] and Chapter 2 for VLV testing is also valid for detecting delay flaws. The supply voltage for VLV testing should be in the range of $2V_t$ and $2.5V_t$, where V_t is the smaller of V_{tn} or $|V_{tp}|$. The delay flaws considered in this chapter may not be detectable by current tests. Moreover, VLV testing works when the total leakage current is too big for I_{DDQ} testing [Chang 96a]. Low voltage technologies have lower threshold voltages to improve their performance [Mii 94]. Although a substrate back-biasing technique can be used to reduce the quiescent currents of these technologies [Burr 94], this technique adds

complexity in the development of technologies and in circuit operations and thus increases the cost.

3.5 Conclusions

Most timing failures are due to degraded signals or transistors with lowered driving capabilities. This chapter discussed how VLV testing can improve the detectability of the timing failures caused by degraded signals or gates with lowered driving capabilities. The supply voltage for VLV testing for detecting delay flaws should be set in the region where the change rate of the propagation delay of a CMOS gate starts increasing significantly. For the technologies used in this study, the change rate of the propagation delay of a CMOS inverter starts increasing when the supply voltage is between $2V_t$ and $2.5V_t$. We then simulated more complicated circuits to verify this finding. The delay flaws considered in this chapter include transmission gate opens, threshold voltage shifts, and diminished-drive gates. Transmission gate opens cause degraded signals. Threshold voltage shifts and diminished-drive gates lower the driving capability of the defective gates. The effects of delay flaws become significant when the supply voltage is set between $2V_t$ and $2.5V_t$. This conclusion is the same as that in Chapter 2 and [Chang 96a].

Delay flaws can cause early-life and intermittent failures and are hard to detect at normal operating conditions. VLV testing provides an effective and low-cost option to detect these marginal timing problems. It can be applied even when the leakage current of a CUT is too big for I_{DDQ} testing. It can also help reduce the need to do burn-in.

Chapter 4

Testing Flaws in CMOS Domino Circuits

This chapter investigates the problems associated with testing flaws in CMOS domino circuits. We propose methods to detect flaws in CMOS domino circuits and also show a new keeper design that can improve the testability of CMOS domino circuits without having a significant impact on the performance. Appendix C includes a detailed discussion of testing resistive shorts in CMOS domino circuits.

CMOS domino circuits are susceptible to leakage, noise, and charge-sharing problems [Weste 92] [Larsson 94]. Figure 4-1 shows a CMOS domino circuit without any keeper and internal prechargers. To ensure that CMOS domino circuits will function correctly, designers usually add keepers to eliminate leakage and noise problems, and add internal prechargers to eliminate charge sharing problems. Figure 4-2 shows an example of a CMOS domino circuit with a keeper and an internal precharger [Colwell 95] [Gronowski 96b].

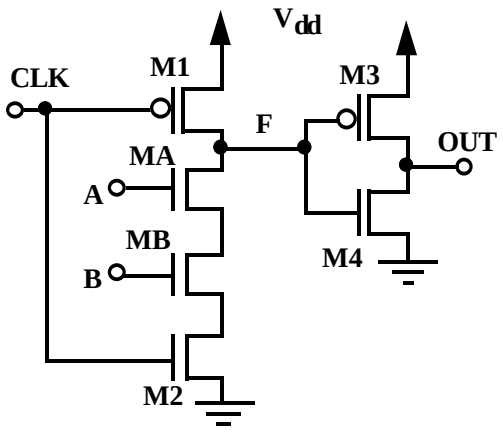

Figure 4-1 CMOS Domino Circuit

In Fig. 4-2, the keeper can hold the value at node F when the clock signal goes high and both inputs stay low throughout the evaluation phase. In this dissertation, node F in any CMOS domino circuit is referred to as a *dynamic node*. Without the keeper, the charge at the dynamic node can be discharged through leakage or be corrupted by noise. This can cause the logic value at the output to change to an incorrect value. During the

precharge phase, the clock signal is low and thus turns on the PMOS internal precharger. The internal node can be precharged to V_{dd} so that the charge-sharing problem can be avoided.

We first analyzed intra-gate and inter-gate resistive shorts in CMOS domino circuits without keepers. Some intra-gate shorts, such as gate oxide shorts can only cause small delay faults at normal voltage. We found that these shorts can become stuck-at faults at very low voltage. We have proposed VLV testing for static CMOS circuits [Hao 93a] [Chang 96a] [Chang 96b]. The supply voltage for VLV testing should be $2V_t$ to $2.5V_t$ for static CMOS circuits, where V_t is the threshold voltage of a transistor [Chang 96a] [Chang 96b]. We also investigated intra-gate resistive shorts other than gate oxide shorts. Section 4.2 summarizes the conclusions of the study. A detailed discussion is presented in Appendix C. For inter-gate resistive shorts, *the defect coverage of resistive shorts*, which we defined as the maximum detectable resistance of a short, can be improved by making the supply voltage about 40% higher than the normal operating voltage or by reducing the supply voltage to about $2V_t$. The defect coverage of inter-gate resistive shorts in CMOS domino circuits can also be improved by increasing the temperature.

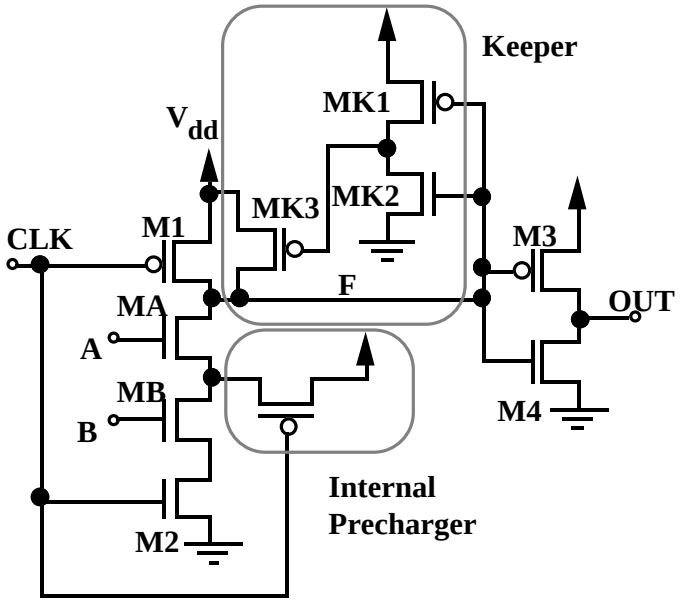

Figure 4-2 CMOS Domino Circuit with a Keeper

I_{DDQ} testing is impractical for CMOS domino circuits without any keepers because of the potential floating node problem on any dynamic nodes. Section 4.5 describes this

problem in detail. Keepers, circuits that can alleviate leakage and noise problems in CMOS domino circuits, can effectively remove the floating node problem and thus make these gates I_{DDQ} testable [Colwell 95]. If all the CMOS domino circuits in a CUT are implemented with keepers, there will not be any floating nodes in the defect-free domino circuits. Therefore, CMOS domino circuits with keepers will not draw any static current and we can keep the CUT in a desired state. However, keepers are not always used in CMOS domino circuits because they add parasitic capacitance at the critical nodes, reducing the performance of these gates [Williams 96].

Keepers are seldom added in small CMOS domino circuits because of the significant performance impact. We propose a new keeper design for small CMOS domino circuits, one that has much less of a performance impact on them than other keeper designs. The detailed structure, simulation results, and comparison are provided in Sec. 4.4.

4.1 Defects in CMOS Domino Circuits

Table 4-1 lists the defects and their corresponding failure modes in CMOS domino circuits. An intra-gate resistive short could be one of the shorts listed in the CrossCheck fault model [Swan 89], i.e., *a short between an interconnect and power (STP), a short between an interconnect and ground (STG), a short within a FET (SHF), or a short between two interconnects within a cell (SHI).* An open defect could be one of the opens listed in the CrossCheck fault model, i.e., *an open within a FET (OPF) or an open interconnect within a cell (OPI).* In the table, the defects in keepers and internal prechargers are separated from the defects in the other transistors in CMOS domino circuits. We classify the defects in this way because not all CMOS domino circuits necessarily have keepers and internal prechargers. To simplify the discussion, we consider only these defects that cause keepers or internal prechargers to disappear in CMOS domino circuits. The other defects in keepers or internal prechargers can degrade the effectiveness of the keepers or internal prechargers.

Depending on their resistance, intra-gate or inter-gate resistive shorts can increase the propagation delay of a gate, cause an input node or an output node to be stuck at some logic value, reduce noise margin, or draw excessive current. Reduced noise margin means that the signal at the output of the circuit is degraded. Reduced noise margin is a more complicated problem for CMOS domino circuits than for static CMOS circuits. If the defective gate with reduced noise margin at its output is followed by another CMOS domino circuit, it can cause that gate to switch to an incorrect logic state and if this

switch occurs, the defect can be detected. However, if the defective gate is followed by a static CMOS gate or a latch, it may not cause the following gate to switch incorrectly and thus may not be detected.

Table 4-1 Defects and Corresponding Failure Modes in CMOS Domino Circuits

Defects	Failure Modes
Intra-gate resistive shorts: Shorts between an interconnect and power (STP) Shorts between an interconnect and ground (STG) Shorts within a FET (SHF) Shorts between two interconnects within a cell (SHI)	Increased gate delay, stuck-at faults, reduced noise margin, or leakage
Inter-gate resistive shorts	Increased gate delay, stuck-at faults, reduced noise margin, or leakage
Opens within a FET (OPF) Open interconnects within a cell (OPI)	Stuck-at faults or stuck-open faults
Missing keepers	Coupling noise or leakage
Missing internal prechargers	Charge sharing or leakage

Open defects (both OPF and OPI) cause fewer problems in CMOS domino circuits than in static CMOS circuits. Because CMOS domino circuits precharge in every cycle, one can detect most open defects, except the ones in PMOS precharge transistors, by using a single test vector. Researchers have studied and proposed methods to detect opens in CMOS domino circuits [Oklobdzija 84] [Wunderlich 86].

Missing keepers or internal prechargers do not always cause CMOS domino circuits to switch incorrectly. The defective CMOS domino circuits can fail intermittently instead. Because keepers are used to avoid leakage and noise problems in CMOS domino circuits, missing keepers result in the defective CMOS domino circuits malfunctioning due to leakage or noise. Similarly, because internal prechargers are used to eliminate charge-sharing problems, missing internal prechargers can make the defective CMOS domino circuits susceptible to charge-sharing problems. The issues in testing missing keepers and internal prechargers are discussed in Sec. 4.5 and 4.6.

Since other researchers have studied and proposed methods to detect open defects in CMOS domino circuits [Barzilai 84] [Oklobdzija 84] [Wunderlich 86] [Jha 88] [Bruni

92], we focused on intra-gate resistive shorts, inter-gate resistive shorts, missing keepers, and missing internal prechargers in this study.

4.2 Intra-Gate Resistive Shorts

We use the four shorts listed in the CrossCheck fault model in this section. In addition, we consider shorts with high and low resistance.

4.2.1 Shorts within a FET (SHF)

We focus on gate-drain and gate-source shorts in all transistors of a CMOS domino circuit. Drain-source shorts are similar to transistor stuck-on faults. Researchers have reported methods for detecting transistor stuck-on faults [Barzilai 84] [Oklobdzija 84] [Wunderlich 86] [Jha 88] [Jha 90] [Bruni 92]. Most drain-source shorts in transistors of a CMOS domino circuit, except the one in the NMOS clocked evaluation transistor (M2 in Fig. 4-1), can be detected by Boolean tests at normal operating voltage [Ma 95b]. Consequently, we do not include drain-source shorts in this discussion.

If keepers are used for all CMOS domino circuits of a CUT, I_{DDQ} testing can be used to test most of the gate oxide shorts. Renovell and Figueras have reported that most internal shorts in CMOS domino circuits, except the shorts between drain and source of the NMOS transistors in the evaluation network, can be detected by I_{DDQ} testing [Renovell 93]. In this study, we used CMOS domino circuits without keepers for the investigation of gate oxide shorts. However, our conclusions can be directly applied to all CMOS domino circuits. Gate oxide shorts with small resistance can be detected by Boolean tests at normal operating voltage. Those that escape Boolean tests at normal operating voltage can be detected through VLV testing.

We injected gate oxide shorts in a 4-input AND gate. Figure 4-3 shows the simulated CMOS domino circuit. Figure 4-4 shows the simulation setup. All the inputs, except the clock signal, were buffered by CMOS domino buffers. The clock signals were buffered by static CMOS buffers. The OR gate was properly loaded. We assumed that the output is observable only in the evaluation phase. A 0.6 μm technology, whose normal operating voltage is 3.3V, was used for all simulations discussed in this section. The nominal threshold voltage for an NMOS transistor is 0.59V.

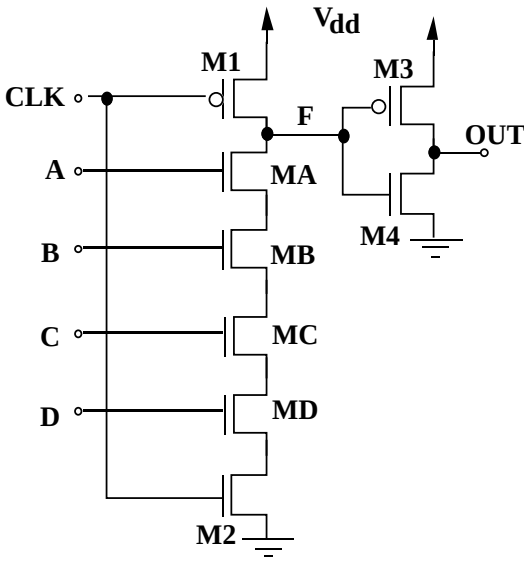

Figure 4-3 4-Input AND Gate

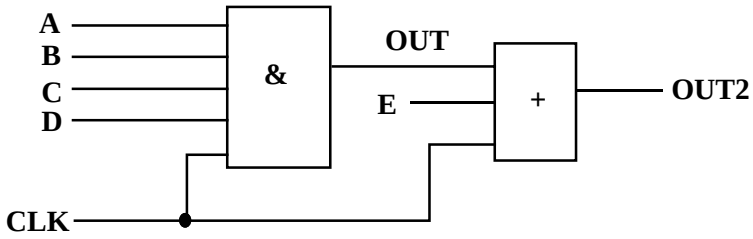

Figure 4-4 Simulation Setup

We can improve the defect coverage by reducing the operating voltage during testing. At low voltages, the equivalent resistance of a transistor increases while the resistance of a short remains almost the same [Hao 93a] [Chang 96a]. Consequently, the fault effect of a resistive short is more significant at low voltages. For the defective gate discussed in this section, the voltage at the dynamic node is close to zero at low voltage for a short with large resistance. Thus, the defect behaves like a stuck-at-one fault at the output of the CMOS domino circuit. Table 4-3 lists the defect coverage of different SHFs at different supply voltages. For the tables presented in this section, the bold and italicized rows indicate the supply voltage range proposed for VLV testing [Chang 96a] [Chang 96b]. The detailed description of the test condition for each SHF can be found in Appendix C.

Table 4-2 Defect Coverage of SHFs at Different Supply Voltages

Vdd(V)	Vdd / Vt	Defect coverage(KΩ)						
		MA GD*	MA GS**	M1 GD	M1 GS	M2 GD	M2 GS	M3 GS
1.2V	***2.0***	***≤ 20***	***≤ 13***	***≤ 14***	***≤ 2.6***	***≤ 5.3***	***≤ 5.0***	***≤ 15***
1.5V	***2.5***	***≤17***	***≤ 6.4***	***≤ 5.1***	***≤ 1.1***	***≤ 1.7***	***≤ 1.7***	***≤ 8.2***
1.7V	2.9	≤ 14	≤ 4.6	≤ 3.7	≤ 0.5	≤ 1.0	≤ 1.1	≤ 6
2.0V	3.4	≤ 11	≤ 3.1	≤ 2.6	≤ 0.5	≤ 0.6	≤ 0.8	≤ 4.4
2.5V	4.2	≤ 9	≤ 2.0	≤ 1.9	≤ 0.3	≤ 0.3	≤ 0.5	≤ 3.1
3.3V	5.6	≤ 5	≤ 1.2	≤ 1.5	≤ 0.2	≤ 0.2	≤ 0.3	≤ 2.1

* GD: gate-drain short

** GS: gate-source short

The gate-drain and gate-source shorts in the other NMOS transistors in the evaluation network behave similarly to the gate-drain and gate-source shorts in MA during the evaluation phase. The difference is that the shorts in the other transistors do not cause any fault effect during the precharge phase. However, they can be detected in a similar way. The defect coverage of gate-source short in M4 and gate-drain shorts in either M3 or M4 is larger than 10 KΩ at normal operating supply voltage.

The gate-source short in M1 is the only short in a CMOS domino circuit that requires a two-pattern test for detection. The first pattern should discharge the dynamic node and thus set the output of the domino circuit to be one in the evaluation phase. The second pattern should be set so that the output of the domino circuit does not switch from zero to one during the evaluation phase.

4.2.2 Shorts between an Interconnect and Power (STP)

All STPs in a CMOS domino circuit can be detected by a 100% SSF test set for the gate. The detailed discussion of the test condition for each STP can be found in Appendix C.

4.2.3 Shorts between an Interconnect and Ground (STG)

Except the STG at the drain node of the NMOS evaluation transistor, all the other STGs in a CMOS domino circuit can be detected by a 100% SSF test set for the gate. An STG at the drain node of the NMOS evaluation transistor can only increase the power consumption of the domino circuit. This STG cannot cause the domino circuit to fail functionally. Appendix C includes a detailed discussion of the test conditions of all the STGs in a CMOS domino circuit.

4.2.4 Shorts between Two Interconnects within the Cell (SHI)

If an SHI occurs within a transistor of a CMOS domino circuit, it is the same as an SHF, whose test condition has been shown in Sec. 4.2.1 and Appendix C. We consider a short between an input/output and an internal node within the cell as an SHI too. Most SHIs can be detected by applying a 100% SSF test set. There are two types of SHIs that cannot be detected by a 100% SSF test set. One is an SHI between an input and a source node of any NMOS transistor in the evaluation network and the two defective NMOS transistors are not in the same transistor stack. The other is an SHI between the output and a source node of any NMOS transistor in the evaluation network. However, these two types of SHIs can be detected by a single vector. The detailed discussion of the test condition for each SHI in a CMOS domino circuit can be found in Appendix C.

4.2.5 Summary

In summary, all but one gate oxide short in a CMOS domino circuit can be provoked by the test vectors for stuck-at pin faults. Only one short, the gate-source short in the precharge PMOS transistor, requires a two-pattern test. We can improve the defect coverage of gate oxide shorts by using VLV Testing [Hao 93]. Based on the data shown in Table 4-2, the supply voltage for VLV Testing should be set between $2V_t$ and $2.5V_t$ [Chang 96a] [Chang 96b].

All STPs and STGs and most SHIs in CMOS domino circuits can be detected by single stuck-at test vectors. There are two types of SHIs in CMOS domino circuits that cannot be detected by single stuck-at test vectors. Nevertheless, they can still be detected by a vector at the nominal supply voltage.

4.3 Inter-Gate Resistive Shorts

CMOS domino circuits dissipate more power than static CMOS gates because the signals in CMOS domino circuits switch every cycle. Consequently, CMOS domino circuits increase the operating temperature faster than static CMOS gates. Also, the noise margin of a CMOS domino circuit strongly depends on the transistor threshold voltage. As the temperature increases, the transistor threshold voltage decreases [Sze 81]. As a result, the noise margin of a CMOS domino circuit decreases as the operating temperature increases. Consequently, resistive shorts with large resistance, which cannot be detected at normal operating voltage and room temperature (25^{o}C), may fail when the operating temperature increases due to power dissipation of CMOS domino circuits.

Figure 4-5 shows the simulated circuit. All four logic gates are implemented with CMOS domino circuits without keepers. A resistive short, shown as the thick line in Fig. 4-5, exists between the output nodes of two 2-input domino AND gates. We assumed that the resistance of the short does not change with changing temperature. The detailed description of the simulation setup and results can be found in Appendix C.

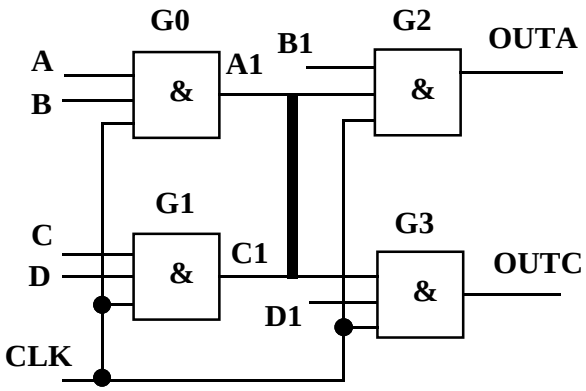

Figure 4-5 Resistive Short

The supply voltage used for testing resistive shorts in CMOS domino logic should be selected so that we can detect all the defects that can cause a circuit to fail at high operating temperature and normal operating voltage. Also, a defect-free circuit should still be functional at the selected supply voltage.

Figure 4-6 shows the defect coverage of the short shown in Fig. 4-5 at different voltages and different temperatures. The gray region is the suggested supply voltage range for testing. The supply voltage should be either 40% higher than a normal operating voltage or about $2V_t$. The proposed supply voltage at very low voltage matches the one proposed in [Chang 96a] [Chang 96b].

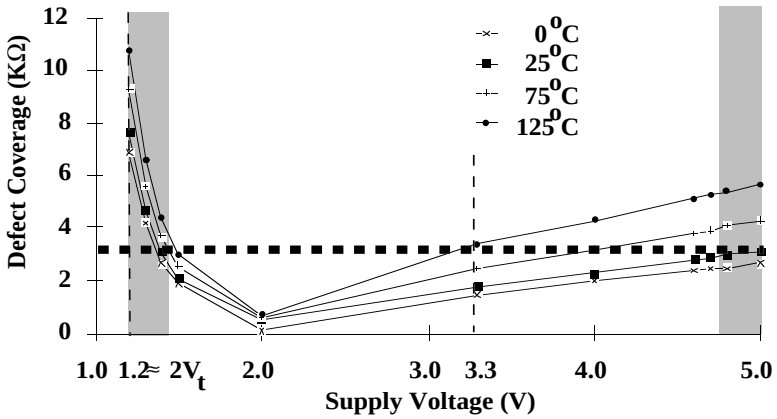

Figure 4-6 Desired Supply Voltage Range (in the Gray Region)

We also did a similar study, in which we changed G2 and G3 to 4-input AND gates, and obtained similar results. Appendix C includes the detailed results for this simulation. Even though the defect coverage is smaller than that for the short simulated in Fig. 4-5 at the same supply voltage and temperature, the conclusion for the proposed supply voltage range remains the same.

4.4 Keepers

When the clock signal of a CMOS domino circuit is low, the CMOS domino circuit is in *the precharge phase.* When the clock signal of a CMOS domino circuit is high, the CMOS domino circuit is in *the evaluation phase.* The dynamic node in a CMOS domino circuit, node F in Fig. 4-1, may become a floating node during the evaluation phase. For the CMOS domino circuit shown in Fig. 4-1, F becomes a floating node in the evaluation phase if A and B are held low. During an I_{DDQ} test or a slow functional test, the voltage at F for a defect-free gate can drop due to the leakage current through MA, MB, M1, and M2. If we wait for all the signals in the CUT to settle, the voltage at F may drop severely enough to either turn on both M3 and M4 or change OUT to an incorrect logic state. The former case causes static current in the CUT. For the latter case, we cannot set the CUT into a desired state and thus will lose fault coverage. Consequently, it is not only difficult to perform I_{DDQ} testing on CMOS domino circuits, but they also require high speed Boolean testing.

Keepers are the transistors that are added to a CMOS domino circuit to make dynamic node static. Keepers, which are used to eliminate leakage and noise problems, remove the floating node problem and make the operation of CMOS domino circuits

static. Not only do keepers ensure CMOS domino circuits function correctly, they also help remove the two testing problems mentioned in the previous paragraph.

Keepers, however, can degrade the switching speed of CMOS domino circuits. The impact of keepers is not significant for the performance of complex CMOS domino circuits, but can be severe for that of small CMOS domino circuits, such as a 2-input OR gate or a 2-input AND gate. If these gates appear in critical paths, keepers usually are not used. However, if keepers are not used for all CMOS domino circuits in a CUT, the background current can still be too large to perform I_{DDQ} testing and we must test CUTs at-speed to avoid losing logic states in CMOS domino circuits without keepers.

We studied several keeper designs [Colwell 95] [Gronowski 96b] and propose a new design specifically for small CMOS domino circuits. Figure 4-7 shows the new keeper design for a 2-input AND gate. Figure 4-8 shows the new keeper design for a 2-input OR gate. Both MKA and MKB in Fig. 4-7 and Fig. 4-8 are minimum-size PMOS transistors. Figure 4-9 is a keeper design that has been used for CMOS domino circuits with small channel width. In Fig. 4-2, MK1, MK2, and MK3 are minimum-size transistors. In Fig. 4-9, MK1 is a PMOS transistor with minimum gate width but large channel length. MK2 is a minimum-size PMOS transistor. We will refer to the new keeper design as keeper design A, the keeper implementation in Fig. 4-2 as keeper design B, and the keeper implementation in Fig. 4-9 as keeper design C. The operation of keeper design C is similar to that of keeper design B. The PMOS transistor with larger channel length is added to weaken the strength of the keeper. In this way, we can keep the extra loading at the output node at the level of the gate capacitance of a minimum-size PMOS transistor and also reduce the performance impact.

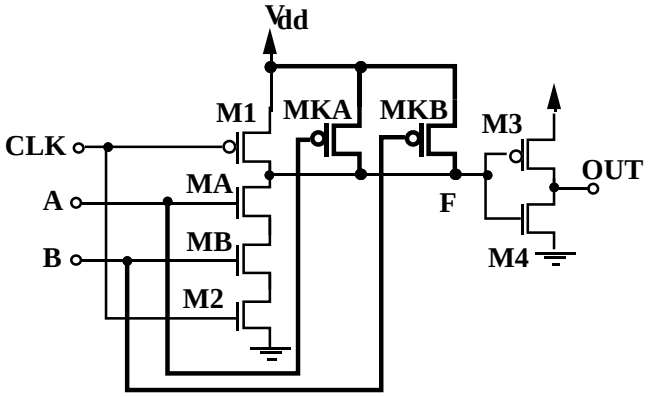

Figure 4-7 2-input CMOS Domino AND Gate with Keeper Design A

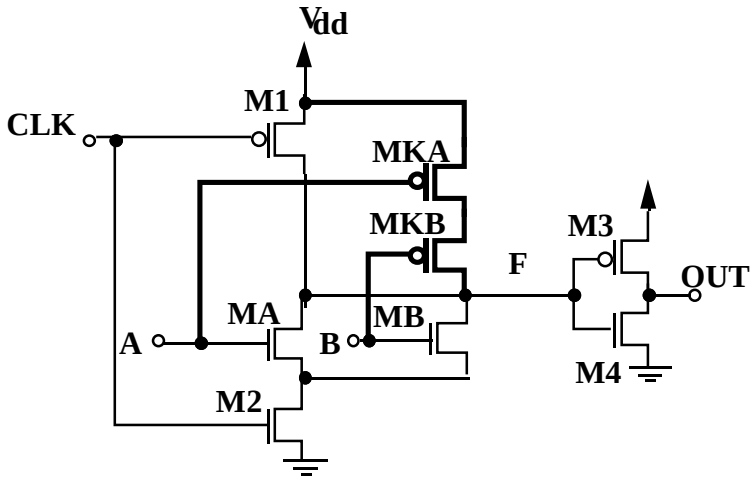

Figure 4-8 2-input CMOS Domino OR Gate with Keeper Design A

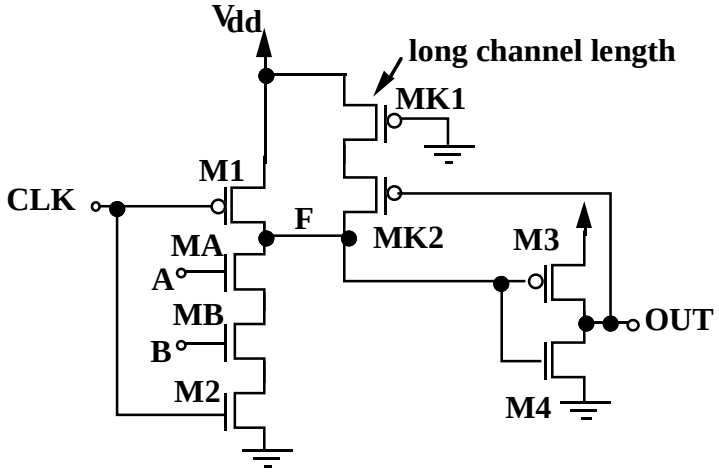

Figure 4-9 Keeper Design C in a Tiny CMOS Domino Circuit

The structure of a CMOS domino circuit with keeper design A is similar to that of a static CMOS logic gate. The difference is that the clock signal precharges the dynamic node to one during the precharge phase and the transistors are sized so that we optimize only single-end transitions. Keeper design A adds extra loading at the input of a CMOS domino circuit. However, since the PMOS transistors are very small, the keeper has minimal impact on the input loading. It adds only very small diffusion capacitance to the dynamic node, F in Fig. 4-1, of a CMOS domino circuit. Although keeper designs B and C do not add any extra loading at the input of a CMOS domino circuit, they add the loading somewhere else. Keeper design B adds gate capacitance and a small diffusion capacitance to the dynamic node of a CMOS domino circuit. Keeper design C adds gate

capacitance to the output of a CMOS domino circuit and a small diffusion capacitance to the dynamic node. The other advantage of keeper design A is that it can correct an erroneous transition at slow speed.

We simulated a 2-input AND gate, a 4-input AND gate, a 2-input OR gate, and a 4-input OR gate. Each gate was implemented with different keeper designs. The simulations were based on two sub micron technologies. One is a 0.35 μm LSI Logic G10p technology. The other is a 0.6 μm HP CMOS14TB technology. The simulated CMOS domino circuits with different keeper designs all have the same size except for their keepers. All internal nodes in the evaluation network were precharged to Vdd before the evaluation phase. We used the fanout-of-four rule at the output load of each gate, and we measured the propagation delay through each CMOS domino circuit.

Tables 4-3, 4-4, 4-5, and 4-6 show the simulation results. The number in each table is the propagation delay of a CMOS domino circuit with a keeper normalized by the propagation delay of the same domino circuit implemented without any keeper. The parameter λ is half of the feature size. The size listed in the first column of each table is the transistor size of an NMOS transistor in the evaluation network of each CMOS domino circuit. For example, it is the size of MA in Fig. 4-1.

Table 4-3 Simulation Results for a 2-Input AND Gate

	Td (with keeper) / Td (without keeper)					
	0.35 μm technology			0.6 μm technology		
size	Keeper A	keeper B	keeper C	keeper A	keeper B	keeper C
3.1λ*	**1.06**	1.58	1.23	**1.07**	1.77	1.25
4.7λ	**1.02**	1.37	1.14	**1.02**	1.31	1.14
6.3λ	**1.00**	1.26	1.09	**0.99**	1.19	1.09
7.8λ	**0.99**	1.19	1.07	**0.98**	1.13	1.07
9.4λ	**0.98**	1.15	1.05	**0.97**	1.10	1.05
10.9λ	**0.97**	1.12	1.03	**0.97**	1.08	1.04
12.5λ	**0.96**	1.11	1.02	**0.97**	1.06	1.03
14.1λ	**0.96**	1.09	1.02	**0.97**	1.05	1.03
15.6λ	**0.96**	1.08	1.01	**0.97**	1.04	1.02

* $\lambda = 0.5 \times$ feature size

Table 4-4 Simulation Results for a 4-Input AND Gate

size	T_d (with keeper) / T_d (without keeper)					
	0.35 μm technology			0.6 μm technology		
	Keeper A	keeper B	keeper C	keeper A	keeper B	keeper C
6.3λ*	**1.13**	1.36	1.16	**1.10**	1.29	1.12
9.4λ	**1.08**	1.21	1.10	**1.04**	1.14	1.07
12.5λ	**1.05**	1.14	1.07	**1.02**	1.09	1.05
15.6λ	**1.03**	1.11	1.06	**1.00**	1.06	1.04
18.8λ	**1.02**	1.08	1.04	**0.99**	1.04	1.03
21.9λ	**1.02**	1.07	1.04	**0.99**	1.03	1.03
25.0λ	**1.01**	1.06	1.03	**0.98**	1.03	1.02
28.1λ	**1.01**	1.05	1.03	**0.98**	1.02	1.02
31.3λ	**1.00**	1.04	1.02	**0.98**	1.02	1.02

* $\lambda = 0.5 \times$ feature size

Table 4-5 Simulation Results for a 2-Input OR Gate

size	T_d (with keeper) / T_d (without keeper)					
	0.35 μm technology			0.6 μm technology		
	keeper A	keeper B	keeper C	keeper A	keeper B	keeper C
3.1λ*	**1.08**	1.33	1.16	**1.05**	1.37	1.13
3.9λ	**1.06**	1.26	1.13	**1.03**	1.23	1.09
4.7λ	**1.05**	1.21	1.11	**1.03**	1.16	1.07
5.5λ	**1.04**	1.18	1.09	**1.02**	1.12	1.06
6.3λ	**1.03**	1.15	1.08	**1.02**	1.10	1.05
7.0λ	**1.03**	1.13	1.07	**1.01**	1.08	1.04
7.8λ	**1.02**	1.11	1.06	**1.01**	1.07	1.04

* $\lambda = 0.5 \times$ feature size

Table 4-6 Simulation Results for a 4-Input OR Gate

size	T_d (with keeper) / T_d (without keeper)					
	0.35 μm technology			0.6 μm technology		
	keeper A	keeper B	keeper C	keeper A	keeper B	keeper C
3.1λ*	**1.14**	1.34	1.16	**1.11**	1.37	1.13
3.9λ	**1.11**	1.27	1.13	**1.08**	1.23	1.09
4.7λ	**1.09**	1.21	1.11	**1.06**	1.16	1.07
5.5λ	**1.08**	1.18	1.09	**1.05**	1.12	1.06
6.3λ	**1.07**	1.15	1.08	**1.04**	1.10	1.05
7.0λ	**1.06**	1.13	1.07	**1.04**	1.08	1.04
7.8λ	**1.05**	1.11	1.06	**1.03**	1.07	1.04

* $\lambda = 0.5 \times$ feature size

The results show that keeper design A has much less impact on the propagation delay of a CMOS domino circuit. For a 2-input AND gate and a 4-input AND gate, the propagation delay of a CMOS domino circuit using keeper design A can have similar or slightly smaller propagation delay than the same domino circuit without any keeper. The reason is as follows: When a CMOS domino circuit goes into the evaluation phase, the clock signal can push the dynamic node F to a voltage slightly higher than V_{dd} through the parasitic capacitance between the gate and drain of the PMOS precharge transistor. For a CMOS domino circuit without any keeper, the extra charge on the dynamic node can only leak through the very small substrate leakage of the precharge PMOS transistor and the NMOS transistor at the top of the evaluation network. There is not enough time for the extra charge to leak away before the CMOS domino circuit switches. Hence, during the evaluation phase, the dynamic node must discharge the extra charge coupled through the clock signal. On the other hand, the keeper can provide a path between the dynamic node and V_{dd}. Right after the clock signal goes high, the extra charge can be discharged through the PMOS transistors in the keeper. Consequently, it needs to discharge less charge on the dynamic node when the domino circuit switches. Thus, when the size of the NMOS transistors in the evaluation network is much larger than the size of the PMOS transistors in the keeper, a CMOS domino circuit with keeper design A can switch slightly faster than one without a keeper.

The results in Tables 4-3, 4-4, 4-5, and 4-6 show that the new keeper design (A) has less performance impact on a CMOS domino circuit than the other two keeper

designs. We suggest that keepers be used in all CMOS domino circuits in a CUT. Depending on the applications, designers can use any keeper design that minimizes the performance penalty. Boolean tests should be used to test CUTs if keepers are not used in all CMOS domino circuits.

4.5 Missing Keepers

Keepers are used in most CMOS domino circuits to eliminate leakage and reduce noise problems. They keep the dynamic nodes in CMOS domino circuits from floating. If all the domino circuits in a CUT have keepers, the CUT can be operated at low speed without losing logic states.

If a defect causes a keeper to disappear in a CMOS domino circuit, the defective gate becomes susceptible to leakage and noise problems. If the defective gate stays in the evaluation phase long enough, the leakage can discharge the dynamic node and thus change the logic state of the defective gate. The defective domino circuit can also fail due to the noise coupled to its dynamic node.

If all the CMOS domino circuits in a CUT have keepers, the defective keeper can be detected by testing the CUT slowly. However, if not all the CMOS domino circuits use keepers, the CUT cannot be operated at low frequencies. In this case, we can use the verification vectors generated by designers for verifying the effects of coupling noise. Because the magnitude of coupling noise is proportional to supply voltage, we can test the CUT at high voltage to maximize the effect of noise coupled to the dynamic node of the defective domino circuit.

4.6 Missing Internal Prechargers

If one or more nodes in the evaluation network (e.g., the source node of MA in Fig. 4-2) is not precharged to V_{dd} before a domino circuit goes into the evaluation phase, a *charge-sharing* problem may occur during the evaluation phase if all the inputs of the domino circuit are held at V_{dd} except the input to the bottom transistor in the evaluation network (e.g., input B in Fig. 4-2). Keepers, however, can hardly help the charge-sharing problem since they are too weak to charge all the internal nodes to V_{dd}. Internal prechargers, such as the one shown in Fig. 4-2, are often used to remove the charge-sharing problem [Gronowski 96b].

A defect that causes the internal prechargers to disappear makes the defective CUT susceptible to the charge-sharing problem. This problem, similar to the coupling-

noise and leakage problem, does not always cause the defective CUT to fail immediately. The defective circuit may function intermittently.

The test vector that sets all but the bottom NMOS transistors in the evaluation network to one is the vector that makes the CUT most vulnerable to charge sharing. This is the same test vector that detects a stuck-at-1 fault at the input node that is connected to the bottom-most transistor in the evaluation network. Thus, a 100% single stuck-at test set can be used as the test set for detecting charge sharing. Moreover, because the voltage drop caused by charge sharing is proportional to supply voltage, we can put the defective CUT into the worst-case charge-sharing condition by running 100% single stuck-at test vectors at the highest operating voltage.

4.7 Conclusions

We have proposed methods to detect intra-gate resistive shorts, inter-gate resistive shorts, missing keepers, and missing internal prechargers in CMOS domino circuits. We found that most gate oxide shorts with low resistance in a CMOS domino circuit can be detected by Boolean tests at normal voltage. Only one gate oxide short requires a two-pattern test for detection. VLV Testing can be used to improve the defect coverage of gate oxide shorts. We can improve the defect coverage of inter-gate resistive shorts in CMOS domino circuits by either making the supply voltage 40% higher than the normal operating voltage or making it as low as $2V_t$ for the technology used in this study.

We suggest that keepers be used in all CMOS domino circuits. Not only can keepers eliminate leakage and noise problems, they also remove the floating node problem in CMOS domino circuits and thus make CMOS domino circuits more testable. Keepers also make CMOS domino circuits consume very small static currents and make them IDDQ testable.

One can detect missing keepers by testing CUTs slowly if all CMOS domino circuits used in the CUTs have keepers. One can detect missing internal prechargers by running 100% single stuck-at test sets at the highest operating voltage.

Chapter 5

SHOrt Voltage Elevation Test

Unlike I_{DDQ} and VLV testing, SHOVE testing detects weak parts by changing their characteristics. Figure 5-1 shows the procedure for SHOVE testing. During SHOVE, test sets such as single stuck-at or pseudo stuck-at test sets, are run at higher-than-normal supply voltage for a short period. Functional tests and I_{DDQ} tests are carried out at normal operating voltage after SHOVE. VLV testing can be used after SHOVE if the background current is too high to perform I_{DDQ} testing. It can also detect the defects whose lifetime is accelerated by SHOVE. This chapter summarizes the theoretical study for SHOVE testing. Appendix D provides a detailed description of the study.

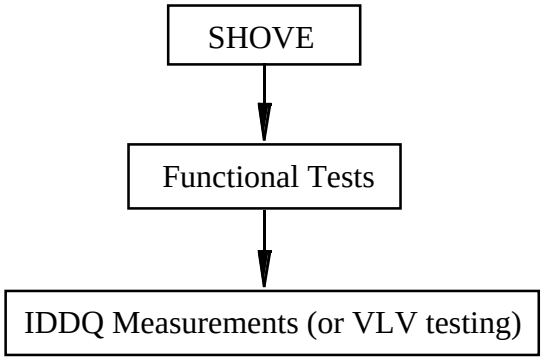

Figure 5-1 SHOVE Testing Procedure

Oxide defects are one of the major causes of unreliability in CMOS ICs [Hnatek 95]. Particulate contamination, crystalline defects in the substrate, spot defects, localized thin regions, or surface roughness can cause localized weak spots in an oxide [Syrzycki 87] [Lee 88]. Moreover, the quality and lifetime of a gate oxide strongly depend on its thickness [Lee 88]. *Oxide thinning* occurs when the oxide thickness of a transistor is actually or effectively thinner than expected. It can be due to localized thin spots, traps in the oxide, surface asperity, or locally reduced tunneling barrier height [Schuegraf 94]. Oxide thinning can increase oxide leakage current or cause time-dependent dielectric breakdown. Hence, it can cause early-life failures and should be detected. We

investigated device behavior during and after SHOVE, and we found that oxide thinning can cause stress-induced oxide leakage or a gate oxide short after SHOVE and thus increase the I_{DDQ} values of the defective CUT.

SHOVE can also cause some *via defects*, which can be via undercut, via overetch, or via contamination [Hnatek 95], to become opens. The defects can then be detected by either I_{DDQ} measurements or functional tests depending on the characteristics of the resulting opens [Barrette 96] [Kawahara 96]. SHOVE is less effective for accelerating electromigration [Hnatek 95]. Temperature stress is a more effective way to stress metalization because electromigration has a larger temperature activation energy than voltage activation energy [Hnatek 95]. On the other hand, temperature stress is less effective for oxide defects or hot carrier effects because of their low temperature activation energy [Hnatek 95].

The stress condition for each transistor is discussed and the parameters, such as stress time and stress voltage for SHOVE testing, are derived. The stress vectors for static and dynamic CMOS circuits are also derived.

5.1 Oxide Thinning and Via Defects

SHOVE testing can increase the leakage current or cause oxide breakdown in a defective oxide whose thickness is less than its specification. Oxide thinning shortens the lifetime of an oxide. As the oxide thickness is decreased in advanced technologies [Charnas 96] [Gronowski 96] [Montanaro 96] [Sanchez 96], oxide thinning becomes a serious problem. Furthermore, as the number of metal layers increases in advanced technologies, via defects are more likely to occur. SHOVE testing can make some via defects become permanent opens. Barrette *et al.* have found that there was no burn-in fallout for the wafer lots that had predominantly oxide defects and there was reduced burn-in fallout for the wafer lots that had predominantly via defects [Barrette 96]. Hnatek also shows that high voltage stress is very effective in screening oxide defects [Hnatek 95].

Several models have been proposed to predict the lifetime of an oxide and the criteria of oxide breakdown onset. Lee *et al.* proposed using “effective oxide thinning” to characterize time-dependent-dielectric-breakdown [Lee 88]. Sune *et al.* proposed a statistical description of oxide breakdown based on neutral trap generation in the oxide during wearout [Sune 90]. Dumin *et al.* found that breakdown occurred locally when the local density of traps exceeded a critical value and the product of the electric field and the higher leakage currents through the traps exceeded a critical energy density [Dumin 94].

We used the "effective oxide thinning" model to estimate the lifetime of an oxide because this model shows the relationship among the voltage across an oxide, effective oxide thickness, and oxide lifetime more directly than other models. Equation 5-1 shows the relationship among these parameters. X_{eff} is the effective oxide thickness, V_{OX} is the voltage across the oxide, t_{BD} is the time-to-breakdown of the oxide, τ_0 is a curve-fitting constant that can be determined by measuring the intrinsic breakdown time under different applied voltages, and G is the slope of $\log(t_{BD})$ versus $1 / E_{OX}$. E_{OX} is the electric field across the oxide, i.e., it is the ratio of V_{OX} to X_{eff}.

$$t_{BD} = \tau_0 \exp(\frac{GX_{eff}}{V_{ox}}) \qquad \textbf{Equation 5-1}$$

Figure 5-2 shows the estimated lifetime of a defective oxide at different voltages for three different technologies. The oxide thickness of the 2V technology is 6.5nm, that of the 3.3V technology is 9nm, and that of the 5V technology is 15nm. The thickness of the defective oxide is assumed to be four-tenths that of a flawless oxide. We assumed that the voltage across the oxide is approximately the same as the supply voltage. We calculated t_{BD} by using Equation 5-1. G is 350 MV/cm and τ_0 is 10 picoseconds [Lee 88].

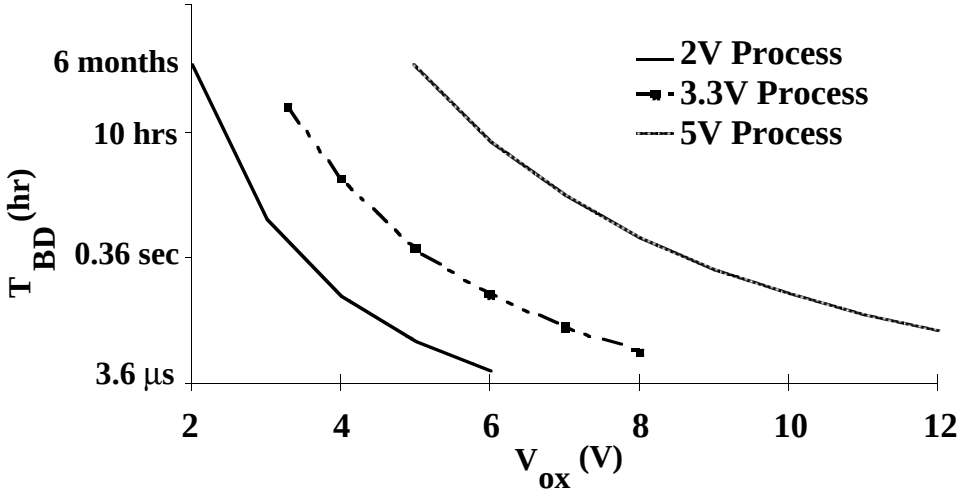

Figure 5-2 Lifetime of Defective Oxides (Thinner by 60%)

Figure 5-2 shows that the lifetime of a defective oxide decreases significantly as the supply voltage is increased. The *stress time* is the duration required to exercise a CUT at an applied voltage until a defect causes the CUT to fail. Figure 5-2 shows that the stress time at high voltage is much shorter than that at normal voltage. For example, the lifetime for a defective oxide is 6 months at the nominal supply voltage for the 5V process. By raising the stress voltage to 9V so that the electric field across the oxide is 6MV/cm, the lifetime of the defective oxide becomes 0.13 seconds. Although the lifetime of a flawless oxide is shortened at high voltage, SHOVE testing does not affect the lifetime of a flawless oxide due to the shortness of the stress period.

Researchers have reported the existence of stress-induced leakage current in a thin oxide film [Naruke 88] [Rofan 91] [Moazzami 92] [Dumin 93] [Patel 94]. They have found that the oxide leakage at normal operating voltage increases in a thin oxide after the thin film is stressed at high voltage. The leakage current occurs before oxide breakdown and can be one of the major failure mechanisms in thin oxides.

The poly gate and channel region of a MOS transistor are highly doped. The energy barrier width is very narrow at a defective site. Consequently, tunneling current occurs at a thin spot when an electrical field is applied across the oxide. The magnitude of the tunneling current increases significantly as the supply voltage increases over its normal value [Moazzami 92] [Dumin 93] [Lee 94]. Large tunneling currents can cause damage in an oxide layer and thus increase oxide leakage current. The failure mechanisms that cause the stress-induced oxide leakage can be localized defects [Olivo 88], localized positive charges [Maserjian 82], or trap states near the injecting surface [Rofan 91] [Moazzami 92]. These mechanisms further reduce X_{eff} in Equation 5-1 and thus shorten the lifetime of an oxide. If the oxide thickness at the defect spot is very thin or the CUT is stressed for enough time, oxide breakdown may occur. Both stress-induced oxide leakage and oxide breakdown can significantly increase the quiescent current of a defective CUT.

Via defects can cause high leakage, timing failure, or functional failure depending on the failure modes [Hnatek 95]. Missing vias between two metal layers can cause functional failure. On the other hand, via undercut can cause a short circuit between two metal layers and thus increase the leakage. The short can also cause timing or functional failure, depending on the resistance of the short.

The dynamic current during SHOVE can make some via defects become opens and thus cause functional failure or leakage. These via defects have high resistance before becoming opens. They increase the propagation delay of the signals passing through the vias, and they can cause intermittent failure or early-life failure. Therefore,

these defects should be detected to ensure IC quality. Because the open vias introduced by SHOVE may either cause functional failure or high leakage, both I_{DDQ} tests and functional tests should be performed after SHOVE to catch these defects.

SHOVE could make unexpected shorts between two metal layers disappear and heal the CUTs if the shorts are thin wires or spot defects. These shorts have high resistance. Thus, it is more likely that the heat generated by the transient or static current across the shorts during SHOVE can burn them off.

We consider only the characteristics of an oxide to determine the parameters for SHOVE tests because the lifetime of an oxide is more sensitive to voltage than the via lifetime.

5.2 Stress Voltage

To stress CUTs effectively, the stress voltage should be set so that it can cause damage only in the defective CUTs and not in flawless CUTs. Because the damage to an oxide at high voltage is mainly due to the tunneling current flowing through the oxide, the stress voltage should be selected so that the oxide tunneling current is very small in a flawless oxide but large in a defective oxide. Two types of tunneling mechanisms, Fowler-Nordheim tunneling and direct tunneling, can appear across an oxide. For most 3.3V and 5V technologies, the oxide thickness of a MOS transistor is larger than 6nm [Schutz 94] [Charnas 95] [Montanaro 96] [Sanchez 96] . Direct tunneling currents only exist in a thin SiO_2 film whose thickness is less than 6nm [Schuegraf 92]. Consequently, Fowler-Nordheim tunneling currents dominate in the flawless oxide at high voltages for most 3.3V and 5V technologies. On the other hand, direct tunneling currents may exist at the thin spot in a defective oxide.

The magnitude of Fowler-Nordheim tunneling current strongly depends on E_{ox}, where E_{ox} is the ratio of V_{ox} to X_{eff} [Schuegraf 92]. Based on various published measurement data, the magnitude of the Fowler-Nordheim tunneling current across an oxide becomes significant when E_{ox} is larger than 6MV/cm [Moazzami 92] [Dumin 93] [Dumin 94] [Watanabe 94] [Depas 96]. Figure 5-3 shows the qualitative relationship between the Fowler-Nordheim tunneling current and E_{ox}. If the stress voltage is selected so that E_{ox} is approximately 6MV/cm in a flawless oxide, E_{ox} across a defective oxide will be much larger than this value. Thus, the tunneling current can flow through the defective site and increase the trap density at the thin spot during SHOVE. Table 5-1 shows the lifetime of a flawless oxide for the 3.3V technology shown in Fig. 5-2. The calculation of the oxide lifetime is based on Equation 5-1. The lifetime of an oxide

shortens significantly when E_{OX} is higher than 6 MV/cm. Table 5-2 lists E_{OX} at normal operating voltages for several technologies. For these technologies, E_{OX} at the normal operating voltage is well below 6MV/cm. In Table 5-2, V_{dd} is the supply voltage and X_{OX} is the oxide thickness. Similar to burn-in, SHOVE can shorten the lifetime of the defective devices and that of a flawless device. After SHOVE, although the lifetime of the flawless device is shortened, it is still reasonably long. Table 5-1 shows that the lifetime of the flawless oxide is 20,041 years after being stressed at 6V (E_{OX} = 6.67MV/cm) for a 3.3V technology. Due to the short stress time, SHOVE testing only slightly affects the oxide quality of a defect-free CUT. As shown in Fig. 5-2, we can accelerate the lifetime of the defective oxide from 6 months at normal operating voltage to 0.13 seconds at the recommended stress voltage.

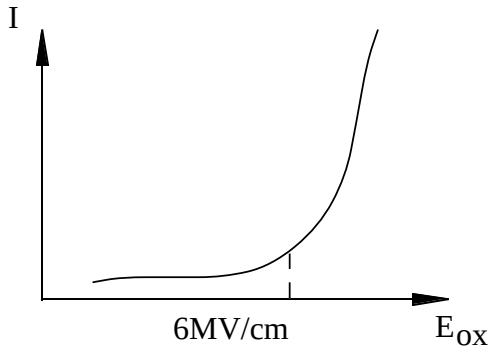

Figure 5-3 Fowler-Nordheim Tunneling Current vs. E_{ox}

Table 5-1 Lifetime of a Flawless Oxide for a 3.3V Technology

V_{OX}	E_{OX}(MV/cm)	t_{BD}
3.3	3.67	9.04×10^{22} yrs
4.0	4.44	5.04×10^{15} yrs
5.0	5.56	7.26×10^{8} yrs
6.0	6.67	20,041 yrs
7.0	7.78	11.1 yrs
8.0	8.89	14.6 days

Table 5-2 Maximum E_{ox} at Normal Operating Voltages

Technologies	V_{dd} (V)	X_{OX}(nm)	E_{OX}(MV/cm)
[Schutz 94]	5	15	3.33
[Charnas 95]	3.3	8.5	3.88
[Sanchez 96]	2.5	7	3.57
[Montanaro 96]	2	6.5	3.08

Based on Equation 5-1, the higher the stress voltage, the shorter the required stress time. Consequently, to shorten the stress time, the stress voltage should be selected so that it can maximize the effect of the stress on the oxide layers of CUTs.

Depending on the oxide thickness of a technology, the recommended stress voltage for SHOVE testing can be determined by using Equation 5-2, which shows the maximum stress voltage for SHOVE testing. X_{OX} is in nanometers.

$$V_{stress} = X_{ox} \times 0.6V / nm \qquad \textbf{Equation 5-2}$$

Based on Equation 5-2, the stress voltage should be 9V for the 5V process shown in Fig. 5-2, 5.4V for the 3.3V process shown in Fig. 5-2, and 3.6V for the 2V process shown in Fig. 5-2. The *voltage acceleration factor* is the ratio of the operating time of an oxide at nominal operating voltage to the equivalent operating time of the same oxide at the stress voltage [Hnatek 95]. At the recommended stress voltage, the voltage acceleration factor of flawless oxides is 1.85×10^{20} for the 5V process, 1.32×10^{16} for the 3.3V process, and 1.85×10^{20} for the 2V process. The voltage acceleration factor for a defective oxide that is 60% thinner than a flawless oxide is 1.28×10^{8} for the 5V process. Figure 5-4 shows the equivalent lifetime of a flawless oxide and a defective oxide (60% thinner than expected) at the recommended stress voltage for the 5V process shown in Fig. 5-2. For example, the equivalent operating time at 9V of the one-year operating time at 5V is 171 picoseconds for a flawless oxide and 0.25 seconds for a defective oxide that is 60% thinner than expected.

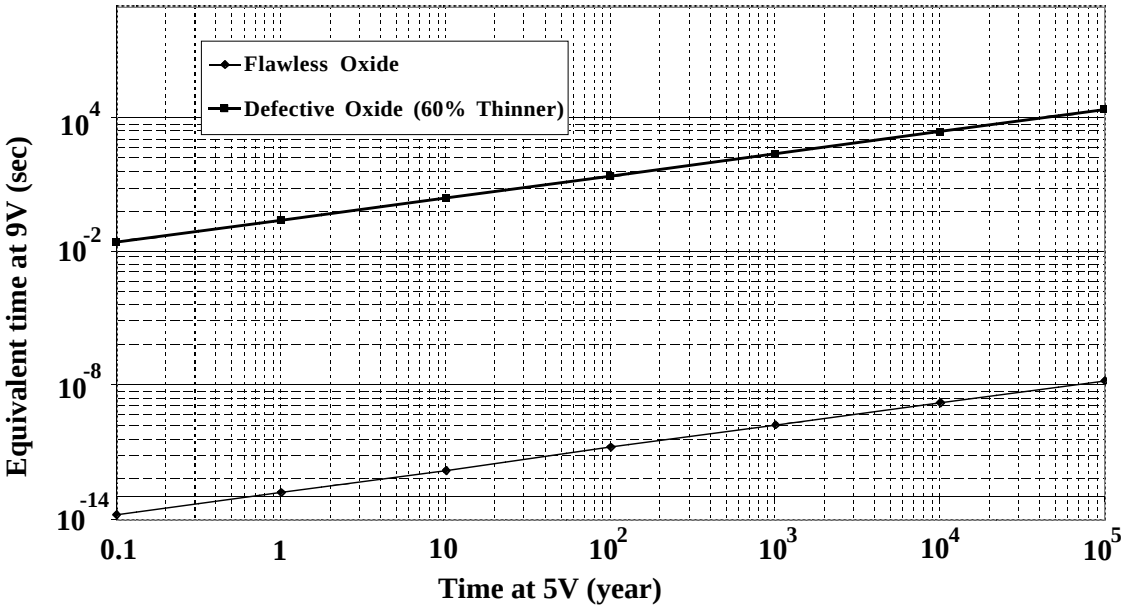

Figure 5-4 Equivalent Operating Time at the Recommended Stress Voltage for the 5V Process Shown in Fig. 5-2

5.3 Stress Vectors

To thoroughly stress all the transistors in a CMOS IC and avoid long stress time, stress vectors must be selected so that the applied voltage occurs across the gate oxide of a transistor. If a junction is not fully biased by the applied voltage, the oxide of the transistor is not stressed effectively. To stress an NMOS transistor, its source, drain, and substrate should be held at 0V while the gate of the transistor is held at the stress voltage. To stress a PMOS transistor, its source, drain, and substrate should be held at the stress voltage while the gate of the transistor is held at 0V. Consequently, to effectively stress an NMOS transistor in a fully complementary CMOS logic gate, the stress vector should connect the logic gate output to ground through the pull-down path that contains the target NMOS transistor. Similarly, to effectively stress a PMOS transistor in a fully complementary CMOS logic gate, the stress vector should connect the logic gate output to the supply voltage through the pull-up path that contains the target PMOS transistor.

To provoke a stuck-at-1 fault at the input of a complementary CMOS logic gate and propagate the fault effect to the output of the logic gate, the stuck-at vector will place logical 0 at the input of a PMOS transistor whose gate is connected to the faulty input node and the inputs of any other PMOS transistors that are located in the same transistor stack as this PMOS transistor. In this way, the vector connects the output of the logic gate to the supply voltage through the PMOS transistor whose input gate is connected to the faulty input node. Thus, the PMOS transistor is put into the stress condition

described above. To provoke a stuck-at-0 fault at the input of a complementary CMOS logic gate and propagate the fault effect to the output of the logic gate, the stuck-at vector will place logical 1 at the input of an NMOS transistor whose gate is connected to the faulty input node and the inputs of any other NMOS transistors that are located in the same transistor stack as this NMOS transistor. Similar to the vector for a stuck-at-1 fault at the input of the logic gate, the vector connects the output of the logic gate to ground through the NMOS transistor whose gate is connected to the faulty input node. As a result, the NMOS transistor is put into the stress condition mentioned above. Moreover, a 100% single stuck-at test of a complementary CMOS logic gate can toggle all input nodes of the logic gate. Therefore, a 100% stuck-at test set for a complementary CMOS logic gate puts each transistor in the required stress condition at least once. Either 100% single stuck-at test sets or pseudo stuck-at test sets can be used as the stress vectors for SHOVE. The latter are more useful than the former because of their shorter test lengths. A *pseudo stuck-at test set* consists of test vectors that provoke single stuck-at faults but propagate the fault effects only to the outputs of the logic gates in which the faults are located. 100% toggle test sets may miss some transistors. Figure 5-4 shows a fully complementary CMOS gate. Table 5-3 shows how transistors are stressed by stress vectors. The four italicized rows include a set of 100% stuck-at test set. For this example, the pseudo stuck-at test set is the same as the 100% stuck-at test set. All transistors are stressed by this stuck-at test set. If a toggle test set consists of input vectors 000 and 111, all the transistors can be stressed. However, if a toggle test set consists of input vectors 010 and 101 instead, transistor MPB and MPC are not stressed.

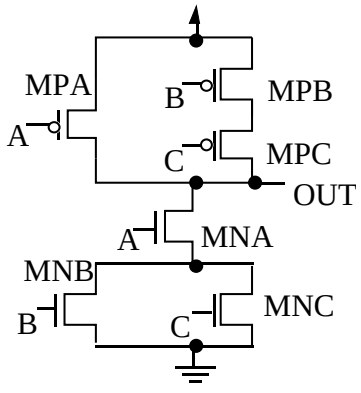

Figure 5-5 A Fully Complementary CMOS Logic Gate

Because not all transistors are stressed by each test vector, some transistors may be stressed longer than others after a test set is applied. Table 5-3 shows that all-zero

vectors can stress all PMOS transistors and all-one vectors can stress all NMOS transistors at once. To stress all transistors evenly and reduce the stress time for fully complementary CMOS logic gates, all-one and all-zero vectors can perform better than stuck-at test sets and pseudo stuck-at test sets as the stress vectors.

Because not all transistors are stressed by each test vector, some transistors may be stressed longer than others after a test set is applied. Table 5-3 shows that all-zero vectors can stress all PMOS transistors and all-one vectors can stress all NMOS transistors at once. To stress all transistors evenly and reduce the stress time for fully complementary CMOS logic gates, all-one and all-zero vectors can perform better than stuck-at test sets and pseudo stuck-at test sets as the stress vectors.

Table 5-3 Stress Vectors and the Stressed Transistors for a Fully Complementary CMOS Logic Gate

A	B	C	MPA	MPB	MPC	MNA	MNB	MNC
0	0	0	X*	X	X			
0	0	1	X					X
0	1	0	X				X	
0	*1*	*1*	*X*				*X*	*X*
1	*0*	*0*		*X*	*X*			
1	*0*	*1*				*X*		*X*
1	*1*	*0*				*X*	*X*	
1	1	1				X	X	X

* the transistor is stressed when the vector is applied

Because not all transistors are stressed by each test vector, some transistors may be stressed longer than others after a test set is applied. Table 5-3 shows that all-zero vectors can stress all PMOS transistors and all-one vectors can stress all NMOS transistors at once. To stress all transistors evenly and reduce the stress time for fully complementary CMOS logic gates, all-one and all-zero vectors can perform better than stuck-at test sets and pseudo stuck-at test sets as the stress vectors.

We can modify the algorithm for line justification used in existing ATPG programs to generate all-zero and all-one vectors. To justify the output value of a logic gate, the inputs of the logic gate should be set to either all ones or zeros. For example, if we want to set the output of a 2-input OR gate to be logical one, we should put logical

ones on both inputs of the gate. In existing ATPG programs, only one of the two inputs will be set to logical one.

For a CMOS domino circuit, an all-one vector is sufficient to put all transistors in a domino logic gate in the stress condition. The all-one vector does not include the clock signal. Moreover, we can stress all the transistors in a logic block consisting of domino logic by using only the all-one vector at the primary inputs of the domino logic block. Figure 5-5 shows a CMOS domino logic gate. Keepers can be put at proper internal nodes to ensure enough noise margin and avoid charge sharing problems [Colwell 95]. To simply the discussion, the keepers do not appear in the domino logic gate we used in this study. However, the conclusion can be extended to domino logic gates that have keepers implemented.

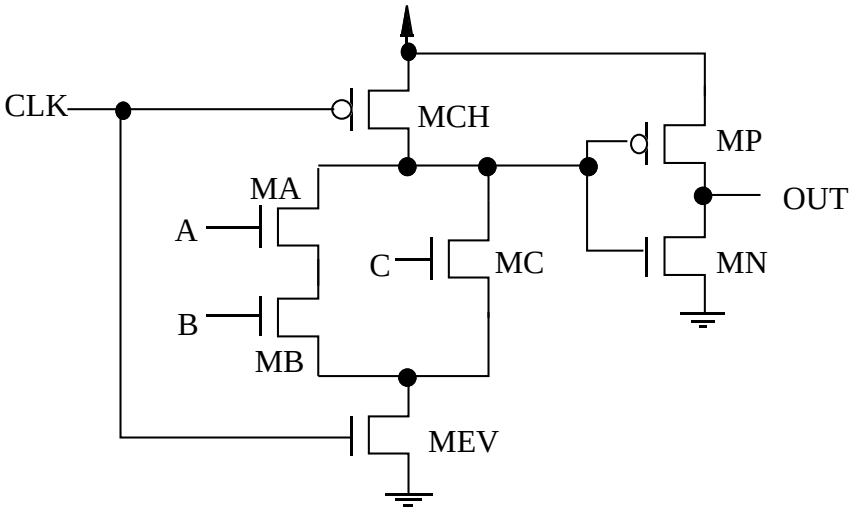

Figure 5-6 A CMOS Domino Circuit

During the precharge phase, the precharge PMOS transistor (transistor MCH in Fig. 5-5) and the NMOS transistor in the output inverter of a domino logic gate (transistor MN in Fig. 5-5) are stressed. During the evaluation phase, if all the inputs are logic one, all transistors in the evaluation branches (transistor MA, MB, MC, and MEV in Fig. 5-5) and the PMOS transistor in the output inverter of a domino logic gate (transistor MP in Fig. 5-5) are in the stress condition. Moreover, the output of the domino logic is logic one during the evaluation phase. Consequently, we can set the inputs of all domino circuits within a logic block to be logic one by putting all primary inputs of the logic block to logic one. Thus, only one vector is required to put all transistors within a logic

block consisting of domino logic in the stress condition. Table 5-4 summarizes the discussion of the stress vectors for CMOS domino logic.

Table 5-4 Stress Vectors for the CMOS Domino Circuit of Fig. 5-5

Input Condition	MCH	MEV	MP	MN	MA	MB	MC
Precharge Phase	X*			X			
Evaluation Phase with All-one at the Inputs		X	X		X	X	X

* the transistor is stressed during the described input condition

5.4 Stress Time and Stress Speed

Each transistor in a CMOS IC must be stressed for long enough to make sure the defective oxide deteriorates significantly so that either oxide breakdown or stress-induced oxide leakage occurs in the defective oxide. To optimize the effect of each stress vector and thus reduce the total stress time, each signal should be held at its full-swing signal level. In this way, transistors can be in the condition mentioned in Sec. 5.3 and thus be stressed efficiently by the stress vectors.

If a transistor can be set in the stress condition by more than one stress vector during SHOVE, we can reduce the overall stress time for a CMOS IC. Equation 5-3 shows the stress time of a CMOS IC, where T_{sl} is the overall stress time of a CMOS IC, n is the number of stress vectors, T_{st} is the stress time for each transistor at the applied stress voltage, and m is the minimum number of vectors that stress a transistor for all transistors in the CUT. T_{st} can be calculated by using Equation 5-1.

To determine an appropriate value for m, we investigated a CUT that was used in an experiment [Franco 95]. The CUT was implemented with only elementary CMOS logic gates. It has 380 gates, 24 inputs, 12 outputs, and 283 internal nodes. Seven 100% single stuck-at test sets and two pseudo stuck-at test sets were used in this study. We simulated all test sets and recorded how each node toggled.

$$T_{sl} = n \times T_{st} / m \qquad \textbf{Equation 5-3}$$

For the two pseudo stuck-at test sets, at least one node was in the logic zero state only once for all test vectors. Thus, m should be 1 for these two test sets. The stress speed for this CUT should be the reciprocal of the stress time for a transistor if pseudo

stuck-at test sets are used. For five out of the seven 100% single stuck-at test sets, each node was in the logic zero or logic one state at least twice. As a result, *m* can be set at two for these test sets. 97% of the nodes were in logic zero or logic one more than four times in all seven 100% single stuck-at test sets. To detect an oxide that is thinner than expected by 60%, the stress time for each transistor is 0.13 seconds when E_{ox} is 6MV/cm. The number of vectors for a pseudo stuck-at test set for this circuit is 26. The overall stress time should be 3.38 seconds.

As explained in the previous section, an all-one vector is sufficient to put all the transistors in the stress condition for CMOS domino circuits. Consequently, for CMOS domino circuits, we can hold the logic block in the precharge phase for the stress time of a transistor and then hold the primary inputs of the logic block in the logic one state for the same amount of stress time during the evaluation phase.

The *stress speed* is the operating frequency during SHOVE. To shorten the overall stress time and maximize the stress effect, each vector should be held at its full-swing value for the stress time of a transistor. Consequently, the stress speed should be reciprocal of the stress time of each transistor.

5.5 Summary

We have described which IC failures can be detected by SHOVE testing. SHOVE testing can detect most oxide defects and some via defects. Both defects can cause early-life failures and intermittent failures and thus reduce IC quality. Barrette *et al.* have found that there was no burn-in fallout for the wafer lots that had predominantly oxide defects and there was reduced burn-in fallout for the wafer lots that had predominantly via defects [Barrette 96]. Pseudo stuck-at test sets or stuck-at test sets can put all transistors of CUTs in the suggested stress conditions. The stress time can be determined by using the "effective oxide thinning" model and analyzing the test sets. The stress time can be shortened if multiple vectors can put transistors in their stress conditions more than once.

SHOVE testing, VLV testing, I_{DDQ} testing, and burn-in all aim at improving the quality level of CMOS ICs. Unlike SHOVE testing and burn-in, VLV testing and I_{DDQ} testing do not change the characteristics of the CUTs. VLV testing detects a weak part by distinguish its electrical characteristics at very low voltage from that at the normal operating voltage. The fault effect of the defect is not severe enough to fail the weak part at normal operating voltage but it becomes significant and thus fails the weak part at very low voltage. I_{DDQ} testing detects a defect by measuring the quiescent current of a CUT.

The fault effect of the defect may not cause Boolean failures but it increase the quiescent power supply current of the CUT.

We have shown that SHOVE testing can detect weak CMOS ICs caused by oxide defects and via defects. Although burn-in can accelerate most defects, it is expensive and delays product delivery. Some defects that can be accelerated more efficiently by voltage than by temperature do not require burn-in. For example, oxide defects have a large voltage activation energy but a small temperature activation energy. Because the defect population can change during the course of a process lifetime, it is not necessary to perform burn-in to ensure IC quality if the majority of the defects can be accelerated by voltage for a process window. SHOVE testing requires a shorter test time than burn-in and does not need extra instruments. Consequently, it is more efficient and economically viable than burn-in if most defects of a process is oxide defects instead of metalization defects. If the defects population of a process has a variety of defects and it is necessary to perform burn-in to improve the IC quality, SHOVE testing can be applied at wafer probe to reduce the number of parts for packaging and burn-in.

SHOVE testing should be applied after DC parametric tests and before any other tests. If the background current is too high to apply I_{DDQ} testing, we can replace it by VLV testing in the SHOVE procedure. VLV testing can detect the oxide defects that are accelerated by SHOVE.

Chapter 6

Experimental Validation

We performed a test chip experiment to evaluate the effectiveness of different test techniques, including VLV testing and I_{DDQ} testing. This chapter reports the experimental results for I_{DDQ} and VLV testing from the final package test. Appendix E describes the detailed experimental setup and results of the final package test. The design of the experiment and architecture of the test chip were described in [Franco 95]. Preliminary results based on only one clocking mode were also reported in [Ma 96]. In [Franco 96], we reported the experimental results for timing-dependent defects and also the defect population in each defect class. Based on the results from the wafer probe, we selected 309 dies for further investigation. These dies were assembled in 120-pin ceramic pin grid array packages and tested with an Advantest T6671E VLSI Test System. The Advantest T6671E VLSI Test System has a clock rate of 125MHz.

This chapter reports the experimental results of the final package test and discusses the correlation among I_{DDQ} failures, VLV-only failures, timing-independent combinational (TIC) defects, and non-TIC defects. We classified a die as having *I_{DDQ} failures* if its maximum I_{DDQ} measurement exceeded a current limit and we classified a die as having *VLV-only failures* if it passed all the sampling (Boolean) tests at the nominal supply voltage but failed some sampling tests at very low voltage. The behavior of a *combinational defect* depends only on the input pattern applied and does not depend on previous patterns. The behavior of a *timing-independent defect* does not depend on the clock speed (which is less than or equal to the rated speed) at the nominal operating voltage. A *timing-independent combinational (TIC) defect* has the properties of both a combinational defect and a timing-independent defect [Franco 96]. A defect that is either timing-dependent or pattern-dependent (non-combinational) is classified as a *non-TIC defect*. If the failure counts (including the counts of both the first failure and total failure) of a TIC defect matched those of a SSF, we classified it as an *SSF TIC defect*. Otherwise, it is a *non-SSF TIC defect.*

The test chip is manufactured by LSI Logic LFT150K FasTest array series. The nominal supply voltage is 5V and the effective channel length is 0.7μm. The test chip is a 25k gate CMOS gate array and has 96 I/O pins. There are five CUTs on the test chip. Two CUTs are datapath logic, MUL and SQR. The other three are control logic, STD,

ELM, and ROB. The three control logic CUTs perform the same function but are implemented in different ways [Franco 94] [Franco 95]. The five CUTs occupy approximately 50% of the chip area. The rest of the chip is occupied by test support circuitry.

We tested the CUTs at four test speeds at the nominal supply voltage. Besides the three test speeds used in the previous probe [Franco 95], we added a test speed that is at least three times lower than the rated test speed. We also tested the CUTs at three different supply voltages: 5V, 2.5V, and 1.7V. When testing at 2.5V and 1.7V, we used two test speeds at each voltage. One test speed is based on the Shmoo plot results. The other one is at least twice as slow. For two-pattern tests, the cycle time for the first vector in each vector pair was at least three times slower than the rated test speed.

6.1 Die Selection

We identified 149 "*interesting*" dies for further study based on the results from the first probe [Ma 95a] [Franco 96]. These include 125 dies that failed at least one sampling (Boolean) test at the nominal supply voltage, 23 dies that passed all the sampling tests at the nominal supply voltage but failed some VLV tests for either CUTs or test support circuitry, and one die that passed all the sampling tests at the nominal supply voltage and VLV tests but had I_{DDQ} values of more than 1mA in the first probe.

We found 128 failed CUTs for the sampling tests at the nominal supply voltage [Franco 96]. We define a defect in a CUT that passed the Stage 1 tests, which include DC parametric tests and test support circuitry tests, but failed at least one sampling test at the nominal supply voltage as a *CUT sampling failure*. Three dies had two failed CUT. Consequently, there were 125 dies that failed at least one CUT sampling tests at the nominal supply voltage. We define a CUT that passed all sampling tests at nominal supply voltage, passed the Stage 1 tests at very low voltage, but failed some sampling tests at very low voltage as a *CUT VLV-only failure.* Finally, we define a defect in a die that passed all sampling tests at nominal supply voltage but failed Stage 1 tests at very low voltage as a *test support circuitry VLV-only failure*. We found 12 CUT VLV-only failures and 11 test support circuitry VLV-only failures.

We used four wafers to investigate the anomalous I_{DDQ} measurement results from the wafer probe. On these four wafers, there are three dies that failed at least one CUT sampling tests at nominal supply voltage and three dies that had VLV-only failures. None of these six dies had more than one failing CUT for either sampling tests at nominal supply voltage or VLV tests. None of the dies on these four wafers were selected for the

final package test. Thus, we packaged 143 "interesting" dies, which included 122 dies that failed at least one CUT sampling test at nominal supply voltage, 20 dies that had VLV-only failures, and one die that passed all sampling tests at nominal supply voltage and VLV tests but had I_{DDQ} values of more than 1mA in the first probe. We also packaged 166 dies that passed all tests in the first probe. These 166 dies were carefully selected. Table 6-1 lists the summary of the packaged dies for the final package test.

Table 6-1 Summary of the Packaged Dies for the Final Package Test

defect class	total number of dies based on wafer probe results	number of packaged dies
CUT sampling failures	125	122*
VLV-only failures	23	20**
I_{DDQ} failures	NA	1
good dies	NA	166
total	NA	309

* Three out of the 125 dies were on the four wafers for studying anomalous I_{DDQ} results from the wafer probe

** Three out of the 23 dies were on the four wafers for studying anomalous I_{DDQ} results from the wafer probe

6.2 Experimental Setup

This section describes only the experimental setup that is related to I_{DDQ} and VLV testing. The detailed experimental setup can be found in Appendix E. The test plan for the final package test is similar to the one for the first probe. We used two-stage testing strategy in the final package test. Stage 1 tests consist of gross parametric tests and test support circuitry tests. Stage 2 tests consist of actual CUT tests, which include verification, exhaustive, pseudo-random, weighted-random, stuck-at, transition, path delay, gate delay, signature analysis, I_{DDQ}, and VLV tests. The test plan of the first probe can be found in [Franco 95], [Ma 95a], and [Franco 96]. For Stage 1 tests, we used the tests that were used in the first probe. We added new test sets and test conditions to the Stage 2 tests.

6.2.1 Supply Voltage

In the first probe, we ran all Boolean test sets at 5V and 1.7V. To investigate the effect of the supply voltage during testing on the test results, we added another supply voltage, 2.5V, in the final package test. We have shown that the supply voltage for VLV testing should be $2V_t$ to $2.5V_t$ [Chang 96a] [Chang 96b]. The test voltage 1.7V is within the proposed supply voltage. Only one extra supply voltage was added to keep the test time for each packaged unit short.

6.2.2 Test Timing

We applied the test sets at three different clock speeds in the first probe. A very slow test timing was added when we tested at nominal supply voltage in the final package test to differentiate timing-dependent defects from timing-independent defects. The very slow test timing is 3 times slower than the rated test timing. Table 6-2 lists the clock speeds used at nominal supply voltage.

Table 6-2 Clock Speeds at the Nominal Supply Voltage for the Final Package Test

test timing	clock speed
r-rated timing	rated (worst-case) speed of each CUT
s-slow timing	slower than rated timing (2/3 rated)
ss-very slow timing	much slower than rated timing (less than 1/3 rated)
f-fast timing	faster than rated timing (15% for MUL and SQR, 5% for others)

We used two clock speeds for all Boolean tests at 2.5V and 1.7V. A very slow test timing was used at each supply voltage to investigate which VLV-only failures are timing dependent. Tables 6-3 and 6-4 list the clock speeds used at 2.5V and 1.7V.

Table 6-3 Clock Speeds at 2.5V for the Final Package Test

test timing	clock speed
r-rated timing	1/3 rated speed at 5V
ss-very slow timing	1/6 rated speed at 5V

Table 6-4 Clock Speeds at 1.7V for the Final Package Test

test timing	clock speed
r-rated timing	1/5.6 rated speed at 5V
ss-very slow timing	1/8 rated speed at 5V

6.2.3 I_{DDQ} Measurements

We took special care during I_{DDQ} measurements. There are four input pins with pull-up resistors. These four pins are the control pins for the embedded CrossCheck array [Gheewala 89]. When we measured I_{DDQ} values, all four of these pins were tied to the supply voltage source of the tester to eliminate static current due to the voltage difference between V_{dd} and V_{IH}. The resolution of the current measurement was 2nA. The wait time before each I_{DDQ} measurement was 1ms. We have carefully characterized the wait time for each I_{DDQ} measurement so that there is no current fluctuation during the measurement.

6.3 Test Sets

Based on the results of the wafer probe, we added several test sets for the final package test. Some new test sets were contributed by the University of Iowa and the University of Southern California. We also used some updated commercial tools, such as Mentor Graphics and Sunrise's ATPG tools, to generate new test sets. To study the causes of pattern-dependent failures, we modified some of the original test sets. Below only the new test sets for I_{DDQ} and VLV testing are described. A detailed description of all new test sets used in the final package test can be found in Appendix E.

6.3.1 I_{DDQ} Test Sets

We added two types of I_{DDQ} test sets. One was generated by ATPG tools that use the pseudo stuck-at model. The vectors in the other type were selected from a set of functional vectors based on the pseudo stuck-at fault coverage of each vector. We measured and recorded the static current for each vector. A detailed description of the I_{DDQ} test sets can be found in Appendix E.

6.3.2 Exhaustive Test Sets

We added exhaustive test sets for the two low voltage tests in the final package test. The results of these exhaustive test sets can be used as references for the results from the two low voltage tests (1.7V and 2.5V).

6.4 Experimental Results

This dissertation focuses on I_{DDQ} measurement results and VLV test results. A detailed description of the experimental results can be found in Appendix E.

6.4.1 I_{DDQ} Measurements

Figure 6-1 illustrates the distribution of maximum I_{DDQ} of all CUTs. The Y axis is in the logarithmic scale. The *maximum* I_{DDQ} of each CUT is the maximum reading from all the measurements. The figure shows 1515 data points measured from 303 dies. There are six dies that failed the Stage 1 tests in the final package test. No data from these six dies are reported here.

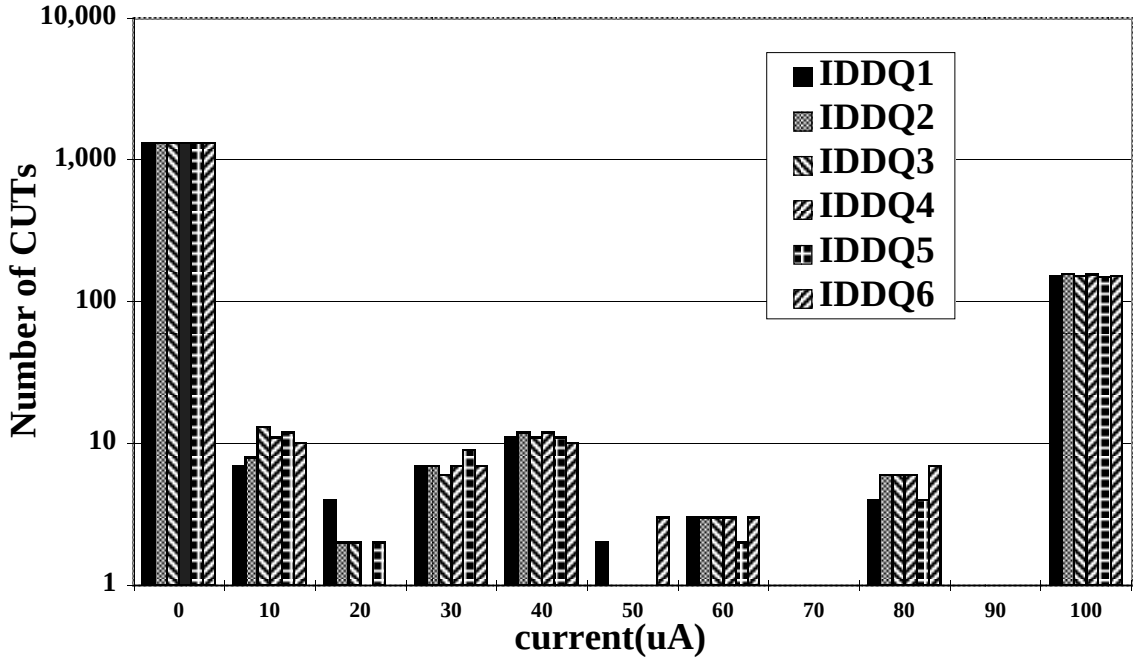

Figure 6-1 Maximum I_{DDQ} Distribution (in the Logarithmic Scale)

Figure 6-1 shows that the maximum I_{DDQ} distribution is similar among different test sets we applied. Although it shows that the I_{DDQ} measurements of most CUTs were either smaller than 10μA or larger than 100μA, we found that the maximum I_{DDQ} distribution of those CUTs whose maximum I_{DDQ} is larger than 100μA can be extended to 10mA. Figure 6-2 shows the maximum I_{DDQ} distribution of the CUTs whose maximum I_{DDQ} values are larger than 100μA. Consequently, it is difficult to determine the threshold of an I_{DDQ} test.

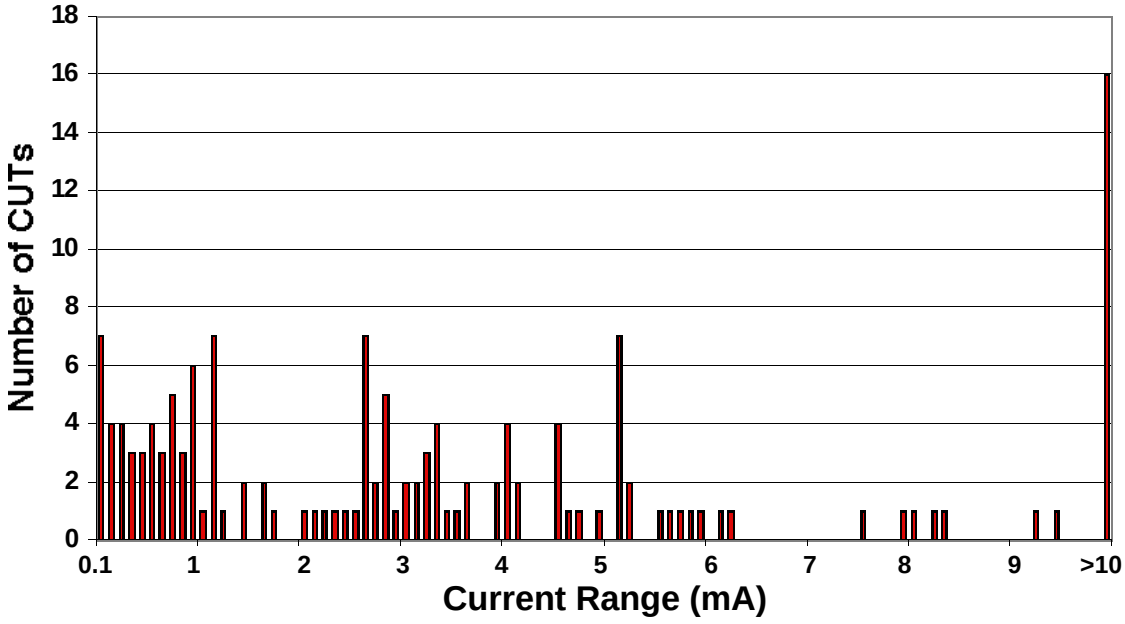

Figure 6-2 Maximum I_{DDQ} Distribution of I_{DDQ} Measurements Larger Than 100μA for IDDQ1 Test Set

Figure 6-3 shows the detailed maximum I_{DDQ} distribution of all 1515 CUTs shown in Fig. 6-1. Figure 6-4 shows the detailed maximum I_{DDQ} distribution of the 930 CUTs that passed all the Boolean tests applied at nominal supply voltage.

Figure 6-3 shows that the maximum I_{DDQ} values of 85% of all 1515 CUTs are below 3 μA. This observation is the same for at least two of the I_{DDQ} test sets applied in this experiment. Figure 6-4 shows that approximately 3.4% of the CUTs that passed all the Boolean tests at nominal voltage failed the I_{DDQ} test if the threshold of the I_{DDQ} test was set at 3μA.

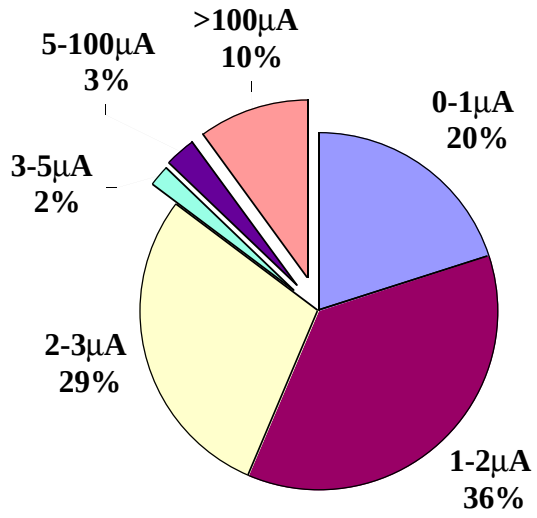

Figure 6-3 Maximum I_{DDQ} Distribution of All 1515 CUTs for IDDQ1 Test Set

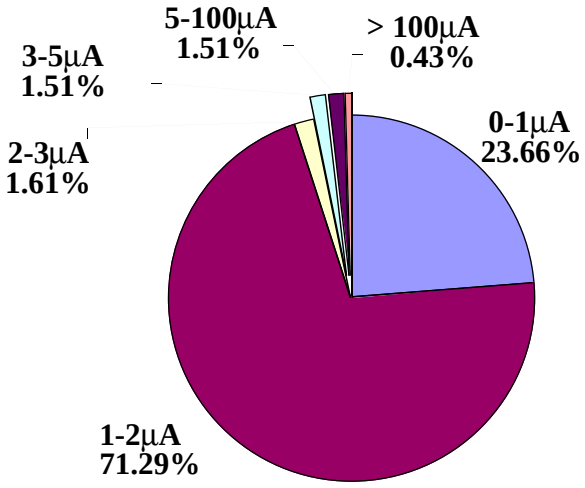

Figure 6-4 Maximum I_{DDQ} Distribution of the 930 CUTs that Passed All the Boolean Tests at Nominal Voltage for IDDQ1 Test Set

Table 6-5 shows the I_{DDQ} measurements for CUTs with different defect classes. The table shows only the CUTs that either were identified in some defect classes or had I_{DDQ} values larger than 3 μA. The last column in Table 6-5 lists the number of CUTs that had I_{DDQ} values within the current range but passed all other tests. This number could be larger than the ones listed in the table because we only packaged 309 dies and no I_{DDQ} information was available for selecting dies for the final package test.

Table 6-5 The Correlation between Defect Classes and I_{DDQ} Values

current range	TIC	SSF TIC	non-TIC	VLV-only	others
$I_{DDQ} \geq 100\ \mu A$	50	27	38	3*	2
$100\ \mu A > I_{DDQ} \geq 20\ \mu A$	3	3	7	5	9
$20\ \mu A > I_{DDQ} \geq 3\ \mu A$	3	3	2	0	20
$3\ \mu A > I_{DDQ}$	9	5	5	11**	NA

* 1 failed test support circuitry tests at very low voltage

** 9 failed test support circuitry tests at very low voltage

We reached the following conclusions based on the results in Table 6-5.

A. Not all non-TIC CUTs had high I_{DDQ} values. Thus, timing-dependent defects may not be detected by I_{DDQ} tests.

B. Although most defects could cause high I_{DDQ} currents, there were some that only slightly increased I_{DDQ} currents.

C. Only some VLV-only CUTs had high I_{DDQ} values. This indicates VLV tests and I_{DDQ} tests may detect different defects.

6.4.2 VLV Tests

We found 23 VLV-only failures based on the data from the first probe. Eleven of these failed support circuitry tests at very low voltage in the first probe. The other 12 failed CUT sampling tests. Ten out of the 12 CUT VLV-only failures and 10 out of the 11 test support circuitry VLV-only failures were packaged for the final package test. One of the 10 CUT VLV-only failures in the first probe passed all tests in the final package test. This could be due to wrong information on the wafer map for die selection. Table 6-6 lists the test results of the 9 CUT VLV-only failures in the final package test. We used the symbols of Tables 6-2, 6-3, and 6-4 to indicate the different clock speeds at each supply voltage. The symbol r is "rated" timing, s is "slow" timing, ss is "very slow" timing, and f is "fast" timing. "E" means "test escape for all tests applied." "F" means "at least failed some tests."

Table 6-6 Test Results of the 9 VLV-Only Failures

CUT	5V				2.5V		1.7V		maximum
	r	**s**	**ss**	**f**	**r**	**ss**	**r**	**ss**	I_{DDQ}
CUT1	E	E	E	F	F	E	F	F	66.4 μA
CUT2	E	E	E	F	F	E	F	F	65.6 μA
CUT3	F	E	E	F	F	F	F	F	> 800 μA
CUT4	E	E	E	F	E	E	F	F	47.2 μA
CUT5	E	E	E	F	E	E	F	F	51.6 μA
CUT6	E	E	E	E	E	E	F	F	2 μA
CUT7	E	E	E	F	E	E	F	E	717.6 μA
CUT8	E	E	E	F	F	E	F	F	2.8 μA
CUT9	E	E	E	F	F	F	F	F	81.0 μA

CUT3 failed exhaustive tests in the at-speed clocking mode but passed all the other test sets for the rated timing at 5V. The other CUT VLV-only failures had test escapes for all the tests at rated, slow, and very slow timings at nominal supply voltage. Most CUT VLV-only failures occurred at some tests for both rated and slow timings at 1.7V. Only one, CUT7, failed some tests for the rated timing but passed all tests for the slow timing. This CUT, however, had a high I_{DDQ} value, 717.6 μA. Consequently, it is a timing-dependent defect rather than a false alarm. The results also confirmed the rated speed at 1.7V, which we chose based on the Shmoo plot of a good device.

The results in Table 6-6 also show that testing at 1.7V was more effective than testing at 2.5V. Several test escapes occurred at 2.5V while all CUT VLV-only failures occurred at 1.7V. This result supports the supply voltage proposed for VLV testing in [Chang 96a] and [Chang 96b]. Two CUT VLV-only failures had I_{DDQ} values smaller than 3 μA. This indicates that VLV tests detect some defects that are not targeted by I_{DDQ} tests.

We added very slow timing in the final package test to investigate if test escapes could occur for the CUTs with timing failures when a test was run at very slow timing. Seven CUTs failed some tests for the rated timing at the nominal supply voltage but passed *all* the tests for very slow timing at the same supply voltage in the final package test. One CUT failed some tests for the rated timing at the nominal supply voltage but

passed *some* tests at very slow timing at the same supply voltage in the final package test. Figure 6-5 shows the characterization results of these eight CUTs.

Based on the results in Fig. 6-5, we reached the following conclusions:

A. Six out of these eight CUTs failed all the tests at 1.7V. This indicates that the effects of some timing-dependent defects are more visible at very low voltage.

B. Four out of these eight CUTs exhibited TIC defects at 1.7V. i.e., the defects that caused timing failures at nominal supply voltage can become TIC defects when tested at very low voltage.

C. Two out of these eight CUTs had test escapes at 1.7V. Some defects that caused timing failures at the nominal supply voltage had no faulty effects at very low voltage.

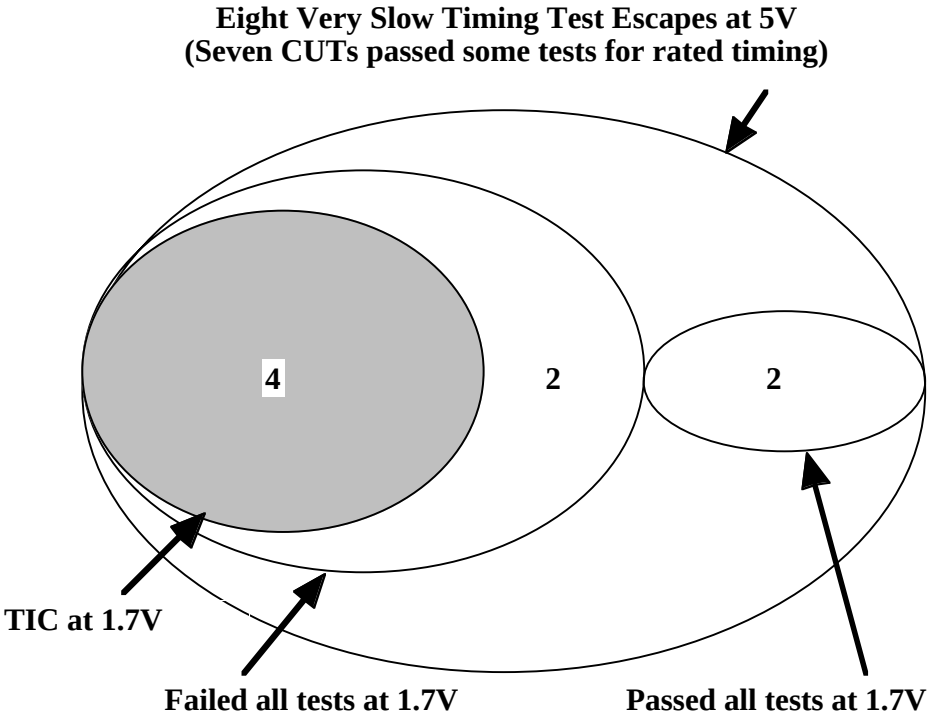

Figure 6-5 VLV Test Results for CUTs with Very-Slow Timing Test Escapes

6.5 Summary and Future Work

We presented the experimental setup and the experimental results for I_{DDQ} and VLV testing in the final package test of an experimental test chip. Although most CUT

failures had high I_{DDQ} values, some had only slightly elevated I_{DDQ} values. Some TIC, non-TIC, and VLV-only defects did not have elevated I_{DDQ} values.

We used two supply voltages for VLV tests. For each supply voltage, we used two clock speeds. We found that the supply voltage of VLV tests should be small enough to achieve the effectiveness of VLV tests. Many VLV-only failures occurred at 1.7V but did not show up at 2.5V. This validates the supply voltage for VLV testing proposed in [Chang 96a] and [Chang 96b]. By using different clock speeds at very low voltage, we also showed that the test speed selected based on the Shmoo plot of a good device is appropriate. Because not all VLV-only failures had high I_{DDQ} values, VLV tests may detect some defects that are not detected by I_{DDQ} tests. We also found that the effects of some timing-dependent defects were more severe at very low voltage.

We plan to apply SHOVE testing to the parts that have interesting results from the retest and some other parts that passed all the tests applied during the retest as control units. This experiment is designed to investigate the amount of stress time required for SHOVE testing. To investigate the reliability of the parts that have VLV-only failures, I_{DDQ}-only failures, and very-slow-timing escapes, we plan to burn in these interesting parts. In order to observe any possible changes to the characteristics of the interesting parts, we will thoroughly characterize these parts before and after 168-hour burn-in. We will apply accelerated life tests to the interesting parts that pass 168-hour burn-in. The burn-in results can be used to indicate the weakness of the interesting parts.

Chapter 7

Concluding Remarks

We have done a thorough study on two voltage screens, VLV testing and SHOVE testing, for detecting early-life failures in CMOS integrated circuits. We first examined existing methods for detecting early-life failures, burn-in and I_{DDQ} testing, and looked into the drawbacks of these two methods. Burn-in is very expensive in terms of the hardware costs and burn-in time. I_{DDQ} testing may not be practical in future deep submicron technologies because of the increasing background current. Depending on the applications, the devices that fail only I_{DDQ} tests can be determined as yield loss or reliability improvement. In our experiment, we found that approximately 3.4% of the CUTs that passed all the Boolean tests at nominal supply voltage failed only I_{DDQ} tests when the threshold of the I_{DDQ} tests was set at 3μA.

For the three major failure mechanisms in CMOS ICs, time-dependent dielectric breakdown (TDDB), hot carrier effects, and electromigration, the first one has a large voltage acceleration factor and small temperature activation energy, the second one has a negative temperature activation energy, and the third one has a large temperature activation energy but has no voltage dependence [Hnatek 95]. SHOVE testing is effective for TDDB, VLV testing is effective for hot carrier effects, and burn-in is effective for electromigration and TDDB.

Both VLV testing and SHOVE testing can be used at wafer sort. They can detect weak parts during a wafer-level test and remove the cost of packaging them. They can also reduce the number of parts for burn-in. SHOVE testing should be applied after DC parametric tests and before any other tests. If the background current is too high to apply I_{DDQ} testing, we can replace it by VLV testing in the SHOVE procedure. VLV testing can also detect oxide defects that are accelerated by SHOVE.

Neither I_{DDQ} testing nor VLV testing changes the characteristics of a CUT. VLV testing detects the flaws. For example, it can detect resistive shorts, threshold voltage shifts, and transmission gate opens. VLV testing is non-destructive to flawless circuits. On the other hand, SHOVE testing detects weak parts by changing their characteristics and shortening their lifetime. Neither SHOVE testing nor burn-in should shorten the lifetime of a flawless circuit significantly.

Table 7-1 lists the summary of the discussion of the four test techniques, VLV testing, SHOVE testing, I_{DDQ} testing, and burn-in. I_{DDQ} testing requires extra hardware to speed up the measurement and ensure its accuracy. It is not applicable to wafer sort if there are decoupling capacitors on the probe card.

Table 7-1 Summary of VLV testing, SHOVE testing , I_{DDQ} testing, and Burn-in

	VLV	SHOVE	I_{DDQ}	Burn-in
Stress technique?	No	Yes	No	Yes
Most effective for? (failure mechanisms)	Hot carrier effects, TDDB*	TDDB	TDDB	Electromigration, TDDB
Most effective for? (flaws)	Resistive shorts, diminished-drive, degraded signals	Oxide defects, via defects	Resistive shorts, degraded signals	Metalization defects, oxide defects, contamination
Wearout accelerated?	No	Yes	No	Yes
Voltage?	$2V_t$ to $2.5V_t$	VDD1†	VDD2††	VDD1 or VDD3†††
Extra hardware?	No	No	Yes**	Yes
Applicable during wafer sort?	Yes	Yes	Yes***	No
Destructive?	No	Yes	No	Yes

* time-dependent dielectric breakdown

** requires special hardware to speed up the current measurement and ensure its accuracy

*** cannot be used during wafer sort if decoupling capacitors exist on the probe card

† VDD1: the highest non-destructive voltage

†† VDD2: the nominal operating voltage or the high voltage corner of the specification (for example, 5% higher than the nominal operating voltage)

††† VDD3: the highest operating voltage (the circuit is still functional)

VLV testing should be carried out with the supply voltage between $2V_t$ and $2.5V_t$. SHOVE testing should be applied at the highest non-destructive voltage. I_{DDQ} testing should be applied at the nominal operating voltage or the high voltage corner of the specification (for example, 5% higher than the nominal operating voltage). Depending on the burn-in procedure, the supply voltage should be the highest operating voltage if

the CUTs are tested during burn-in and it can be the highest non-destructive voltage if no tests are applied during burn-in.

VLV testing is effective for flaws that cause early-life failures or intermittent failures. It does not add to the cost of an IC in either area or performance. Furthermore, it is non-destructive and does not require the increased time for burn-in and I_{DDQ} testing. Based on the differences in the electrical characteristics at different supply voltages, VLV testing can detect some defects that are undetectable at normal supply voltage.

We have shown that the supply voltage for VLV testing should be between $2V_t$ and $2.5V_t$, where V_t is the threshold voltage of a transistor. The supply voltage can be adjusted within this range to accommodate practical considerations, such as the magnitude of the external noise around the test environment and the accuracy limitation of the automatic test equipment at very low voltage. We also investigated the effectiveness of VLV testing for low-voltage technologies. By using $2V_t$ as the supply voltage during testing, we achieved reasonable flaw coverage for gate oxide shorts and metal shorts.

Most timing defects are due to degraded signals or transistors with lowered driving capabilities. We have shown that VLV testing can detect the timing defects caused by degraded signals or by gates that have lower driving capabilities than they are designed for. The supply voltage for VLV testing for detecting delay flaws should be set in the region where the change rate of the propagation delay of a CMOS gate starts increasing significantly. We found that the change rate of the propagation delay of a CMOS inverter starts increasing when the supply voltage is between $2V_t$ and $2.5V_t$. Consequently, by setting the supply voltage to be $2V_t$ to $2.5V_t$, VLV testing is also most effective in detecting delay flaws.

VLV testing can also be used to improve the defect coverage of gate oxide shorts for CMOS domino circuits. We found that most gate oxide shorts with low resistance in a CMOS domino circuit can be detected by Boolean tests at normal supply voltage. Only one gate oxide short requires a two-pattern test for detection. For inter-gate resistive shorts, the defect coverage can be improved by either setting the supply voltage 40% higher than the normal operating voltage or by lowering the supply voltage to $2V_t$ for the technologies used in this study. Keepers should be used in all CMOS domino circuits to improve their testability. Not only can keepers eliminate leakage and noise problems, they also remove the floating node problem in CMOS domino circuits and thus make CMOS domino circuits more testable. Keepers also make CMOS domino circuits consume very small static currents and make them I_{DDQ} testable.

SHOVE testing can detect most oxide defects and some via defects. Both defects can cause early-life failures and intermittent failures and thus reduce IC quality. Researchers have shown that there was no burn-in fallout after SHOVE testing for wafer lots that had predominantly oxide defects. Pseudo-SSF test sets or SSF test sets can put all transistors of CUTs in the stress conditions described in this dissertation. One can determine the stress time for SHOVE by using the "effective oxide thinning" model and analyzing the test sets. The stress time can be shortened if multiple vectors can put transistors in their stress conditions more than once.

The experimental results from the final package test of a test chip experiment validates the supply voltage proposed for VLV testing. We found that the supply voltage must be low enough to make VLV testing effective. The experimental results also show that the effects of some timing-dependent failures become more severe at very low voltage. Some timing-dependent failures become TIC defects at very low voltage.

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Appendix A

Quantitative Analysis of Very-Low-Voltage Testing

Proceedings of VLSI Test Symposium, pp. 332-337, 1996

Appendix B

Detecting Delay Flaws by Very-Low-Voltage Testing

Proceedings of International Test Conference, pp. 367-376, 1996

Appendix C

Testing Resistive Shorts in CMOS Domino Circuits

This appendix includes the detailed discussion of testing intra-gate and inter-gate resistive shorts in CMOS domino circuits. The results are summarized in Chapter 4.

C.1 Intra-Gate Resistive Shorts

We used the four shorts listed in the CrossCheck fault model. In addition, we considered shorts with high and low resistance.

C.1.1 Shorts within a FET (SHF)

We injected gate oxide shorts in a 4-input AND gate. Figure C-1 shows the simulated CMOS domino gate. During simulations, the 4-input AND gate was followed by a 2-input OR gate. Figure C-2 shows the simulation setup. All the inputs, except the clock signal, were buffered by CMOS domino buffers. The clock signals were buffered by static CMOS buffers. The OR gate was properly loaded. We assumed that the output is observable only in the evaluation phase. The 0.6 μm technology, whose normal operating voltage is 3.3V, was used for all simulations discussed in this section. The nominal threshold voltage for an NMOS transistor is 0.59V.

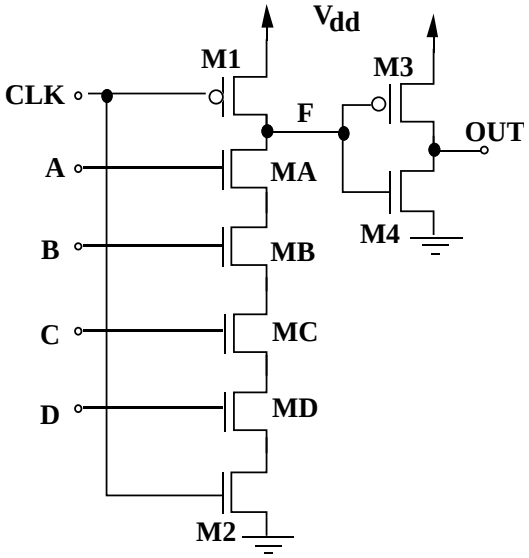

Figure C-1 4-Input AND Gate

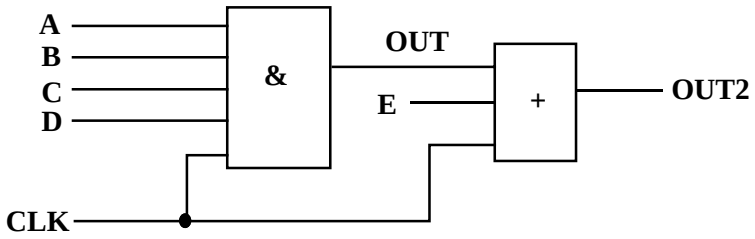

Figure C-2 Simulation Setup

Gate-drain short in MA (Fig. C-1)

We should set A to be zero during the evaluation phase to provoke this defect. During the precharge phase, there is a conducting path between V_{dd} and ground through the short, the precharge PMOS transistor, and the NMOS transistor in the inverter of the preceding domino gate. If the short has very small resistance, the voltage level at the dynamic node in the defective gate is close to zero. The output of the defective gate is one and that of a defect-free gate is zero. If A is set to be zero during the evaluation phase, the charge at the dynamic node in the defective gate can discharge through the short. Thus, for a gate-drain short with small resistance, the output of the defective gate will switch to one and that of a defect-free gate remains zero. The erroneous transition should finish within a cycle and we should therefore be able to detect the short. The signal at the output of a defective gate starts switching right after the clock signal goes high at the beginning of the evaluation phase. If the defective gate is the first gate in a critical path, the time from the rising edge of the clock signal to when the erroneous transition occurs at the output of the defective gate should be shorter than the propagation delay of a defect-free gate for successful detection. Table C-1 lists this time for shorts with different resistances.

The propagation delay of a defect-free gate is 384 ps for the simulated technology. The results in Table C-1 show that the defect coverage of a gate-drain short by a Boolean test at normal operating voltage is at least 5 KΩ. The rows with bold numbers and characters indicate the resistive shorts that are detectable by Boolean tests at normal operating supply voltage. Researchers have reported that 98.3% of bridging defects have resistance less than 5 KΩ for a CMOS process [Rodriguez 92].

Table C-1 Time to an Erroneous Transition for Different Short Resistances

Short Resistance	Delay
1 KΩ	**OUT stuck-at-one**
2 KΩ	**164 ps**
3 KΩ	**219 ps**
4 KΩ	**266 ps**
5 KΩ	**310 ps**
6 KΩ	**352 ps**
7 KΩ	393 ps

We can improve the defect coverage by reducing the operating voltage during testing. At low voltages, the equivalent resistance of a transistor increases while the resistance of a short remains almost the same [Hao 93a] [Chang 96a]. Consequently, the fault effect of a resistive short is more significant at low voltages. For the defective gate discussed in this section, the voltage at the dynamic node is close to zero at low voltage for a short with large resistance. Thus, the defect behaves like a stuck-at-one fault at the output of the CMOS domino gate. Table C-2 lists the defect coverage of the gate-drain short at different supply voltages. For the tables presented in this section, the bold and italicized rows indicate the supply voltage range proposed for VLV testing [Chang 96a] [Chang 96b].

Table C-2 Defect Coverage of a Gate-Drain Short in MA at Different Supply Voltages

V_{dd}	V_{dd} / V_t	Defect Coverage
1.2V	***2.0***	***≤ 20 KΩ***
1.5V	***2.5***	***≤ 17 KΩ***
1.7V	2.9	≤ 14 KΩ
2.0V	3.4	≤ 11 KΩ
2.5V	4.2	≤ 9 KΩ
3.3V	5.6	≤ 5 KΩ

The gate-drain shorts in the other NMOS transistors in the evaluation network behave similarly to the gate-drain short in MA during the evaluation phase. The difference is that the shorts in the other transistors do not cause any fault effect during the precharge phase. However, they can be detected in a similar way. The test vectors that detect a stuck-at-one fault at the output of a CMOS domino gate can provoke a gate-drain short in MA. The test vectors that detect a stuck-at-one fault at the inputs of a CMOS domino gate can provoke a gate-drain short in the other transistors, MB, MC, and MD, in the evaluation network.

Gate-source short in MA (Fig. C-1)

We should set A to be one during the evaluation phase to provoke the defect. To sensitize the fault effect to the output of the domino gate, the other input signal should also be set to one during the evaluation phase.

If the short resistance is low, e.g., 1 KΩ, the voltage level at node A can be pulled below the threshold voltage of an NMOS transistor at normal operating supply voltage. The dynamic node cannot be discharged during the evaluation phase and the defect behaves as a stuck-at-zero fault at the input node of the defective transistor. However, for large short resistance, the defect can only increase the propagation delay of the defective gate.

The fault effect of the gate-source short can become more significant at voltages well below the normal operating voltage. Defects with high short resistance can behave like stuck-at faults or large delay faults. Thus, the defect coverage of the short improves significantly at very low voltage. Table C-3 lists the defect coverage of the short at different supply voltages.

Table C-3 Defect Coverage of a Gate-Source Short in MA (Fig. C-1) at Different Supply Voltages

V_{dd}	V_{dd} / V_t	Defect Coverage
1.2V	***2.0***	***≤ 13 KΩ***
1.5V	***2.5***	***≤ 6.4 KΩ***
1.7V	2.9	≤ 4.6 KΩ
2.0V	3.4	≤ 3.1 KΩ
2.5V	4.2	≤ 2.0 KΩ
3.3V	5.6	≤ 1.2 KΩ

The gate-source shorts in the other NMOS transistors in the evaluation network behave similarly to the one in MA. They can be provoked by the same test vector and the defect coverage at different supply voltages is similar to the results in Table C-3.

Gate-source short in M3 (Fig. C-1)

We should set all the inputs of a CMOS domino gate to be one during the evaluation phase to provoke the defect. For a defect with low short resistance, the defect behaves like a stuck-at-one fault at the output of the defective CMOS domino gate. However, the short can only increase the propagation delay of the defective gate if it has high resistance. The defect coverage of this short can also be improved by using VLV Testing. Table C-4 lists the defect coverage of the short at different supply voltages.

Table C-4 Defect Coverage of a Gate-Source Short in M3 (Fig. C-1) at Different Supply Voltages

V_{dd}	V_{dd} / V_t	Defect Coverage
1.2V	***2.0***	***≤ 15 KΩ***
1.5V	***2.5***	***≤ 8.2 KΩ***
1.7V	2.9	≤ 6 KΩ
2.0V	3.4	≤ 4.4 KΩ
2.5V	4.2	≤ 3.1 KΩ
3.3V	5.6	≤ 2.1 KΩ

Gate-source short in M4 (Fig. C-1)

We should set the inputs of the CMOS domino gate so that the output node will not switch during the evaluation phase. The defect behaves like a stuck-at-one fault at the output of the CMOS domino gate. The short provides a path between the dynamic node and ground. Consequently, the charge at the dynamic node will discharge right after the domino gate enters the evaluation phase. The defect coverage of a Boolean test at normal operating supply voltage is larger than 15 KΩ.

Gate-drain short in either M3 or M4 (Fig. C-1)

We should set the inputs of a CMOS domino gate in such a way that its output node will not switch during the evaluation phase. The defect coverage of a Boolean test

at normal supply voltage is larger than 10 KΩ. Although we can also provoke the defect by setting the inputs of a CMOS domino gate so that its output will switch from zero to one, the fault effect is that the following gate has a degraded V_{ih}. The defective gate can still function correctly. Sometimes, it can even switch faster than a defect-free gate. There is no way to distinguish a defective gate from a defect-free gate in this case.

Gate-drain short in M1 (Fig. C-1)

We should set the inputs of a CMOS domino gate and its following domino gate so that their outputs will not switch during the evaluation phase. The fault effect can only be observed at the output of the following CMOS domino gate. If the short resistance is small, e.g., 500 Ω, the dynamic node stays at zero during the precharge phase. The output of the CMOS domino gate is one before the gate enters the evaluation phase. When the clock goes high at the beginning of the evaluation phase, the dynamic node can be charged to V_{dd} through the short. The output of the defective domino gate can switch to its defect-free value, zero. Before the output node returns to its defect-free value, the following domino gate has been triggered by the erroneous logic value at the output of the defective domino gate right after the clock has gone high. Thus, we can observe the fault effect at the output of the domino gate following the defective domino gate. If the short resistance is large, the dynamic node in a defective CMOS domino gate can still be charged to V_{dd} during the precharge phase. The output of the defective gate can stay at zero during both the precharge and the evaluation phase. Hence, the gate-drain short in M1 with large resistance cannot be detected by a Boolean test at normal operating voltage. However, the short can be detected at very low voltage. This is because the fault effect of the short with large resistance becomes significant at very low voltage. The same mechanism that occurs for shorts with low resistance at normal supply voltage occurs for shorts with high resistance at very low voltage. Table C-5 lists the defect coverage of the short at different supply voltages.

If the defective gate is followed by a latch or a static CMOS gate, the short cannot be detected. Although the short can also be provoked by setting all the inputs of the defective gate to one, it can cause only a very small delay fault if the resistance is high. The propagation delay of a defective gate is 16% longer than that of a defect-free gate. If the resistance is low, the defect can cause the defective gate to switch even faster than a defect-free gate. This is because the dynamic node cannot be charged to V_{dd} during the precharge phase. Consequently, it takes a shorter time to discharge the dynamic node in a defective gate than in a defect-free gate. On the other hand, it is unlikely that the short can cause the defective CUT to malfunction if the defective gate is followed by a latch or

a static CMOS gate. For a short with low resistance, the output of the defective domino gate will either be a correct logic value or the gate will switch faster than a defect-free one. For a short with high resistance, the output of the defective domino gate will also either be a correct logic value or the gate will switch slightly slower than it is supposed to.

Table C-5 Defect Coverage of a Gate-Drain Short in M1 (Fig. C-1) at Different Supply Voltages

V_{dd}	V_{dd} / V_t	Defect Coverage
1.2V	***2.0***	***≤ 14 KΩ***
1.5V	***2.5***	***≤ 5.1 KΩ***
1.7V	2.9	≤ 3.7 KΩ
2.0V	3.4	≤ 2.6 KΩ
2.5V	4.2	≤ 1.9 KΩ
3.3V	5.6	≤ 1.5 KΩ

Gate-source short in M1 (Fig. C-1)

This is the only short in a CMOS domino gate that requires a two-pattern test for detection. The first pattern should discharge the dynamic node and thus set the output of the domino gate to be one in the evaluation phase. The second pattern should be set so that the output of the domino gate does not switch from zero to one during the evaluation phase. If the short has small resistance, it can effectively turn off the precharge PMOS transistor during the precharge phase. Consequently, the dynamic node cannot be charged to V_{dd} in the second cycle. The output of a defective gate should remain at V_{dd} in the second cycle. If the resistance of the short is large, the dynamic node can still go to V_{dd} during the precharge phase. Consequently, a defective CUT with large short resistance can still function correctly at normal operating voltage. The defect coverage can be improved by testing the CUT at very low voltage. At very low voltage, the fault effect of the short with large resistance becomes so significant that the PMOS precharge transistor is turned off during the precharge phase. Thus, the defect can be detected in the second cycle. Table C-6 lists the defect coverage of a gate-source short in M1 at different supply voltages.

Table C-6 Defect Coverage of a Gate-Source Short in M1 (Fig. C-1) at Different Supply Voltages

Vdd	Vdd / Vt	Defect Coverage
1.2V	***2.0***	≤ ***2.6 KΩ***
1.5V	***2.5***	≤ ***1.1 KΩ***
1.7V	2.9	≤ 0.5 KΩ
2.0V	3.4	≤ 0.5 KΩ
2.5V	4.2	≤ 0.3 KΩ
3.3V	5.6	≤ 0.2 KΩ

Gate-drain short and gate-source short in M2 (Fig. C-1)

To detect either of the shorts, we should set the inputs so that the output of a CMOS domino gate switches from zero to one during the evaluation phase. If the resistance of the short is very small, it can prevent the dynamic node from discharging. Thus, the defect behaves as a stuck-at 0 fault at the output of a CMOS domino gate. However, the defect coverage is poor at normal operating voltage. We can improve the defect coverage of either short by reducing the supply voltage during testing. Table C-7 lists the defect coverage of a gate-drain short and a gate-source short in M2 at different supply voltages.

Table C-7 Defect Coverage of a Gate-Drain Short and Gate-Source Short in M2 (Fig. C-1) at Different Supply Voltages

		Defect coverage	
Vdd	Vdd / Vt	gate-drain short	gate-source short
1.2V	***2.0***	≤ ***5.3 KΩ***	≤ ***5.0 KΩ***
1.5V	***2.5***	≤ ***1.7 KΩ***	≤ ***1.7 KΩ***
1.7V	2.9	≤ 1.0 KΩ	≤ 1.1 KΩ
2.0V	3.4	≤ 0.6 KΩ	≤ 0.8 KΩ
2.5V	4.2	≤ 0.3 KΩ	≤ 0.5 KΩ
3.3V	5.6	≤ 0.2 KΩ	≤ 0.3 KΩ

C.1.2 Shorts between an Interconnect and Power (STP)

If an STP occurs at the input or output node of a CMOS domino gate, the domino gate behaves as if it had a stuck-at-one fault at either its input or output. An STP at the dynamic node also behaves as a stuck-at fault. If an STP occurs at the clock signal line, the domino gate cannot be precharged to V_{dd} during the precharge phase. Thus, it behaves like a stuck-at-one fault at the output of the domino gate. An STP at the drain node of the NMOS evaluation transistor or at the dynamic node can disable the dynamic node to discharge. Consequently, it behaves like a stuck-at-zero fault at the output of the domino gate.

An STP at one of the nodes in the NMOS evaluation network behaves like a stuck-at-zero fault at the gate node of the NMOS transistor whose drain node has the STP. For example, if there is an STP at the drain node of the MB transistor in Fig. C-1, it behaves like a stuck-at-zero fault at node B.

C.1.3 Shorts between an Interconnect and Ground (STG)

If an STG exists at the input or output node of a CMOS domino gate, it behaves like a stuck-at-zero fault at the input or output node of the domino gate. An STG at the gate or drain node of the PMOS precharge transistor in a CMOS domino gate causes the output of the domino gate to be stuck at zero in the evaluation phase. An STG at the dynamic node of a CMOS domino gate behaves like a stuck-at-one fault at the output of the domino gate. If an STG occurs at the gate node of the NMOS evaluation transistor, it prevents the dynamic node of the domino gate from discharging. Thus, it behaves as a stuck-at-zero fault at the output of the domino gate. An STG at the drain node of the NMOS evaluation transistor can only increase the power consumption of the domino gate. This STG cannot cause the domino gate to fail functionally.

An STG in the NMOS evaluation network can be detected by a vector for the stuck-at-one fault at the gate node of the NMOS transistor whose drain node has the STG. Figure C-3 shows an STG in the NMOS evaluation network of a CMOS domino gate. By setting A to be 1 and B to be 0 in the evaluation phase, the charge on the dynamic node of a defective domino gate discharges through MA to ground. On the other hand, the charge on the dynamic node of a defect-free domino gate is not discharged. Although the defect does not behave exactly the same as the stuck-at-one fault at node B, the vector for the stuck-at-one fault at node B can provoke it.

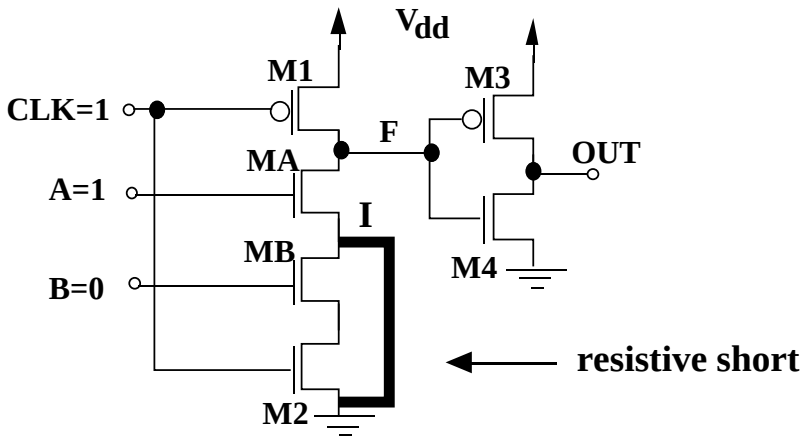

Figure C-3 An STG Short in the NMOS Evaluation Network

C.1.4 Shorts between Two Interconnects within the Cell (SHI)

Below, all SHIs in CMOS domino gates are analyzed one by one.

Short between an input and a source node of any NMOS transistor in the evaluation network

If the NMOS transistor with the faulty input and the NMOS transistor with the faulty source node are in the same transistor stack, the short can be detected in the same way a gate-source short in any NMOS transistor in the evaluation network can be detected. This has been shown in Sec. C.1.1.

However, if the two defective NMOS transistors are not in the same transistor stack, as shown in Fig. C-4, there is no equivalent or dominant single stuck-at fault for the SHI. By applying the vector shown in Fig. C-4, we can discharge the charge on the dynamic node through MA and the SHI to ground. Consequently, the output node of a defective gate becomes V_{dd} and that of a defect-free gate remains at 0V. However, the vector for detecting this SHI is not a single stuck-at fault vector. The defect coverage of this SHI at different supply voltages is similar to that of a gate-drain short in MA of Fig. C-1, which has been discussed in Sec. C.1.1.

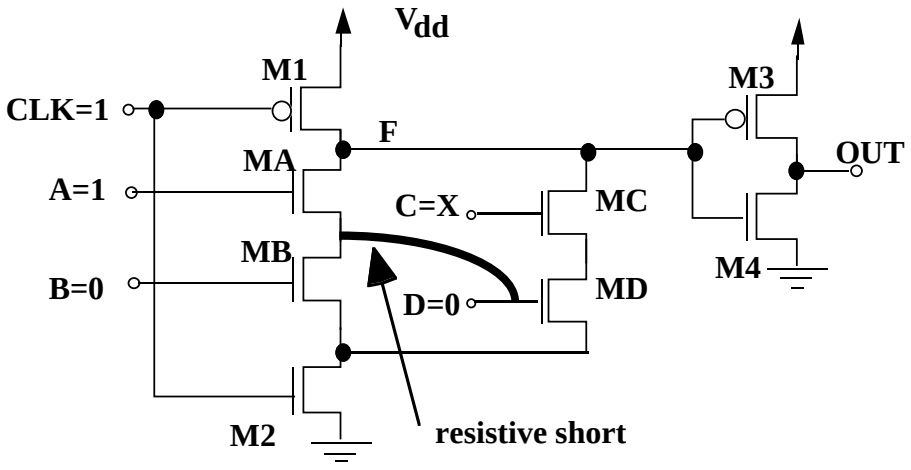

Figure C-4 An SHI between an Input Node and the Source Node of an NMOS Transistor in the Evaluation Network

Short between the output and a source node of any NMOS transistor in the evaluation network

Figure C-5 shows an SHI between the output node of a CMOS domino gate and the source node of an NMOS transistor in the evaluation network. To detect the SHI, we can set the input of all the NMOS transistors between the dynamic node and the defective node to be 1 and the rest of the inputs to be 0. There is no fault effect during the precharge phase. During the evaluation phase, the charge at the dynamic node can discharge through MA, MB, and the short to the output node. Because the sizes of M3 and M4 are usually skewed so that the output node is very sensitive to the voltage level at the dynamic node, the output node of the defective domino gate rises quickly after that at the dynamic node falls. The output node cannot switch to its full-swing value and can only have a degraded signal instead. Nevertheless, the degraded signal can make the next domino gate switch erroneously. The defect coverage of the SHI at the nominal supply voltage is larger than 10 KΩ. Although the SHI can be detected by only one vector, the vector is not a single stuck-at fault vector.

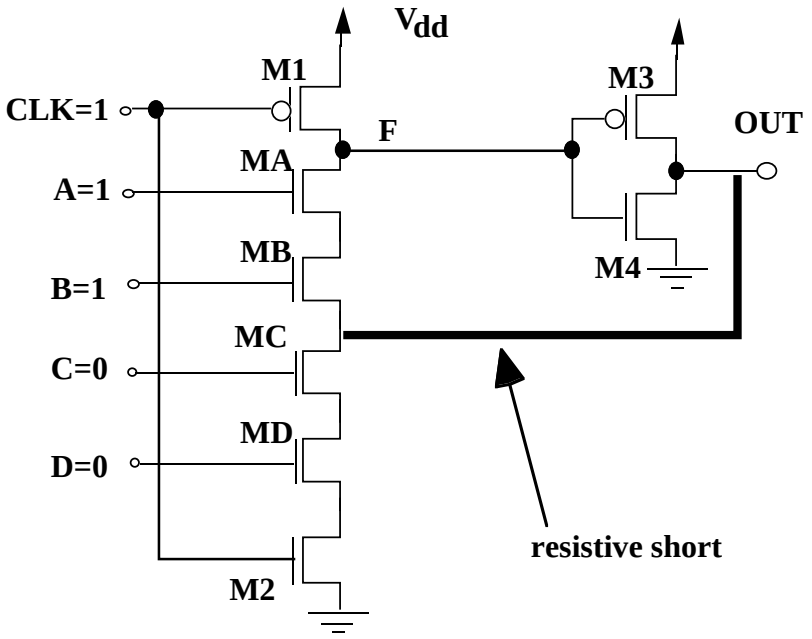

Figure C-5 An SHI between the Output Node and the Source Node of an NMOS Transistor in the Evaluation Network

Output-dynamic node

An SHI between the output node and the dynamic node of a CMOS domino gate behaves like a gate-drain short in M3 or M4 in Fig. C-1, which has been discussed in Sec. C.1.1.

Input-output

An SHI between an input node and the output node of a CMOS domino gate turns the CMOS domino gate into a buffer to the defective input node. It can be detected by applying a vector that can distinguish between the function of a defective domino gate and that of a defect-free domino gate.

Short between the source nodes of two NMOS transistors in the evaluation network

An SHI between two nodes in the evaluation network of a CMOS domino gate changes the function of the defective domino gate. If the SHI connects two nodes in the same transistor stack, it behaves as a stuck-at-one fault at the gate node of any NMOS transistor between the short. For example, if there is a short between the source node of MA and the source node of MC in Fig. C-1, the SHI behaves as a stuck-at-one fault at either B or C. If the SHI connects two nodes between two different transistor stacks, we

can detect the short by applying the vector that distinguishes the Boolean function of the defective gate from that of a defect-free gate.

Clock signal-output

An SHI between the clock signal and the output node in a CMOS domino gate behaves as a stuck-at-one fault at the output node of the domino gate in the evaluation phase.

Clock signal-dynamic node

An SHI between the clock signal and the dynamic node of a CMOS domino gate is the same short as a gate-drain short in M1 in Fig. C-1, which has been discussed in Sec. C.1.1.

Clock signal-input

An SHI between the clock signal and any of the input node of a CMOS domino gate behaves as a stuck-at-one fault at the faulty input node during the evaluation phase.

Clock signal-drain node of the NMOS evaluation transistor

An SHI between the clock signal and the drain of the NMOS evaluation transistor is the same as a gate-drain short in M2 in Fig. C-1, which has been discussed in Sec. C.1.1.

Clock signal-drain node of any NMOS transistor in the evaluation network

An SHI between the clock signal and the drain of any NMOS transistor in the evaluation network behaves similar to an STP at the drain node of the defective NMOS transistor in the evaluation phase. Consequently, it behaves as a stuck-at-zero fault at the gate node of the defective NMOS transistor in the evaluation phase.

C.1.5 Summary

In summary, All but one gate oxide short in a CMOS domino gate can be provoked by the test vectors for stuck-at pin faults. Only one short, the gate-source short in the precharge PMOS transistor, requires a two-pattern test. We can improve the defect coverage of gate oxide shorts by using VLV Testing [Hao 93a]. Based on the data shown in Tables C-2, C-3, C-4, C-5, C-6, and C-7, the supply voltage for VLV Testing should be set between $2V_t$ and $2.5V_t$ [Chang 96a] [Chang 96b].

All STPs and STGs and most SHIs in CMOS domino gates can be detected by single stuck-at test vectors. There are two types of SHIs in CMOS domino gates that cannot be detected by single stuck-at test vectors. Nevertheless, they can still be detected by a vector at the nominal supply voltage.

C.2 Inter-Gate Resistive Shorts

We can improve the defect coverage of inter-gate resistive shorts in a CMOS domino circuit by using VLV testing or raising the supply voltage to 40% higher than its nominal value.

C.2.1 Defect Coverage at Different Temperatures

CMOS domino gates dissipate more power than static CMOS gates because the signals in CMOS domino gates switch every cycle. Consequently, CMOS domino gates increase their operating temperature faster than static CMOS gates. Also, the noise margin of a CMOS domino gate strongly depends on the transistor threshold voltage. As the temperature increases, the transistor threshold voltage decreases [Sze 81]. As a result, the noise margin of a CMOS domino gate decreases as the operating temperature increases. Consequently, resistive shorts with large resistance, which cannot be detected at normal operating voltage and room temperature, may fail when the operating temperature increases due to power dissipation of CMOS domino gates.

Figure C-6 shows the simulated circuit. All four logic gates are implemented with CMOS domino circuits without keepers. A resistive short, shown as the thick line in Fig. C-6, exists between the output nodes of two 2-input domino AND gates. We assumed that the resistance of the short does not change with changing temperature. All input and output nodes are properly buffered. All domino gates are driven by a single clock signal. The simulation is based on the same 0.6 μm technology used in previous tests. All internal nodes were charged to the full-swing value during the precharge phase. In the evaluation phase, A, B, B1, and D1 were switched from 0 to 1. At the same time, C and D were held at 0. The resistive short was detected if OUTA and OUTC meet one of the following criteria:

A. OUTC changes from 0 to 1;

B. OUTA does not change from 0 to 1 or it changes ten times slower than expected.

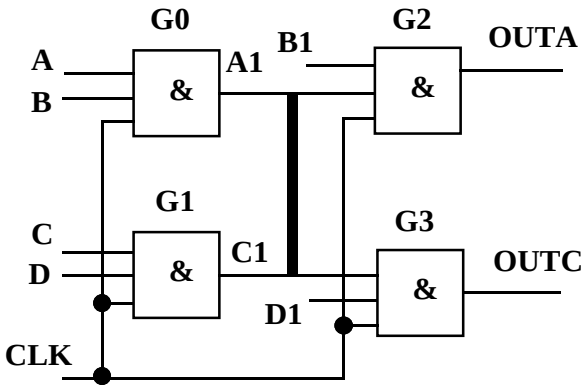

Figure C-6 Resistive Short

We performed the same simulation at four temperatures, 0^{O}C, 25^{O}C, 75^{O}C, and 125^{O}C. Figure C-7 shows the defect coverage of the resistive short shown in Fig. C-6 at different temperatures and at normal operating voltage 3.3V.

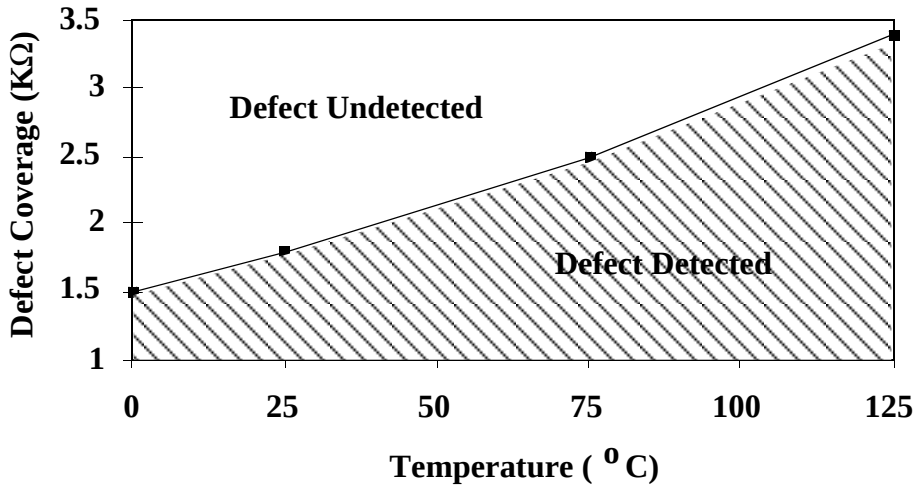

Figure C-7 Defect Coverage of the Short in Fig. C-6 at Different Temperatures for V_{dd} = 3.3V

Figure C-7 shows that the defect coverage of the resistive short increases as the temperature increases when the supply voltage is held constant. For the simulated circuit, a short with resistance greater than 1.5 KΩ cannot be detected at room temperature

(25°C). However, the defective CUT will fail at a higher operating temperature. Thus, the defective circuit can pass at room temperature but fail in the system when the operating temperature becomes higher than room temperature. This can make such a defective circuit fail intermittently or fail early in its lifetime. Therefore, resistive shorts in CMOS domino gates should be detected to ensure IC quality.

C.2.2 Defect Coverage at Different Voltages

We used the same circuit shown in Fig. C-6 to investigate the voltage dependence of the defect coverage of a resistive short. The operating temperature of the circuit was held at room temperature (25°C) during the simulation. We assumed that the test time is too short for the device to heat up during the tests at different voltages. Figure C-8 shows the simulation results.

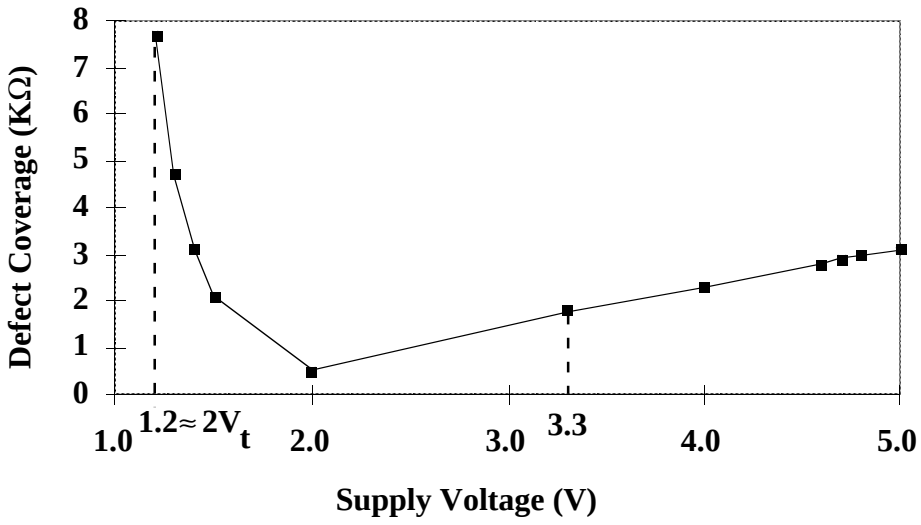

Figure C-8 Defect Coverage of the Short in Fig. C-6 at Different Voltages for Temperature = 25°C

Based on the results shown in Fig. C-8, we reached the following conclusions:

A. Above the normal operating voltage of 3.3V, the defect coverage of the resistive short improves as the voltage increases.

B. The defect coverage of the resistive short gets worse when the supply voltage is reduced from 3.3V and before it is close to 2V.

C. The defect coverage of the resistive short is best when the supply voltage is close to $2V_t$.

These observations are explained qualitatively below. At high voltage, the fault effect of the resistive short can be observed at OUTC in Fig. C-6. Noise can couple from A1 through the resistive short to C1. If the coupled noise at C1 becomes larger than the threshold voltage of an NMOS transistor, it can cause G3 to switch. Thus, OUTC can switch from 0 to 1 unexpectedly. The magnitude of the coupled noise can be approximated by Equation C-1. V_n is the magnitude of the coupled noise. R_S is the resistance of the resistive short. R_M is the equivalent resistance of the pull-down transistor (M4 in Fig. C-1) of G1. Since both inputs of G1 are zeros, R_M is almost a constant. V_{dd} is the supply voltage. Based on Equation C-1, the coupled noise is proportional to the supply voltage. Thus, the defect coverage improves when the supply voltage increases.

$$V_n = \frac{R_M}{R_s + R_M} \times V_{dd} \qquad \textbf{Equation C-1}$$

At very low voltage, the effect of the resistive short becomes severe because the equivalent resistance of a transistor increases significantly at very low voltage [Hao 93] [Chang 96a]. A1 is pulled down by the pull-down transistor (M4 in Fig. C-1) of G1 to be smaller than the threshold voltage of a transistor at very low voltage. Thus, G2 cannot switch or can only switch slowly. Consequently, we observe the fault effect at OUTA. Figure C-8 shows that the supply voltage should be as low as $2V_t$ to improve defect coverage significantly.

However, if the supply voltage is reduced from its normal operating value but not made as low as $2V_t$, the defect coverage becomes worse than it is at the normal operating voltage. When the supply voltage is in this range, the coupled noise at C1 is too small to turn on G3 and the weakened signal at A1 is still much larger than the threshold voltage of a transistor and thus cannot turn off G2.

C.2.3 Supply Voltage Selection

The supply voltage used for testing resistive shorts in CMOS domino logic should be selected so that we can detect all the defects that can cause a circuit to fail at high operating temperature and normal operating voltage. Also, a defect-free circuit should still be functional at the selected supply voltage.

Figure C-9 shows the defect coverage of the short shown in Fig. C-6 at different voltages and different temperatures. The gray region is the suggested supply voltage range for testing. The supply voltage should be either 40% higher than a normal operating voltage or about $2V_t$. The proposed supply voltage at very low voltage matches the one proposed in [Chang 96a].

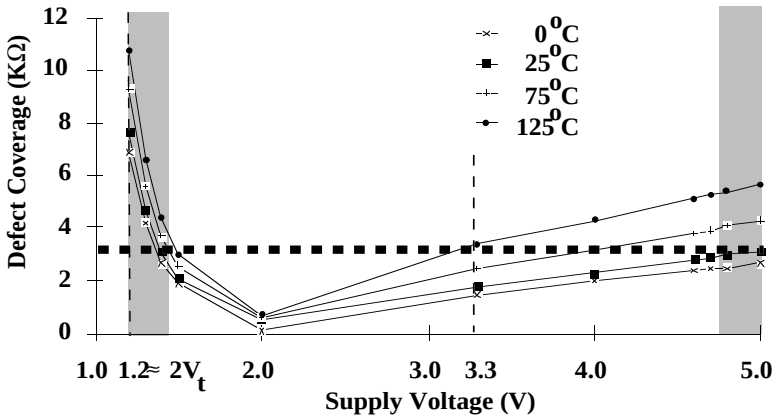

Figure C-9 Desired Supply Voltage Range (in the Gray Region)

We also did a similar study, in which we changed G2 and G3 to 4-input AND gates, and obtained similar results. Figure C-10 shows the voltage dependence of the defect coverage at different temperatures for the modified circuit. The gray region is the proposed supply voltage range. Even though the defect coverage is smaller than that for the short simulated in Fig. C-6 at the same supply voltage and temperature, the conclusion for the proposed supply voltage range remains the same.

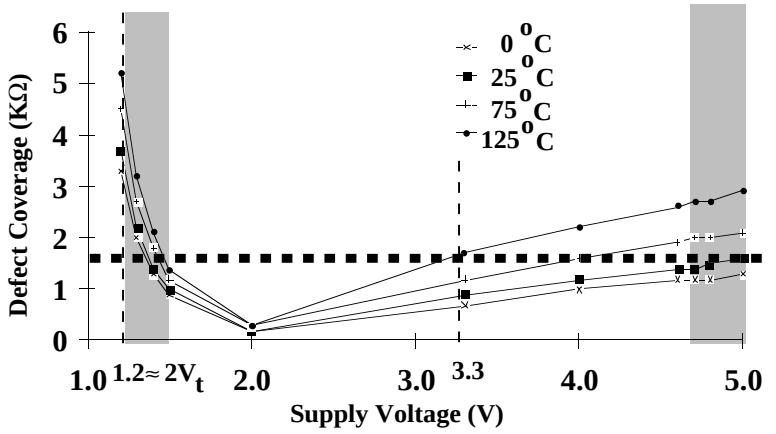

Figure C-10 Desired Supply Voltage Range (in the Gray Region) When G2 and G3 in Fig. C-6 are 4-Input AND Gates

Appendix D

SHOrt Voltage Elevation (SHOVE) Test for Weak CMOS ICs

Proceedings of VLSI Test Symposium, pp. 446-451, 1997

Appendix E

Experimental Results for IDDQ and VLV Testing

Proceedings of VLSI Test Symposium, pp.118-123, 1998