PRELIMINARY VERSION

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ANALYSIS OF FAIL-ALL-TEST-SET CUTs AND FAIL-SOME-TEST-SET CUTs IN AN EXPERIMENTAL TEST CHIP

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Abstract:

A test chip was designed and manufactured to evaluate the effectiveness of various test techniques. In this report, defective CUTs are classified into two groups: Fail-Some-Test-Set (FSTS) CUTs and Fail-All-Test-Set (FATS) CUTs. This study shows that, in general, FATS CUTs can be detected by fewer vectors. The "efficiency" of different test sets is also discussed in terms of how fast the defective CUTs can be detected. The result of this study in comparing test results at nominal voltage and at very low voltage (VLV) is also shown in this report. Classification of timing-dependent defects and sequence-dependent defects are examined using test results from a timing which is at least 30 times slower than nominal timing. Seven percent of CUTs have different test results in different clock speed.

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ABSTRACT

A test chip was designed and manufactured to evaluate the effectiveness of various test techniques. In this report, defective CUTs are classified into two groups: Fail-Some-Test-Set (FSTS) CUTs and Fail-All-Test-Set (FATS) CUTs. This study shows that, in general, FATS CUTs can be detected by fewer vectors. The "efficiency" of different test sets is also discussed in terms of how fast the defective CUTs can be detected. The result of this study in comparing test results at nominal voltage and at very low voltage (VLV) is also shown in this report. Classification of timing-dependent defects and sequence-dependent defects are examined using test results from a timing which is at least 30 times slower than nominal timing. Seven percent of CUTs have different test results in different clock speed.

1. INTRODUCTION

A test chip has been designed and manufactured. The chip is used in an experiment to evaluate the effectiveness of different test techniques. This report is part of a series that reported the results from the experiment. The chip and experiment design was described in ITC'95[1,2]. The preliminary results from wafer probe were also presented in ITC'95[3]. The results for different clock rate and clocking mode in wafer probe were presented in ITC'96[4]. In VTS'98[5],

the preliminary results of the final package test focusing on IDDQ and VLV were presented. In ITC'98[6], the results for sequence-dependent and timing-dependent failures were presented. In this report, new studies on the test chip experiment results will be presented.

Based on 119 CUTs that fail some test sets at final package test, the CUTs are divided into two groups: Fail-Some-Test-Set (FSTS) CUTs and Fail-All-Test-Set (FATS) CUTs. There are 72 out of 119 CUTs classified as FATS CUTs and 47 out of 119 CUTs classified as FSTS CUTs. The first failure counts of these two groups of CUTs are examined. The first failure count (from the test sets which do not have test escape for the particular CUT) in the wafer probe of FSTS CUTs are, in general, significantly larger than the first failure count of FATS CUTs. There are no significant relationship between FSTS/FATS classification and IDDQ test result. There are no significant correlation between FSTS/FATS classification and sequence-dependency. There are no significant correlation between FSTS/FATS classification and timing-dependency. The statistics of the position of the die in a wafer is similar for FATS and FSTS CUTs.

The first failure counts of different test sets for defective CUTs are examined to explore the "efficiency" of the test sets. A comparison for stuck-at fault test sets with different fault coverage shows that the number of defective CUTs detected by the same number of vectors are approximately the same. For test sets generated from different fault models, the result shows that stuck-at fault test sets can detect more defective CUTs than delay fault test sets when the number of test vectors are the same.

As for VLV test, a comparison of testing at nominal voltage and at very low voltage (VLV) shows that for some defective CUTs, testing at VLV can detect defective CUTs faster. For some defective CUTs, testing at nominal voltage can detect defective CUTs faster. While for some CUTs, both cases show up for different test sets.

Based on the test results from nominal timing and slow timing which is at least thirty times slower than nominal timing, we concluded that around thirty percent of the defective CUTs behave differently with different clock speed. Around seven percent of the defective CUTs have different test results for some test sets with different clock speed.

This report is organized as follows. Section 2 lists the 119 CUTs under discussion in this report. Section 3 defines the terminology used in this report. Section 4 shows the statistics for the first failure count of FATS CUTs and FSTS CUTs. Section 5 describes the correlation between FATS/FSTS classification and IDDQ test result, timing dependency, sequence dependency, die

location in a wafer. Section 6 discusses the "effectiveness" of different test sets. Section 7 presents the comparison of test results between VLV and normal test. Section 8 discusses defect classification. Section 9 concludes this report.

2. CUTs UNDER DISCUSSION

For the 122 dies that failed some Boolean tests at nominal supply voltage in the wafer probe, there are 113 dies that failed some Boolean tests at nominal voltage in the final package tests. Three of them have two CUTs failing some Boolean tests at nominal voltage[6]. There are three dies passed all Boolean tests in the wafer probe but failed some Boolean tests at nominal voltage in the final package test. The 119 CUTs under consideration in this report includes the 113 dies (totally 116 interesting CUTs on these 113 dies) that failed some Boolean tests in the wafer probe and the three dies (3 interesting CUTs on these 3 dies) that passed all Boolean tests in the wafer probe.

3. TERMINOLOGY

This section defines the terminology used in this report.

Definition: First failure count

The *first failure count* is the first vector that causes a CUT to fail for a test set.

Definition: Fail-All-Test-Set (FATS) CUT

A *Fail-All-Test-Set CUT* is a CUT which fails all Boolean tests applied to the CUT at nominal voltage, rated speed and pulse-width clocking mode [1][2] in the final package test.

Definition: Fail-Some-Test-Set (FSTS) CUT

A *Fail-Some-Test-Set CUT* is a CUT which fails at lease one Boolean tests applied to the CUT and passes at least one Boolean tests applied to the CUT at nominal voltage, rated speed and pulse-width clocking mode [1][2] in the final package test.

Definition: Efficiency (of a test set)

The *efficiency* of a test set is measured by the number of vectors needed to detect 75% of the defective CUTs.

Definition: VLV effective CUT

A *VLV effective CUT* is a CUT that at least one of the test sets applied to the CUT has a smaller first failure count at very low voltage (1.7V) than at nominal voltage in the final package test.

Definition: NV effective CUT

A *NV effective CUT* is a CUT that at least one of the test sets applied to the CUT has a smaller first failure count at nominal voltage than at very low voltage (1.7V) in the final package test.

Definition: NV&VLV effective CUT

A *NV&VLV effective CUT* is a CUT that is both VLV effective and NV effective.

Definition: VLV effective only CUT

A *VLV effective only CUT* is a CUT that is VLV effective but is not NV effective.

Definition: NV effective only CUT

A *NV effective only CUT* is a CUT that is NV effective but is not VLV effective.

Definition: TIC defect

A *TIC defect* is a defect whose behavior depends on only the input vector applied, not the previous vectors and does not depend on the clock speed.

Definition: Sequence-Dependent Defects

A *sequence-dependent defect* is a defect whose behavior depend on not only the vector applied , but also the previous vectors.

Definition: Timing-Dependent Defects

A *timing-dependent defect* is a defect whose behavior depend on clock speed

4. FSTS/FATS AND FIRST FAILURE COUNT IN WAFER PROBE

In this section, we discuss only the 116 CUTs that fail some Boolean tests in wafer probe. Table 1 to table 4 shows the distribution of the first failure counts in wafer probe for MUL FATS CUTs, MUL FSTS CUTs, ROB FATS CUTs and ROB FSTS CUTs. The statistics come from data for tests at nominal voltage, rated speed and pulse-width clocking mode [1][2]. The number of LSI gates for each CUT was reported in [1], we list it in table 5 for reference. The lengths of test sets were also reported in [1][2], they are listed in table 6 here.

Table 1: Distribution of First Failure Counts in Wafer Probe – MUL FATS CUTs

		First Failure Count						
	Test Set	1-20	21-40	41-100	101-300	301-1000	1000+	escape
1.1	Design Verification	20	1	0	0	0	0	1
2.1	SSF tool 1 (100% gate faults)	20	2	0	0	0	0	0
2.2	SSF tool 2 (100% gate faults)	21	0	0	1	0	0	0
2.3	SSF tool 2 (100%, pin faults)	21	0	1	0	0	0	0
2.4	SSF tool 3 (100%, pin faults)	22	0	0	0	0	0	0
2.6	SSF tool 4 (100% gate faults)	22	0	0	0	0	0	0
2.7	SSF Tool 4 (99.0%)	22	0	0	0	0	0	0
2.8	SSF Tool 4 (98.0%)	21	1	0	0	0	0	0
2.9	SSF Tool 4 (95.0%)	20	1	0	0	0	0	1
2.10	SSF Tool 4 (90.0%)	21	0	0	0	0	0	1
2.11	SSF Tool 4 (80.0%)	20	1	0	0	0	0	1
2.12	SSF Tool 4 - Min 5 Det/Fault	21	1	0	0	0	0	0
2.13	SSF Tool 4 - Min 15 Det/Fault	22	0	0	0	0	0	0
3.1	Switch-level ATPG	17	5	0	0	0	0	0
4.1	Pseudo-Random/Exhaustive	18	3	0	0	0	1	0
5.1	Weightrd Random - (WR-MUR)	18	3	0	0	0	1	0
5.2	Weightrd Random - (WR-MUR)	19	2	0	0	0	1	0
6.1	Stuck-Open ATPG	20	2	0	0	0	0	0
7.1	Transition Fault, ATPG Tool 5	16	5	1	0	0	0	0
7.2	Transition Fault, ATPG Tool 6	19	2	1	0	0	0	0
9.1	Gate Delay Fault - X-> 0	18	0	1	2	0	0	1
9.2	Gate Delay Fault - X-> ran	18	0	1	2	0	0	1

Table 2: Distribution of First Failure Counts in Wafer Probe – MUL FSTS CUTs

	Test Set	First Failure Count						
		1-20	21-40	41-100	101-300	301-1000	1000+	escape
1.1	Design Verification	6	3	0	0	0	0	5
2.1	SSF tool 1 (100% gate faults)	7	2	2	0	0	0	3
2.2	SSF tool 2 (100% gate faults)	6	1	2	3	0	0	2
2.3	SSF tool 2 (100%, pin faults)	7	2	3	0	0	0	2
2.4	SSF tool 3 (100%, pin faults)	9	1	0	0	0	0	4
2.6	SSF tool 4 (100% gate faults)	12	0	2	0	0	0	0
2.7	SSF Tool 4 (99.0%)	8	2	3	0	0	0	1
2.8	SSF Tool 4 (98.0%)	10	1	1	0	0	0	2
2.9	SSF Tool 4 (95.0%)	9	1	1	0	0	0	3
2.1	SSF Tool 4 (90.0%)	5	2	0	0	0	0	7
2.11	SSF Tool 4 (80.0%)	6	0	0	0	0	0	8
2.12	SSF Tool 4 - Min 5 Det/Fault	8	2	4	0	0	0	0
2.13	SSF Tool 4 - Min 15 Det/Fault	10	0	4	0	0	0	0
3.1	Switch-level ATPG	6	6	2	0	0	0	0
4.1	Pseudo-Random/Exhaustive	1	3	3	0	4	3	0
5.1	Weightrd Random - (WR-MUR)	1	3	3	0	4	3	0
5.2	Weightrd Random - (WR-MUR)	4	3	2	1	1	3	0
6.1	Stuck-Open ATPG	10	3	0	0	0	0	1
7.1	Transition Fault, ATPG Tool 5	7	3	2	0	0	0	2
7.2	Transition Fault, ATPG Tool 6	9	3	1	1	0	0	0
9.1	Gate Delay Fault - X-> 0	6	0	1	1	2	0	4
9.2	Gate Delay Fault - X-> ran	6	0	1	1	2	0	4

Table 3: Distribution of First Failure Counts in Wafer Probe – ROB FATS CUTs

	Test Set	First Failure Count						
		1-20	21-40	41-100	101-300	301-1000	1000+	escape
2.1	SSF tool 1 (100% gate faults)	12	0	1	0	0	0	0
2.2	SSF tool 2 (100% gate faults)	13	0	0	0	0	0	0
2.3	SSF tool 2 (100%, pin faults)	13	0	0	0	0	0	0
2.4	SSF tool 3 (100%, pin faults)	11	1	0	1	0	0	0
2.5	SSF tool 3 (100%, compressed)	11	2	0	0	0	0	0
2.6	SSF tool 4 (100% gate faults)	11	1	1	0	0	0	0
2.7	SSF Tool 4 (99.0%)	11	2	0	0	0	0	0
2.8	SSF Tool 4 (98.0%)	10	3	0	0	0	0	0
2.9	SSF Tool 4 (95.0%)	11	1	1	0	0	0	0
2.10	SSF Tool 4 (90.0%)	12	1	0	0	0	0	0
2.11	SSF Tool 4 (80.0%)	12	0	1	0	0	0	0
2.12	SSF Tool 4 - Min 5 Det/Fault	10	2	1	0	0	0	0
2.13	SSF Tool 4 - Min 15 Det/Fault	9	1	3	0	0	0	0
3.1	Switch-level ATPG	11	2	0	0	0	0	0
4.1	Pseudo-Random/Exhaustive	8	5	0	0	0	0	0
5.1	Weightrd Random - (WR-MUR)	8	5	0	0	0	0	0
5.2	Weightrd Random - (WR-MUR)	12	0	1	0	0	0	0
6.1	Stuck-Open ATPG	12	0	1	0	0	0	0
7.1	Transition Fault, ATPG Tool 5	11	0	1	1	0	0	0
7.2	Transition Fault, ATPG Tool 6	9	3	1	0	0	0	0
8.1	Gate Delay Fault - X-> 0	8	1	3	1	0	0	0
8.2	Gate Delay Fault - X-> ran	9	3	1	0	0	0	0
9.1	Path Delay - Crit. Path - X->0	4	1	3	2	3	0	0
9.2	Path Delay - Crit. Path - X->ran	4	1	3	3	2	0	0
9.3	Path Delay - Robust - X->0	6	3	3	0	0	1	0
9.4	Path Delay - Robust - X->ran	6	4	3	0	0	0	0
9.5	Path Delay - Robust Test	6	1	3	2	1	0	0
9.6	Path Delay - Non-Robust - A	12	1	0	0	0	0	0
9.7	Path Delay - Non-Robust - B	12	0	1	0	0	0	0

Table 4: Distribution of First Failure Counts in Wafer Probe – ROB FSTS CUTs

	Test Set	First Failure Count						
		1-20	21-40	41-100	101-300	301-1000	1000+	escape
2.1	SSF tool 1 (100% gate faults)	6	1	3	5	0	0	3
2.2	SSF tool 2 (100% gate faults)	5	1	5	3	3	0	1
2.3	SSF tool 2 (100%, pin faults)	5	1	5	3	3	0	1
2.4	SSF tool 3 (100%, pin faults)	7	1	6	3	0	0	1
2.5	SSF tool 3 (100%, compressed)	8	1	4	3	0	0	2
2.6	SSF tool 4 (100% gate faults)	6	3	0	5	0	0	4
2.7	SSF Tool 4 (99.0%)	4	4	2	6	0	0	2
2.8	SSF Tool 4 (98.0%)	8	2	3	2	0	0	3
2.9	SSF Tool 4 (95.0%)	5	1	3	6	0	0	3
2.10	SSF Tool 4 (90.0%)	6	7	2	0	0	0	3
2.11	SSF Tool 4 (80.0%)	5	0	4	3	0	0	6
2.12	SSF Tool 4 - Min 5 Det/Fault	4	2	3	6	1	1	1
2.13	SSF Tool 4 - Min 15 Det/Fault	8	0	2	6	1	1	0
3.1	Switch-level ATPG	2	4	4	2	0	1	5
4.1	Pseudo-Random/Exhaustive	3	1	5	5	2	2	0
5.1	Weightrd Random - (WR-MUR)	3	1	5	4	3	1	1
5.2	Weightrd Random - (WR-MUR)	5	1	4	3	1	4	0
6.1	Stuck-Open ATPG	4	3	4	3	3	0	1
7.1	Transition Fault, ATPG Tool 5	6	1	1	6	2	0	2
7.2	Transition Fault, ATPG Tool 6	3	2	2	3	3	0	5
8.1	Gate Delay Fault - X-> 0	4	1	4	1	1	0	7
8.2	Gate Delay Fault - X-> ran	3	1	6	3	0	0	5
9.1	Path Delay - Crit. Path - X->0	1	0	0	1	0	0	16
9.2	Path Delay - Crit. Path - X->ran	1	0	1	4	1	1	10
9.3	Path Delay - Robust - X->0	1	0	2	3	2	9	1
9.4	Path Delay - Robust - X->ran	4	1	0	4	1	6	2
9.5	Path Delay - Robust Test	3	2	0	3	1	7	2
9.6	Path Delay - Non-Robust - A	5	2	4	4	0	0	3
9.7	Path Delay - Non-Robust - B	7	0	5	2	1	2	1

Table 5: LSI gate counts for different CUTs

CUT	Number of LSI Gates
MUL	1146
SQR	446
STD	298
SIM	380
ROB	898

Table 6: Test lengths for different test sets

	Test Set	Test Length				
		SQR	MUL	STD	SIM	ROB
1.1	Design Verification	90	57			
2.1	SSF tool 1 (100% gate faults)	34	62	68	79	244
2.2	SSF tool 2 (100% gate faults)	74	163	129	144	490
2.3	SSF tool 2 (100%, pin faults)	34	61	129	144	489
2.4	SSF tool 3 (100%, pin faults)	22	21	69	82	262
2.5	SSF tool 3 (100%, compressed)			62	66	234
2.6	SSF tool 4 (100% gate faults)	39	68	72	93	275
2.7	SSF Tool 4 (99.0%)	38	78	71	91	254
2.8	SSF Tool 4 (98.0%)	39	69	80	87	245
2.9	SSF Tool 4 (95.0%)	39	62	73	74	219
2.10	SSF Tool 4 (90.0%)	35	63	67	72	190
2.11	SSF Tool 4 (80.0%)	20	49	48	58	159
2.12	SSF Tool 4 - Min 5 Det/Fault	168	258	339	397	1235
2.13	SSF Tool 4 - Min 15 Det/Fault	473	754	1046	1163	3745
3.1	Switch-level ATPG	56	110	108	109	327
4.1	Pseudo-Random/Exhaustive	4096	2^24	2^24	2^24	2^24
5.1	Weightrd Random - (WR-MUR)	417	23332	3404	1438	34330
5.2	Weightrd Random - (WR-MUR)	372	12341	634	738	7807
6.1	Stuck-Open ATPG	153	269	203	219	766
7.1	Transition Fault, ATPG Tool 5	68	84	222	256	796
7.2	Transition Fault, ATPG Tool 6	304	434	274	292	586
8.1	Gate Delay Fault - X-> 0	976		312	304	612
8.2	Gate Delay Fault - X-> ran	976		312	304	612
9.1	Path Delay - Crit. Path - X->0	1692	620	992	408	400
9.2	Path Delay - Crit. Path - X->ran	1692	620	992	408	400
9.3	Path Delay - Robust - X->0			2864	2864	7068
9.4	Path Delay - Robust - X->ran			2864	2864	7068
9.5	Path Delay - Robust Test			3044	3044	7092
9.6	Path Delay - Non-Robust - A			562	542	884
9.7	Path Delay - Non-Robust - B			2164	2156	4136

Based on table 1 to table 4, we made the following observation:

· There are significant correlation between FSTS/FATS classification and the first failure counts obtained in the wafer probe. The first failure count is, in general, smaller for FATS CUTs. The result shows that most of the FATS CUTs can be detected in the first 40 vectors for most of the test sets. For FSTS CUTs, longer length of vectors is needed to detect a defective CUT.

- For some delay test sets, we had two copies of them. We replaced “X’s” by “0s” in one copy and randomly replaced “X’s” by “0s” and “1s” in the other. (Test sets 8.1 and 8.2, 9.1 and 9.2, 9.3 and 9.4). The results from the two copies (9.1 and 9.2) for MUL CUTs are the same. For ROB CUTs, replacing “X’s” randomly by “0s” and “1s” detects defective CUTs faster, especially for FSTS CUTs. For SIM and STD CUTs, results similar to ROB CUTs were found. There are more transition activities in the copy with “X’s” randomly replaced by “0s” and “1s”. Thus more coupling can occur and the delay of target paths can be affected. This could be the reason why replacing “X’s” randomly by “0s” and “1s” detects defective CUTs faster.
- Detecting defective MUL CUTs require smaller number of vectors than ROB CUTs. This is consistent with the longer test lengths for ROB CUTs

5. FSTS/FATS AND IDDQ, TIMING-DEPENDENT, SEQUENCE-DEPENDENT, DIE LOCATION IN A WAFER

5.1 FSTS/FATS and IDDQ

Table 7 lists the IDDQ results in the final package test for FSTS CUTs and FATS CUTs.

Table 7: Maximum IDDQ measured for FATS/FSTS CUTs

		Number of CUTs whose maximum IDDQ is																	
	Total	<3uA		3-10 uA		10-50 uA		50-100 uA		100-500 uA		500-1000 uA		1000-5000 uA		5000-10000 uA		> 10000 uA	
FATS CUTs	72	9	13%	0	0%	4	6%	2	3%	4	6%	2	3%	22	31%	18	25%	11	15%
FSTS CUTs	47	8	17%	2	4%	3	6%	1	2%	3	6%	4	9%	18	38%	2	4%	6	13%

The maximum IDDQ is obtained from six IDDQ test sets. There are 9 (13%) FATS CUTs and 8 (17%) FSTS CUTs passing IDDQ test (for single threshold=3μA). The correlation of the IDDQ test result and the FSTS/FATS classification is not significant. However, there are 29 (40%) FATS CUTs whose maximum measured IDDQ value exceed 5mA. Only 8 (17%) FSTS CUTs whose maximum measured IDDQ value exceed 5mA.

5.2 FSTS/FATS and sequence-dependent(SD), timing-dependent(TD)

There are no significant correlation between FSTS/FATS classification and SD/TD/TIC classification. The distribution is shown in Table 8.

Table 8: FATS/FSTS and SD/TD

	Number of CUTs											
	Total	SD&TD		SD only		TD only		SD		TD		TIC	
FATS CUTs	72	16	22%	5	7%	7	10%	21	29%	23	32%	44	61%
FSTS CUTs	47	9	19%	6	13%	8	17%	15	32%	17	36%	24	51%

5.3 FSTS/FATS and the location of the die in a wafer

The die location for both groups of CUTs are very similar to the one presented in [6]. The results are listed in Table 9. The definitions of each class of location are the same as in [6].

Table 9: FATS/FSTS and die location

	Number of dies										
	Total	Near gross failure		Near wafer periphery		Near eith gross failure or wafer periphery		Near wafer center		Others	
FATS CUTs*	67	61	91%	21	31%	64	96%	11	16%	3	4%
FSTS CUTs**	45	37	82%	4	9%	38	84%	6	13%	6	13%

*67 = 72(total) - 3(passed in wafer sort) - 2(FATS CUT and FSTS CUT on the same die)
**45 = 47(total) - 2(FATS CUT and FSTS CUT on the same die)

Based on table 9, we made the following observation:

- Most of the defective dies are located near gross failure or near wafer periphery for both groups of dies.
- Compared with dies with FATS CUTs, less percentage of dies with FSTS CUTs are located near either gross failure or wafer periphery.

6. EFFICIENCY OF DIFFERENT TEST SETS

Since we have larger number of defective MUL and ROB CUTs, data of these two types of CUTs are discussed. Figure 1 and 2 shows number of vectors applied versus number of defective CUTs detected for the first 100 vectors. Figure 1 is for MUL CUTs. Figure 2 is for ROB CUTs. Stuck-at fault test sets with different fault coverage are shown.

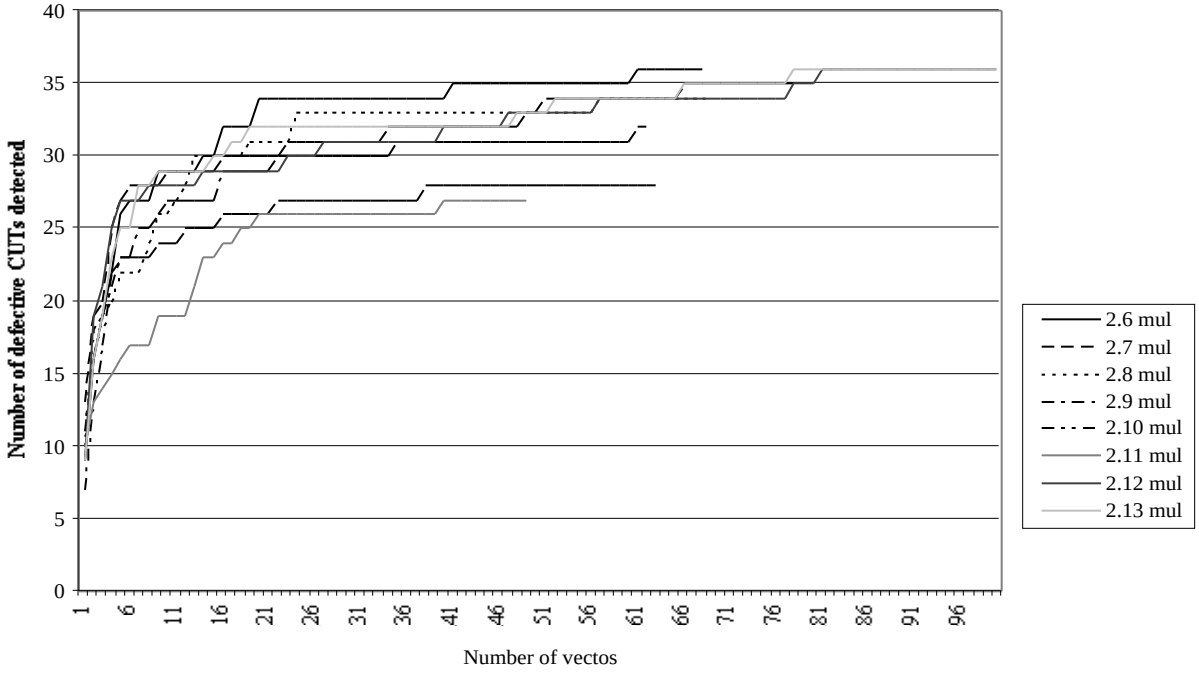

Figure 1: Efficiency of Test Sets – SSF Test Sets, MUL CUTs

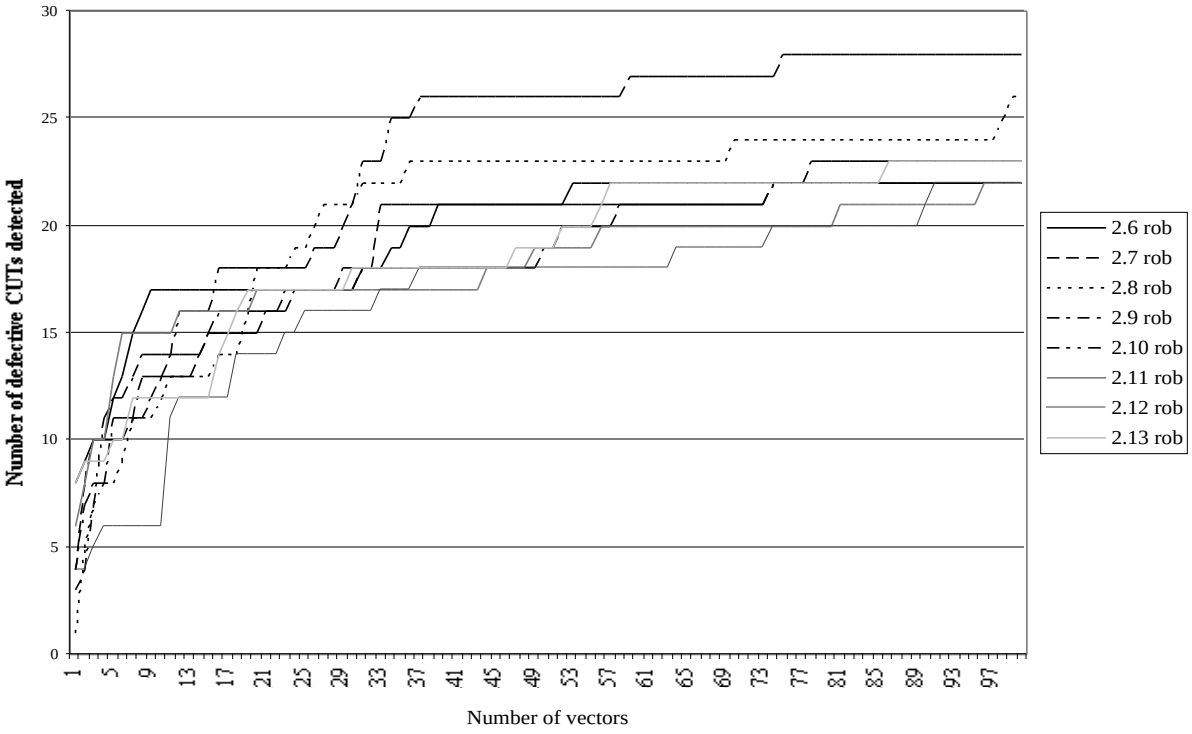

Figure 2: Efficiency of Test Sets – SSF Test Sets, ROB CUTs

From the figures 1 and figure 2, we made the following observation:

- The efficiency of stuck-at test sets with different fault coverage in terms of number of vectors needed to detect a defective CUTs varies with type of CUT in this experiment. However, the efficiency has no significant difference among different test sets. For SQR, SIM and STD CUTs, the efficiency of different test sets are even closer than ROB and MUL.

Figure 3 and 4 also show number of vectors applied versus number of defective CUTs detected for the first 100 vectors. Test sets generated from different fault models are shown.

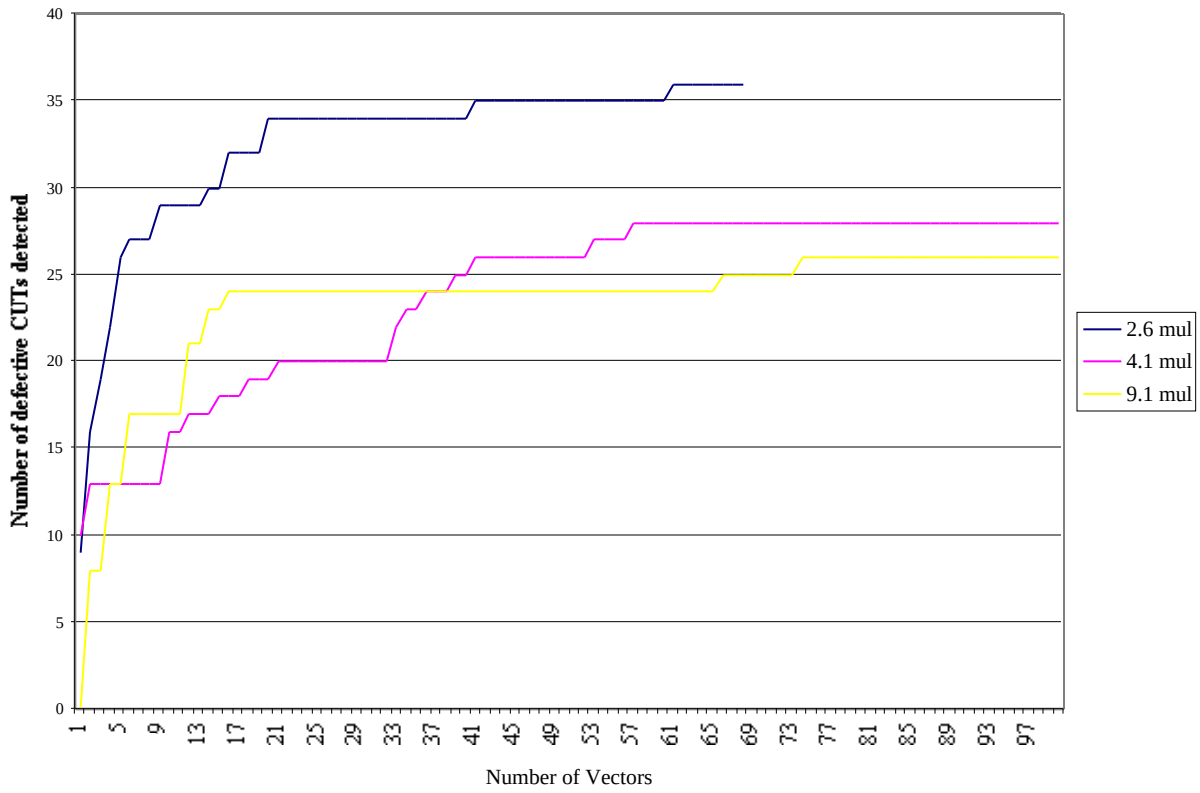

Figure 3: Efficiency of Test Sets – Test Sets from Different Fault Models, MUL CUTs

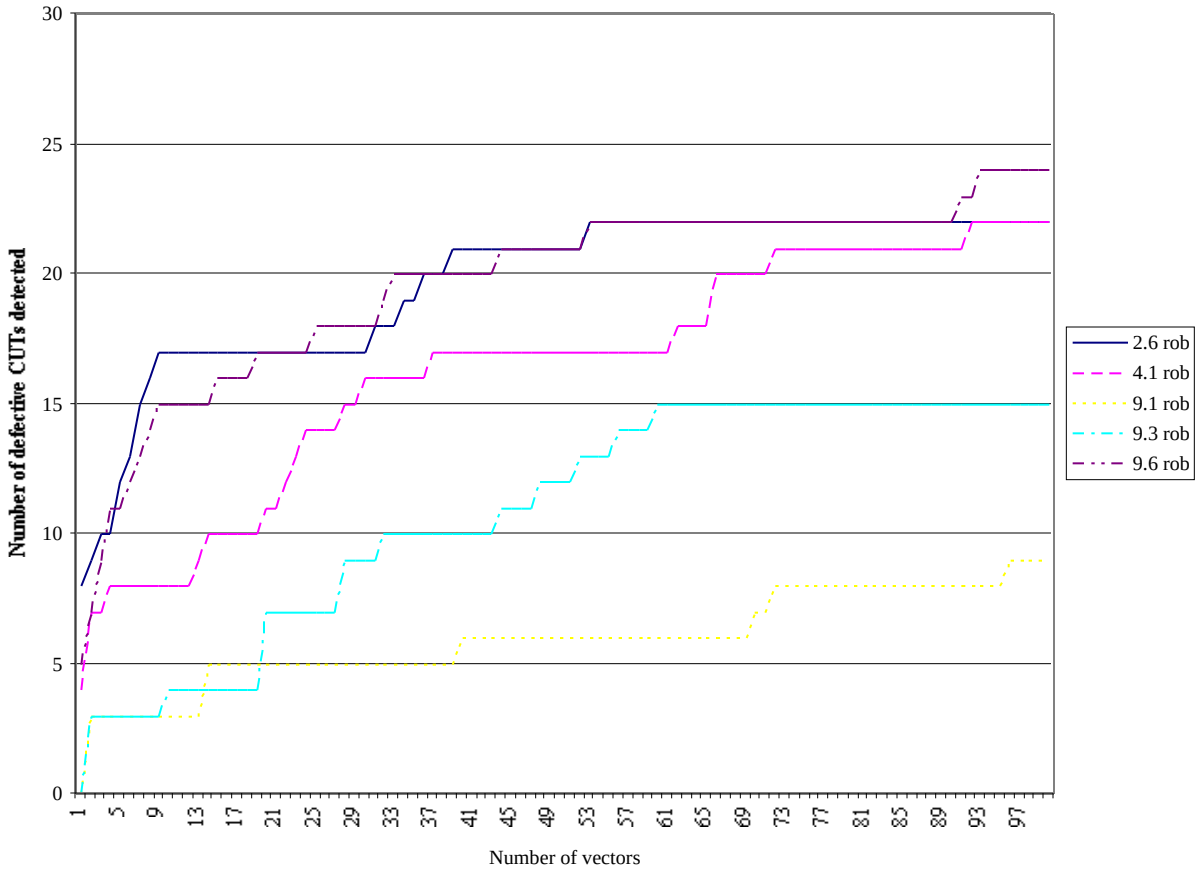

Figure 4: Efficiency of Test Sets – Test Sets from Different Fault Models, ROB CUTs

From figure 3 and figure 4, we found that

- Stuck-at fault test set (2.6) is more efficient than other test sets.
- Non-robust delay test set (9.6) is also very effective for ROB CUTs. However, the result for SIM and STD CUTs (not shown here) shows that the efficiency for non-robust delay test sets is approximately the same as pseudo-random test set (4.1) and they are both less efficient than single stuck-at test set (2.6). Since there are two vectors in a pattern for delay tests, this can be the reason why delay test is less efficient.
- Robust delay test set (9.3) is less efficient than single stuck-at test set (2.6) and pseudo-random test set (4.1).
- Critical path delay test set (9.1) is the least efficient among all the test sets. This shows that a large number of defects are not on critical paths.

7. COMPARISON OF THE TEST RESULTS AT VLV AND AT NOMINAL VOLTAGE

A study of first failure count at VLV (1.7V) and at nominal voltage for 119 CUTs shows that there are 28(24%) NV&VLV effective CUTs . There are 7(6%) NV effective only CUTs and 14(12%) VLV effective only CUTs. The result is summarized in table 10.

Table 10: Summary of NV Effective and VLV Effective CUTs

Number of CUTs								
total	NV&VLV effective		NV effective only		VLV effective only		others	
119	28	24%	7	6%	14	12%	70	59%

The result shows that

- For most of the CUTs (around 60%), test results at nominal voltage and at VLV are the same.
- Some defective CUTs are easier to be detected at nominal voltage. Some defective CUTs are easier to be detected at VLV. For nearly 1/4 of all CUTs, the first failure counts at nominal voltage are smaller than at VLV for some test sets but the first failure counts at VLV are smaller than at nominal voltage for some other test sets.

8. DEFECT CLASSIFICATION

In order to do the study of defect classification, we tested the CUTs in both nominal voltage and slow timing which is at least thirty times slower than the nominal voltage. We also modify the original 15 test sets in five different ways:

- Insert an all-one vector in front of each vector.
- Insert an all-zero vector in front of each vector.
- Insert a bit-wise complemented vector in front of each vector.
- Reverse the vector sequence in the original test set.
- Insert a shifted vector in front of each vector.

Based on the 119 CUTs that failed some sampling tests at nominal voltage, we classified 68 CUTs as having TIC (Timing Independent Combinational) defects. For these 68 CUTs, the values in the failure counters were compared to a diagnostic dictionary for stuck-at faults. This analysis shows that 41 CUTs behave like single-stuck at faults. If a defective CUT is not classified as having TIC defects, it is classified as having *non-TIC* defects. There were 51 CUTs classified as having non-TIC defects. Among the 51 non-TIC CUTs, 36 CUTs were identified having sequence-dependent failures and 40 CUTs having timing-dependent failures. Figure 5 gives a summary for the classification.

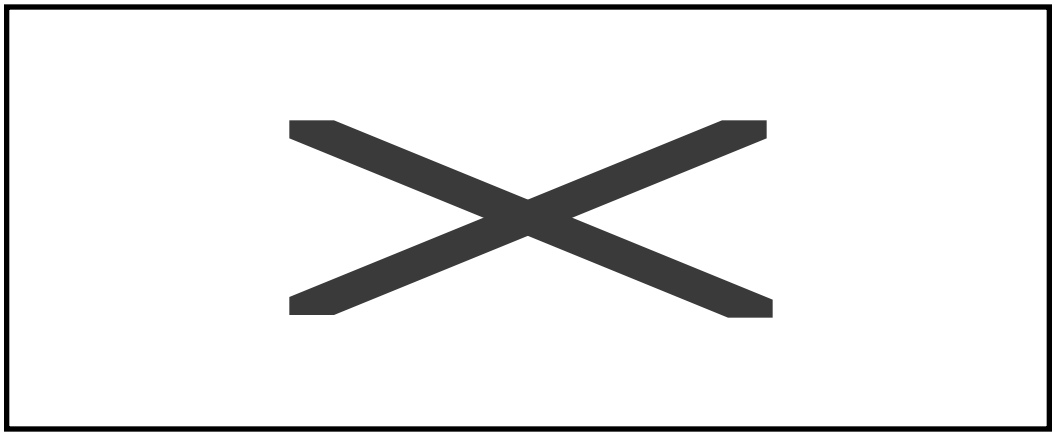

Figure 5: Defect Classification

Among the 40 CUTs whose behavior are timing-dependent, there are seven CUTs which escape more test sets at slow timing (thirty times slower than the nominal timing) than at nominal timing. There is one CUT which escapes more test sets at nominal timing than at slow timing. Around seven percent (8 out of 119) of the defective CUTs have different test result for some test sets at different clock speed.

9. CONCLUSION

Based on the test results from an test chip experiment, a study of FATS/FSTS CUTs, the efficiency of different test sets and a comparison for test results at VLV and at nominal voltage are presented in this report.

From the studies shown in this report, we concludes that the first failure counts for FATS CUTs are, in general, smaller than the first failure counts for FSTS CUTs. From the data of this experiment, we didn't find significant correlation between FATS/FSTS classification and IDDQ test result, timing-dependent, pattern-dependent or the location of a die on the wafer.

We also presented the result for the efficiency of different test sets in terms of how many vectors needed to detect defective CUTs. No significant differences in efficiency for stuck-at fault test sets with different test coverage were found. However, stuck-at test sets are more efficient than delay fault test sets.

We also showed that for about 40% of the CUTs, the results are not the same for VLV test and test at nominal voltage. For nearly 1/4 of all CUTs, the first failure counts at nominal voltage are smaller than at VLV for some test sets but the first failure counts at VLV are smaller than at nominal voltage for some other test sets.

Around one third of the defective CUTs whose failure counts match failure counts from single stuck-at fault simulation. Around one third of the defective CUTs have sequence-dependent failures. Around one third of the defective CUTs have timing-dependent failures, among which seven percent of all defective CUTs whose test result depends on clock speed for some test sets.

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