

An Overview of the Stanford TOPS (Totally-Optimized Synthesis) Tool

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Introduction

TOPS (totally-optimized synthesis) is a synthesis-for-test tool which takes as input a functional-level VHDL design specification and automatically generates a dependable, gate-level VHDL implementation of the design.

The main goals of the TOPS project are to:

- Address dependability issues at the highest possible level of design.
- Minimize design specification and implementation mistakes.
- Reduce the design cycle time.
- Automatically generate the best design that meets all given requirements.

The synthesis-for-test algorithms implemented in TOPS automatically generate designs that are more dependable and have lower hardware overhead than designs that are first synthesized for area and performance and then modified to be more dependable. TOPS accomplishes this by simultaneously synthesizing both the test and functional logic.

In this presentation we will provide an overview of the operation of TOPS. In particular, we will discuss in detail the features of TOPS that distinguish it from other high-level synthesis tools:

- support of input design descriptions specified in functional-level VHDL.
- internal data structure features that allow for synthesis of realistic design examples.
- multiple synthesis-for-test algorithms.

TOPS Overview

The operation of TOPS is illustrated in Fig. 1. The Vantage (Viewlogic) VHDL compiler is used to generate VHDL Intermediate Format (VIF) descriptions of both the input functional description of the design and a component library. TOPS then synthesizes structural VHDL descriptions of both data path and control logic, making use of the components defined in

the component library. TOPS currently performs high-level synthesis operations such as scheduling, allocation, binding, and control logic generation, as well as compiler optimization operations such as dead code elimination and constant propagation. A modified version of the Berkeley SIS tool is used to perform state assignment and logic optimization on the control logic.

We have implemented several synthesis-for-test algorithms in the TOPS high-level synthesis and logic optimization operations. These algorithms automatically generate logic that is optimized for the given dependability requirements. The synthesis-for-test algorithms currently implemented in TOPS include:

- Register binding for parallel BIST
- Synthesis for scan dependence
- Synthesis of random-pattern-testable logic
- Synthesis of concurrent error detectors

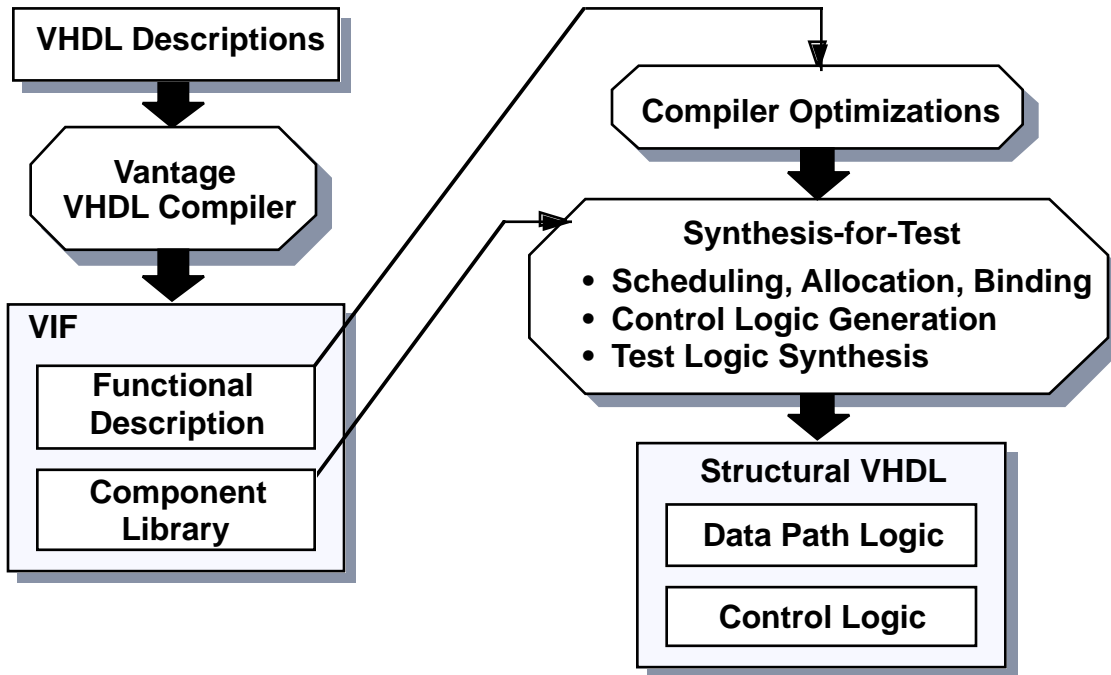


Figure 1: TOPS operation.

In addition to developing synthesis-for-test techniques, we are developing a functional-level specification methodology, within the context of VHDL, to be used for the designs that are input to TOPS. Functional-level specifications allow TOPS to increase the design search space and generate implementations that have greater sharing of design and test logic. TOPS currently supports synthesis of designs specified with the data types and functions defined in the VHDL Synthesis Packages that were developed by the VHDL Synthesis working group (IEEE 1076.3).