SHOrt Voltage Elevation (SHOVE) Test

Jonathan T.-Y. Chang and Edward J. McCluskey
Center for Reliable Computing
Stanford University
Gates Hall 2A
Stanford, CA 94305

Abstract

A stress procedure for reliability screening, SHOrt Voltage Elevation (SHOVE) test, is analyzed here. During SHOVE, test vectors are run at higher-than-normal supply voltage for a short period. The IDDQ values of circuits-under-test are then measured at the normal voltage. This procedure is effective in screening oxide thinning, which occurs when the oxide thickness of a transistor is less than expected. Oxide thinning can cause early-life failures. The stress voltage of SHOVE testing should be set such that the electrical field across an oxide is approximately 6MV/cm. The stress time can be calculated by using "effective oxide thinning" model. We will also discuss the requirement of an input vector for stressing a complementary CMOS logic gate efficiently.

1. Introduction

SHOVE testing aims at screening early-life failures and improving the quality level of CMOS ICs. In conjunction with other testing techniques, such as IDDQ testing [Levi 81] and Very-Low-Voltage (VLV) Testing [Hao 93] [Chang 96], we can ensure CMOS ICs' quality without performing burn-in. Although burn-in can provoke various defects and improve the reliability of CMOS ICs [Hnatek 95], it increases the production cost and lengthens the test time. IDDQ testing can detect weak parts, which are ICs with low mean-time-to-failure (MTTF) [McCluskey 91], by measuring their quiescent currents. On the other hand, VLV testing can make weak parts fail functional tests at very low voltage. Both IDDQ testing and VLV testing do not change the characteristics of a circuit-under-test (CUT). Unlike IDDQ testing and VLV testing, SHOVE testing detects weak parts by changing their intrinsic characteristics.

During SHOVE, test sets, such as single stuck-at or pseudo stuck-at test sets, are run at higher-than-normal supply voltage for a short period. The IDDQ values of the CUTs are then measured at the normal operating voltage. It has been found that IDDQ values of some CUTs increase significantly after SHOVE [Duey 93] [Josephson 95]. SHOVE testing is useful at wafer sort. It can screen out weak parts during a wafer-level test and remove the cost of packaging them. This procedure has been widely practiced in industry [Kowalczyk 90] [Duey 93] [Josephson 95]. However, no detailed analysis has been found in any published literature. This paper will provide a theoretical study of SHOVE testing.

Oxide defects are one of the major causes for the reliability problems for CMOS ICs [Hnatek 95]. Particulate contamination, crystalline defects in the substrate, spot defects, localized thin regions, or surface roughness can cause localized weak spots in an oxide [Syrzycki 87] [Lee 88]. Moreover, the quality and lifetime of a gate oxide strongly depend on its thickness [Lee 88]. *Oxide thinning* occurs when the oxide thickness of a transistor is physically or effectively thinner than expected. Oxide thinning can be due to localized thin spots, traps in the oxide, surface asperity, or locally reduced tunneling barrier height [Schuegraf 94]. It can shorten the lifetime of a gate oxide, increase oxide leakage current, or cause time-dependent dielectric breakdown. As a result, it can cause early-life failures and must be detected. We investigated the device behavior during and after SHOVE. It is found that oxide thinning can cause stress-induced oxide leakage or become a gate oxide short after SHOVE and thus increase the IDDQ values of the defective CUT.

To stress defective oxides effectively and still avoid damaging flawless oxides, the electrical field across the oxides, E_{ox}, must be carefully controlled. Fowler-Nordheim tunneling currents may occur across flawless oxides if E_{ox} is larger than a critical value. The excess tunneling currents flowing through gate oxides can damage the oxides. The damage can cause increased oxide leakage currents even after the supply voltage is reduced to the normal operating voltage. Based on various published measurement data, the critical E_{ox} to avoid the Fowler-Nordheim tunneling current is approximately 6MV/cm [Moazzami 92] [Dumin 93] [Dumin 94] [Watanabe 94] [Depas 96]. E_{ox} at the normal operating voltage for different technologies is always well below this critical value [Schutz 94] [Charnas 95] [Sanchez 96] [Montanaro 96]. By applying the critical E_{ox} across the flawless oxide during SHOVE, we can maximize the stress effects on the defective oxides and also minimize the stress time.

In a CMOS IC, each transistor must be stressed for enough time during SHOVE. To effectively stress an NMOS transistor, the gate of the transistor should be held at the stress voltage and the drain and source of the transistor at 0V. Similarly, to effectively stress a PMOS transistor, the gate of the transistor should be held at 0V and the drain and source of the transistor at the stress voltage. Both single stuck-at and pseudo stuck-at test sets can be the stress vectors for SHOVE testing for fully complementary static CMOS logic. We also investigated the toggle probability of various test sets in a CUT. For pseudo stuck-at test sets, some nodes were in logical one or zero for one or two vectors only. Thus, each vector must be held for at least the stress time for a transistor to make sure all transistors in a CMOS IC are stressed for enough time. The stress speed should be the reciprocal of the stress time for a transistor in this case. The stress time of a transistor is the time to effectively stress an oxide.

This paper is organized as follows. Section 2 examines the behavior of oxide thinning during and after SHOVE. Section 3 discusses the stress voltage. Section 4 investigates the stress vectors. Section 5 analyzes the stress time and stress speed. Section 6 concludes this paper.

2. Oxide Thinning

SHOVE testing can increase the leakage current or cause oxide breakdown in a defective oxide whose thickness is less than expected. Oxide thinning shortens the lifetime of an oxide. As the oxide thickness is decreased in advanced technologies [Charnas 96] [Gronowski 96] [Montanaro 96] [Sanchez 96], oxide thinning becomes a more serious problem.

Several models have been proposed to predict the lifetime of an oxide and the onset criteria of oxide breakdown. Lee *et al.* proposed using "effective oxide thinning" to characterize time-dependent-dielectric-breakdown [Lee 88]. Sune *et al.* proposed a statistical description of oxide breakdown based on neutral trap generation in the oxide during wearout [Sune 90]. Dumin *et al.* found out that breakdown occurred locally when the local density of traps exceeded a critical value and the product of the electric field and the higher leakage currents through the traps exceeded a critical energy density [Dumin 94]. We use the "effective oxide thinning" model to estimate the lifetime of an oxide in this paper because this model shows the relationship among the voltage across an oxide, effective oxide thickness, and oxide lifetime more directly than other models. Equation 1 shows the relationship among these parameters. X_{eff} is the effective oxide thickness, V_{ox} is the voltage across the oxide, t_{BD} is the time-to-breakdown of the oxide, τ_0 is determined by the intrinsic breakdown time under an applied voltage of V_{ox}, and G is the slope of $\log(t_{BD})$ versus $1/E_{ox}$.

$$t_{BD} = \tau_0 \exp(\frac{GX_{eff}}{V_{ox}}) \qquad (1)$$

Table 1 shows the lifetime of a flawless and a defective oxide at different voltages for a 3.3V technology. The oxide thickness of this technology is 9nm. The thickness of the defective oxide is assumed to be half that of a flawless oxide. We assumed that the voltage across the oxide is approximately the same as the supply voltage. t_{BD} was calculated by using Equation 1. G is 350 MV/cm and τ_0 is 10 picoseconds [Lee 88].

Table 1 Lifetime of oxides

V_{ox}	E_{ox}(MV/cm)	t_{BD}	
		Flawless	Defective
3.3	3.67	9.04×10^{22} yrs	169.3 yrs
4.0	4.44	5.04×10^{15} yrs	14.6 days
5.0	5.56	7.26×10^{8} yrs	8.0 min
6.0	6.67	20,041 yrs	2.5 sec
7.0	7.78	11.1 yrs	60 msec
8.0	8.89	14.6 days	3.6 msec

Table 1 shows that the lifetime of a defective oxide is much shorter than that of a flawless oxide. It also shows that the lifetime of the oxide decreases as the supply voltage is increased. SHOVE testing should stress CUTs without affecting the property of flawless oxides significantly.

Researchers have reported the existence of stress-induced leakage current in a thin oxide film [Naruke 88] [Rofan 91] [Moazzami 92] [Dumin 93] [Patel 94]. It is found that the oxide leakage at low voltage increased in a thin oxide after the thin film was stressed at high voltage. The leakage current occurs before oxide breakdown and can be one of the major failure mechanisms in thin oxides.

The poly gate and channel region of a MOS transistor are highly doped. The energy barrier width is very thin at the defective site. Consequently, tunneling current occurs at the thin spot when an electrical field is applied across the oxide. The magnitude of the tunneling current increases significantly as the supply voltage increases over its normal value [Moazzami 92] [Dumin 93] [Lee 94]. Large tunneling currents can cause damage in an oxide layer and thus increase oxide leakage current. The failure mechanisms that cause the stress-induced oxide leakage can be localized defects [Olivo 88], localized positive charges [Maserjian 82], or trap states near the injecting surface [Rofan 91] [Moazzami 92]. These mechanisms further make X_{eff} in Equation 1 smaller and thus shorten the lifetime of an oxide. If the oxide thickness at the defect spot is very thin or the CUT is stressed long enough, oxide

breakdown may occur. Both stress-induced oxide leakage and oxide breakdown can significantly increase the quiescent current of a defective CUT.

3. Stress Voltage

To stress CUTs effectively, the stress voltage should be set such that it can only cause damage in the defective CUTs and avoid damaging flawless CUTs. Because the damage to an oxide at high voltage is mainly due to the tunneling current flowing through the oxide, the stress voltage should be selected so that the oxide tunneling current is very small in a flawless oxide but large in a defective oxide. Two types of tunneling mechanisms, Fowler-Nordheim tunneling and direct tunneling, can exist across an oxide. For most 3.3V and 5V technologies, the oxide thickness of a MOS transistor is larger than 6nm [Schutz 94] [Charnas 95] [Montanaro 96] [Sanchez 96] . Moreover, direct tunneling currents exist in a thin SiO_2 film whose thickness is less than 6nm [Schuegraf 92]. Consequently, Fowler-Nordheim tunneling currents dominates in the flawless oxide at high voltages for most 3.3V and 5V technologies. On the other hand, direct tunneling currents may exist at the thin spot in a defective oxide.

The magnitude of Fowler-Nordheim tunneling current strongly depends on E_{ox} [Schuegraf 92]. Based on various published measurement data, the magnitude of the Fowler-Nordheim tunneling current across an oxide becomes significant when E_{ox} is larger than 6MV/cm [Moazzami 92] [Dumin 93] [Dumin 94] [Watanabe 94] [Depas 96]. If the stress voltage is selected so that E_{ox} is approximately 6MV/cm in a flawless oxide, E_{ox} across a defective oxide will be much larger than this value. Thus, the tunneling current can flow through the defective site and increase the trap density at the thin spot during SHOVE. The oxide lifetime shown in Table 1 supports this observation too. Table 1 shows that the lifetime of a flawless oxide is still reasonably long when E_{ox} is 6.67MV/cm and that of a defective oxide is reduced to only several seconds. Table 2 lists E_{ox} at normal operating voltages for several technologies. For these technologies, E_{ox} at the normal operating voltage is well below 6MV/cm. In Table 2, V_{dd} is the supply voltage and T_{ox} is the oxide thickness.

Table 2 Maximum E_{ox} at normal operating voltages

Technologies	V_{dd} (V)	T_{ox}(nm)	E_{ox}(MV/cm)
[Schutz 94]	5	15	3.33
[Charnas 95]	3.3	8.5	3.88
[Sanchez 96]	2.5	7	3.57
[Montanaro 96]	2	6.5	3.08

Based on Equation 1, the higher the stress voltage is used, the shorter the stress will be. Consequently, to shorten the stress time, the stress voltage should be selected so that it can maximize the effect of the stress on the oxide layers of CUTs. Table 1 shows that the stress time for a transistor is approximately 8 min at 5V and 2.5 sec at 6V. Thus, the stress time can be reduced significantly by using the maximum allowed voltage during SHOVE.

Consequently, depending on the oxide thickness of a technology, the stress voltage for SHOVE testing can be determined. Equation 2 shows the maximum stress voltage for SHOVE testing. The unit of T_{ox} is nm.

$$V_{stress} = T_{ox} \times 0.6V / nm \qquad (2)$$

4. Stress Vectors

To thoroughly stress all the transistors in a CMOS IC and avoid long stress time, stress vectors must be selected so that the voltage across the oxide layer of a transistor is maximized. For an NMOS transistor, its source, drain, and substrate should be held at 0V, at the same time, the gate of the transistor is held at the stress voltage. For a PMOS transistor, its source, drain, and substrate should be held at the stress voltage and the gate of the transistor is held at 0V. Consequently, to effectively stress an NMOS transistor in a fully complementary CMOS logic gate, the stress vector should connect the logic gate output of and ground through the pull-down path that contains the target NMOS transistor. Similarly, to effectively stress a PMOS transistor in a fully complementary CMOS logic gate, the stress vector should connect the logic gate output and the supply voltage through the pull-up path that contains the target PMOS transistor.

To provoke a stuck-at-1 fault at the input of a complementary CMOS logic gate and propagate the fault effect to the output of the logic gate, the stuck-at vector will place logical 0 at the input of a PMOS transistor whose gate is connected to the faulty input node. In this way, the vector connects the output of the logic gate to the supply voltage through the PMOS transistor whose input gate is connected to the faulty input node. Thus, the PMOS transistor is put into the stress condition described in the previous paragraph. To provoke a stuck-at-0 fault at the input of a complementary CMOS logic gate and propagate the fault effect to the output of the logic gate, the stuck-at vector will place logical 1 at the input of an NMOS transistor whose gate is connected to the faulty input node. Similar to the vector for a stuck-at-1 fault at the input of the logic gate, the vector connects the output of the logic gate to ground through the NMOS transistor whose gate is connected to the faulty input node. As a result, the NMOS transistor is put into the stress condition mentioned in the previous paragraph. Moreover, a 100% single stuck-at test of a

complementary CMOS logic gate can toggle all input nodes of the logic gate. Thus, a 100% stuck-at test set for a complementary CMOS logic gate can put each transistor in the required stress condition at least once. Thus, both 100% single stuck-at test sets and pseudo stuck-at test sets can be used as the stress vectors for SHOVE. The latter are more suitable than the former because of their shorter test lengths. On the other hand, 100% toggle test sets may still miss some transistors. IDDQ test sets that target inter-gate bridging faults are not suitable for SHOVE testing. Figure 1 shows a fully complementary CMOS gate. Table 3 shows how transistors are stressed by stress vectors.

Because not all transistors are stressed by each test vector, some transistors may be stressed longer than others. Table 3 shows that all-zero vectors can stress all PMOS transistors and all-one vectors can stress all NMOS transistors at once. To stress all transistors evenly and reduce the stress time for fully complementary CMOS logic gates, all-one and all-zero vectors can perform better than stuck-at test sets as the stress vectors.
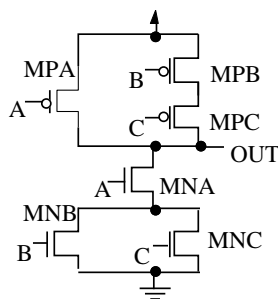

Figure 1 Fully complementary CMOS logic gate

Table 3 Stress vectors and the stressed transistors for a fully complementary CMOS logic gate

A	B	C	MPA	MPB	MPC	MNA	MNB	MNC
0	0	0	X*	X	X			
0	0	1	X					X
0	1	0	X				X	
0	1	1	X				X	X
1	0	0		X	X			
1	0	1				X		X
1	1	0				X	X	
1	1	1				X	X	X

* the transistor is stressed when the vector is applied

We can modify the algorithm for line justification used in existing ATPG programs to generate all-zero and all-one vectors. To justify the output value of a logic gate, the inputs of the logic gate should be set to either all ones or zeros. For example, if we want to set the output of a 2-input OR gate to be logical one, we should put logical ones on both inputs of the gate. In existing

ATPG programs, only one of the two inputs will be set to logical one.

5. Stress Time and Stress Speed

Each transistor in a CMOS IC must be stressed for long enough to make sure the defective oxide deteriorates significantly so that either oxide breakdown or stress-induced oxide leakage occurs in the defective oxide. To optimize the stress effect of each stress vector and thus reduce the total stress time, each signal should be held at its full-swing signal level for enough time. In this way, transistors can be in the condition mentioned in Sec. 4 and thus be stressed efficiently by the stress vectors.

If a transistor can be stressed more than once during SHOVE by different stress vectors, we can reduce the overall stress time for a CMOS IC. Equation 3 shows the stress time of a CMOS IC. In Equation 3, T_{sl} is the overall stress time of a CMOS IC, n is the number of stress vectors, T_{st} is the stress time for each transistor at the applied stress voltage, and m is the minimum number of vectors that stress a transistor for all transistors in the CUT. T_{st} can be calculated by using Equation 1.

$$T_{sl} = n \times T_{st} / m \qquad (3)$$

To determine an appropriate value for m, we investigated a CUT which was used in an experiment [Franco 95]. The CUT was implemented by using only elementary CMOS logic gates. It has 380 gates, 24 inputs, 12 outputs, and 283 internal nodes. Seven 100% single stuck-at test sets and two pseudo stuck-at test sets were used in this study. We simulated all test sets and recorded how each node toggled.

For the two pseudo stuck-at test sets, there was at least one node that was in the logic zero state only once for all test vectors. Thus, m should be 1 for these two test sets. The stress speed for this CUT should be the reciprocal of the stress time for a transistor if pseudo stuck-at test sets are used. For 5 out of the 7 100% single stuck-at test sets, each node was in logic zero or logic one state at least twice among all test vectors. As a result, m can be set at 2 for these test sets. Nevertheless, 97% of the nodes were in logic zero or logic one more than 4 times among all vectors in all 7 100% single stuck-at test sets.

6. Conclusions

SHOVE testing, VLV testing, IDDQ testing, and burn-in all aim at improving the quality level of CMOS ICs. We have shown that SHOVE testing can detect weak CMOS ICs caused by oxide defects. SHOVE testing requires shorter test time than burn-in and does not need extra instruments. Consequently, SHOVE testing is an alternative to burn-in and can be used with

VLV testing and IDDQ testing to improve the quality level of CMOS ICs and reduce the production cost.

Acknowledgments

References

[Chang 96] Chang, J.T.Y. and E.J. McCluskey, "Quantitative Analysis of Very-Low-Voltage Testing," *Proc. the 14th IEEE VLSI Test Symp.*, Princeton, NJ, pp. 332-337, Apr. 28-May 1, 1996.

[Charnas 95] Charnas, A., *et al.*, "A 64b Microprocessor with Multimedia Support," *1995 IEEE ISSCC*, San Francisco, CA, pp. 178-179, Feb. 15-17, 1995.

[Depas 96] Depas, M., *et al.*, "Critical Processes for Ultrathin Gate Oxide Integrity," *The Physics and Chemistry of SiO$_2$ and the Si-SiO$_2$ Interface - 3*, Vol. 96-1, pp. 352-366, 1996.

[Duey 93] Duey, S.J., A.R. Harvath, and P.G. Kowalczyk, "Improved Quality and Reliability Using Operating Extremes Test Methods," *Proc. 1993 IEEE CICC*, San Diego, CA, pp. 30.5.1-30.5.4, 1993

[Dumin 93] Dumin, D.J., and J. Maddux, "Correlation of Stress-Induced Leakage Current in Thin Oxides with Trap Generation Inside the Oxides," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 5, pp. 986-993, May 1993.

[Dumin 94] Dumin, D.J., J.R. Maddux, R.S. Scott, and R. Subramoniam, "A Model Relating Wearout to Breakdown in Thin Oxides," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 9, pp. 1570-1580, Sept. 1994.

[Franco 95] Franco, P., W.D. Farwell, R.L. Stokes, and E.J. McCluskey, "An Experimental Chip to Evaluate Test Techniques Chip and Experiment Design," *Proc. 1995 IEEE ITC*, Washington, DC, pp. 653-662, Oct. 21-25, 1995.

[Gronowski 96] Gronowski, P.E., *et al.*, "A 433MHz 64b Quad-Issue RISC Microprocessor," *1996 IEEE ISSCC*, San Francisco, CA, pp. 222-223, Feb. 8-10, 1996.

[Hao 93] Hao, H., and E.J. McCluskey, "Very-Low-Voltage Testing for Weak CMOS Logic IC's," *Proc. 1993 ITC*, Baltimore, MD, pp. 275-284, Oct. 17-21, 1993.

[Hnatek 95] Hnatek, E.R., *Integrated Circuit Quality and Reliability*, Second Edition, Revised and Expanded, Marcel Dekker, Inc., 1995.

[Josephson 95] Josephson, D., M. Storey, and D. Dixon, "Microprocessor I$_{DDQ}$ Testing: A Case Study," *IEEE Design and Test of Computers*, Vol. 12, No. 2, pp. 42-52, Summer 1995.

[Kowalczyk 90] Kowalczyk, P., "Wafer Leval Stress Testing: Containment of Infant Mortality Failures," *1990 WLR Workshop Final Rep.*, pp. 169-176, 1990.

[Lee 88] Lee, J.C., I. Chen, and C. Hu, "Modeling and Characterization of Gate Oxide Reliability," *IEEE Trans. Elec. Dev.*, Vol. 35, No. 12, pp. 2268-2278, Dec. 1988.

[Lee 94] Lee, S., B. Cho, J Kim, and S Choi, "Quasi-breakdown of Ultrathin Gate Oxide under High Field Stress," *Proc. 1994 IEEE Int. Elec. Dev. Meeting*, San Francisco, CA, pp. 605-608, Dec. 11-14, 1994.

[Levi 81] Levi, M., "CMOS is Most Testable," *Proc. 1981 ITC*, pp. 217-220, 1981.

[Maserjian 82] Maserjian, J., and N. Zamani, "Behavior of the Si / SiO$_2$ Interface Observed by Fowler Nordheim Tunneling," *J. Appl. Phys.*, Vol. 53, pp. 559-567, Jan. 1982.

[McCluskey 91] McCluskey, E.J., "Who Needs Design-For-Testability," *1991 IEEE ISSCC*, San Francisco, CA, Feb. 13-17, 1991.

[Moazzami 92] Moazzami, R., and C. Hu, "Stress-Induced Current in Thin Silicon Dioxide Films," *Proc. 1992 IEEE Int. Elec. Dev. Meeting*, San Francisco, CA, pp. 139-142, Dec. 13-16, 1992.

[Montanaro 96] Montanaro, J., *et al.*, "A 160MHz 32b 0.5W CMOS RISC Microprocessor," *1996 IEEE ISSCC*, San Francisco, CA, pp. 214-215, Feb. 8-10, 1996.

[Naruke 88] Naruke, K., S. Taguchi, and M. Wada, "Stress Induced Leakage Current Limiting to Scale Down EEPROM Tunnel Oxide Thickness," *Int. Elec. Dev. Meeting Tech. Dig.*, New York, NY, pp. 424-427, 1988.

[Olivo 88] Olivo, P., T.N. Nguyen, and B. Ricco, "High-Field-Induced Degradation in Ultra-Thin SiO$_2$ Films," *IEEE Trans. Elec. Dev.*, Vol. 35, No. 12, pp. 2259-2267, Dec. 1988.

[Patel 94] Patel, N.K., and A. Toriumi, "Stress-Induced Leakage Current in Ultrathin SiO$_2$ Films," *Appl. Phys. Lett.*, Vol. 64, No. 14, pp. 1809-1811, Apr. 4, 1994.

[Rofan 91] Rofan., R., and C. Hu, "Stress-Induced Oxide Leakage," *IEEE Elec. Dev. Let.*, Vol. 12, No. 11, pp. 632-634, Nov. 1991.

[Sanchez 96] Sanchez, H., *et al.*, "A 200MHz 2.5V 4W Superscalar RISC Microprocessor," *1996 IEEE ISSCC*, San Francisco, CA, pp. 218-219, Feb. 8-10, 1996.

[Schuegraf 92] Schuegraf, K.F., C.C. King, and C. Hu, "Ultra-thin Silicon Dioxide Leakage Current and Scaling Limit," *1992 Symp. on VLSI Tech. Dig. of Tech. Papers*, Seattle, WA, pp. 18-19, Jun. 2-4, 1992.

[Schuegraf 94] Schuegraf, K.F., and C. Hu, "Effects of Temperature and Defects on Breakdown Lifetime of Thin SiO$_2$ at Very-Low Voltages," *Proc. 1994 IEEE Int. Rel. Phys. Symp.*, San Jose, CA, pp. 126-135, Apr. 11-14, 1994.

[Schutz 94] Schutz, J., "A 3.3V 0.6 μm BiCMOS Superscalar Microprocessor," *1994 IEEE ISSCC*, San Francisco, CA, pp. 202-203, Feb. 16-18, 1994.

[Sune 90] Sune, J., I. Placencia, N. Barnoil, E. Farres, F. Martin, and X. Aymerich, "On the Breakdown Statistics of Very Thin SiO$_2$ Films," *Thin Solid Films*, Vol. 185, pp. 347, 1990.

[Syrzycki 87] Syrzycki, M., "Modelling of Spot Defects in MOS transistors," *Proc. 1987 ITC*, Washington, DC, pp. 148-157, Sept. 1-3, 1987.

[Watanabe 94] Watanabe, H., S. Aritome, G.J. Hemink, T. Maruyama, and R. Shirota, "Scaling of Tunnel Oxide Thickness for Flash EEPROMs Realizing Stress-Induced Leakage Current Reduction," *1994 Symp. on VLSI Tech. Dig. of Tech. Papers*, pp. 47-48, 1994.