Detecting Bridging Faults in Dynamic CMOS Circuits

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Abstract

New methods for detecting bridging faults in dynamic CMOS circuits are proposed. We show that resistive shorts in CMOS dynamic circuits can cause intermittent failures and reliability problems. We found that the defect coverage of resistive shorts, which we defined as the maximum detectable resistance of a short, in CMOS domino gates can be improved by increasing the supply voltage to be about 40% higher than the normal operating voltage or by reducing the supply voltage to about $2V_t$, where V_t is the threshold voltage of a transistor.

1. Introduction

Dynamic CMOS circuits are popular in speed critical designs because they can switch faster than static CMOS circuits [Colwell 95] [Heikes 96] [Kowaleski 96] [Naffziger 96] [Choudhury 97] [Jain 97]. We have studied the effects of resistive shorts on CMOS dynamic circuits and show that they can cause intermittent failures and reliability problems. In this paper, we focus on CMOS domino gates, as shown in Fig. 1, and inter-gate resistive shorts. Researchers have discussed the current testability of the intra-gate shorts in dynamic CMOS circuits [Renovell 93] [Ma 95].

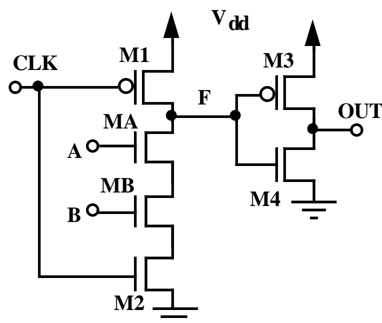

Figure 1 CMOS Domino Gate

CMOS domino gates switch faster than static CMOS circuits, but they are susceptible to noise and charge sharing problems. Also, because the clock signal is distributed to every CMOS domino gate, designs using CMOS domino gates consume more power and tend to have higher operating temperatures than those using only static CMOS gates. As will be shown later in Sec. 2, the effects of resistive shorts at different temperatures are very different. A resistive short that passes a test at room temperature can fail at high temperature. We assume that a test is normally performed at room temperature and the test time is too short to raise the temperature during a test. Consequently, an undetected resistive short in a CMOS domino gate can cause early-life failures or intermittent failures.

When the clock signal of a CMOS domino gate is low, the CMOS domino gate is in *precharge phase*. When the clock signal of a CMOS domino gate is high, the CMOS domino gate is in *evaluation phase*. There may be a floating node in a CMOS domino gate during evaluation phase. For the CMOS domino gate shown in Fig. 1, F can become a floating node in the evaluation phase if A and B are held low. During an IDDQ test, the voltage at F for a defect-free gate can drop due to the leakage current through MA, MB, M1, and M2. If we wait for all the signals in the *circuit-under-test* (CUT) to settle, the voltage at F may drop severely so that it may either turn on both M3 and M4 or switch OUT to the incorrect wrong logic state. The former case causes static current in the CUT. For the latter case, we cannot set the CUT into a desired state and thus will lose fault coverage. Consequently, because there may be floating nodes in CMOS domino gates, it is difficult to perform IDDQ testing on them.

Keepers, circuits that can alleviate charge sharing problems in CMOS domino gates, can effectively remove the floating nodes and thus make them IDDQ testable [Colwell 95]. Figure 2 shows an example of a CMOS domino gate with a keeper circuit. If all the CMOS domino gates in a CUT are implemented with keepers, there will not be any floating nodes in the domino gates. Thus, there will be no static current and we can put the CUT in any desired state. However, keepers are not always used in CMOS domino gates because they add parasitic capacitance at the critical nodes, reducing the performance of the CMOS domino gates [Williams 96]. We can skew the threshold voltage of the inverter stage of a CMOS domino gate by

properly sizing M3 and M4 to reduce the sensitivity of the inverter to voltage drop at its input. However, this will also impede the performance of a CMOS domino gate too. To enhance the performance of a CMOS domino gate, M3 and M4 should be designed so that the output node will switch from 0 to 1 faster than a CMOS static gate. This makes the output node very sensitive to the voltage drop at the input of the inverter. In this paper, we propose methods to detect bridging faults in high performance CMOS domino gates that do not have keepers but have skewed inverters.

Figure 2 CMOS Domino Gate with a Keeper

We investigated the voltage and temperature dependency of the faulty behavior of resistive shorts for CMOS domino gates without keepers. We found that *the defect coverage of resistive shorts*, which we defined as the maximum detectable resistance of a short, can be improved by increasing the supply voltage to about 40% higher than the normal operating voltage or by reducing the supply voltage to about 2 V_t, where V_t is the threshold voltage of a transistor. Furthermore, the defect coverage of resistive shorts in CMOS domino gates improves as the temperature increases.

This paper is organized as follows. Section 2 shows the temperature dependence of the defect coverage of resistive shorts in CMOS domino gates. Section 3 shows the defect coverage of resistive shorts in CMOS domino gates at different supply voltages. Section 4 discusses the proposed supply voltage range. Section 5 concludes the paper.

2. Defect Coverage at Different Temperatures

CMOS domino gates dissipate more power than static CMOS gates because the signals in CMOS domino gates switch every cycle. Consequently, CMOS domino gates increase the operating temperature faster than static CMOS gates. Also, the noise margin of a CMOS domino gate strongly depends on the threshold voltage of a transistor. As the temperature increases, the threshold voltage of a transistor decreases [Sze 81]. As a result, the noise margin of a CMOS domino gate reduces as the operating temperature increases. Consequently, resistive shorts with large resistance, which cannot be detected at normal operating voltage and room temperature, may fail when the operating temperature increases due to power dissipation of CMOS domino gates.

Figure 3 shows the simulated circuit. All four logic gates are implemented with CMOS domino circuits without keepers. A resistive short, shown as the thick line in Fig. 3, exists between the output nodes of two 2-input domino AND gates. We assumed that the resistance of the short does not change with changing temperature. All input and output nodes are properly buffered. All domino gates are driven by a single clock signal. The simulation is based on a 0.6 µm technology, whose normal operating voltage is 3.3V. The nominal threshold voltage for an NMOS transistor is 0.59V. All internal nodes were charged to the full-swing value during the precharge phase. In the evaluation phase, A, B, B1, and D1 were switched from 0 to 1. At the same time, C and D were held at 0. The resistive short was detected if OUTA and OUTC meet one of the following criteria:

a. OUTC changes from 0 to 1;
b. OUTA does not change from 0 to 1 or it changes ten times slower than expected.

Figure 3 Resistive Short

We performed the same simulation at four temperatures, $0^{o}C$, $25^{o}C$, $75^{o}C$, and $125^{o}C$. Figure 4 shows the defect coverage of the resistive short shown in Fig. 3 at different temperatures and at normal operating voltage 3.3V.

The results in Fig. 4 show that the defect coverage of the resistive short increases as the temperature increases when the supply voltage is held constant. For the simulated circuit, a short with resistance greater than 1.5 KΩ cannot be detected at room temperature. However, the defective CUT will fail at a higher

operating temperature. Thus, the defective CUT can pass at room temperature but fail in the system when the operating temperature becomes higher than room temperature. This can make a CUT fail intermittently or fail early in its lifetime. Therefore, resistive shorts in CMOS domino gates must be detected to ensure IC quality.

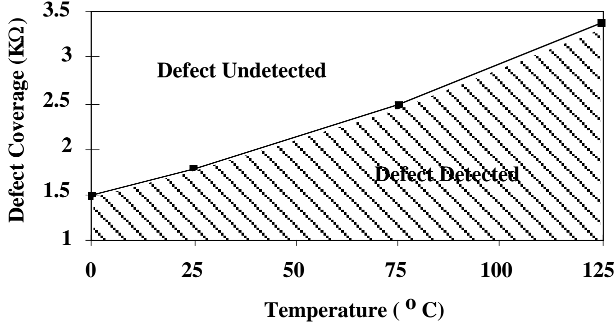

Figure 4 Defect Coverage at Different Temperatures for V_{dd} = 3.3V

3. Defect Coverage at Different Voltages

We used the same circuit in Fig. 3 to investigate the voltage dependence of the defect coverage of a resistive short. The operating temperature of the circuit was held at room temperature 25°C during the simulation. We assumed that the test time is too short for the device to heat up during the test at different voltages. Figure 5 shows the simulation results.

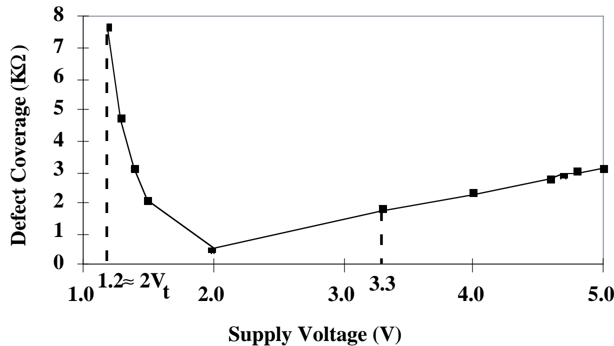

Figure 5 Defect Coverage at Different Voltages for temperature = 25°C

Based on the results shown in Fig. 5, we make the following observations.

A. The defect coverage of the resistive short improves as the supply voltage increases.
B. The defect coverage of the resistive short gets worse when the supply voltage is reduced from the normal operating voltage and before it is close to 2 V_t.
C. The defect coverage of the resistive short is best when the supply voltage is close to 2 V_t.

We will explain these observations qualitative in the following three paragraphs. At high voltage, the fault effect of the resistive short can be observed at OUTC in Fig. 3. Noise can couple from A1 through the resistive short to C1. If the coupled noise at C1 becomes larger than the threshold voltage of an NMOS transistor, it can cause G3 to switch. Thus, OUTC can switch from 0 to 1 unexpectedly. The magnitude of the coupled noise can be approximated by Equation 1. V_n is the magnitude of the coupled noise. R_s is the resistance of the resistive short. R_M is the equivalent resistance of the pull-down transistor (M4 in Fig. 1) of G1. Since G1 is turned on in the simulation setup, R_M is almost a constant. V_{dd} is the supply voltage. Based on Equation 1, the coupled noise is proportional to the supply voltage. Thus, the defect coverage improves when the supply voltage increases.

$$V_n = \frac{R_M}{R_s + R_M} \times V_{dd} \qquad (1)$$

At very low voltage, the effect of the resistive short becomes severe because the equivalent resistance of a transistor increases significantly at very low voltage [Hao 93] [Chang 96]. A1 is pulled down by the pull-down transistor (M4 in Fig. 1) of G1 to be smaller than the threshold voltage of a transistor at very low voltage. Thus, G2 cannot switch or it can only switch slowly. Consequently, we observe the fault effect at OUTA. The results in Fig. 5 show that the supply voltage should be as low as 2 V_t to improve defect coverage significantly.

However, if the supply voltage is reduced from its normal operating value but not as small as 2 V_t, the defect coverage becomes worse than that at the normal operating voltage. When the supply voltage is in this range, the coupled noise at C1 is too small to turn on G3 and the weakened signal at A1 is still much larger than the threshold voltage of a transistor and thus cannot turn off G2.

4. Which Supply Voltage?

The supply voltage used for testing resistive shorts in CMOS domino logic should be selected so that we can detect all the defects that can cause a CUT to fail at high operating temperature and normal operating voltage. Also, a defect-free CUT should still be functional at the selected supply voltage.

Figure 6 shows the defect coverage of the short shown in Fig. 3 at different voltages and different

temperatures. The gray region is the suggested supply voltage range for testing. The supply voltage should be either 40% higher than that of a normal operating voltage or about 2 V_t. The proposed supply voltage at very low voltage matches the one proposed in [Chang 96].

We also did a similar study, where we changed G2 and G3 to 4-input AND gates and obtained similar results. Figure 7 shows the voltage dependence of the defect coverage at different temperatures for the modified circuit. The gray region is the proposed supply voltage range. Even though the defect coverage is smaller than that of the short simulated in Fig. 3 at the same supply voltage and temperature, the conclusion for the proposed supply voltage range remains the same.

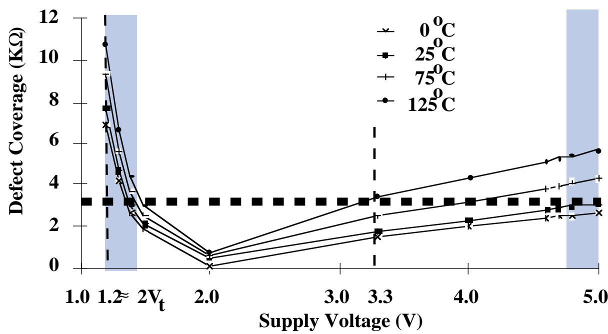

Figure 6 Desired Supply Voltage Range (in gray region)

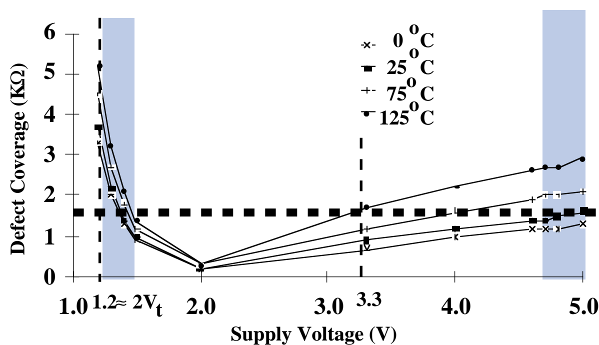

Figure 7 Desired Supply Voltage Range (in gray region) When G2 and G3 in Fig. 3 Are 4-Input AND Gates

5 Conclusion

If keepers are not used in all domino gates for a CUT, we can improve the defect coverage of resistive shorts in CMOS domino gates by either increasing the supply voltage to be 40% higher than the normal operating voltage or reducing the supply voltage to be as low as 2 V_t for the technology used in this paper.

Acknowledgments

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