Detecting Resistive Shorts for CMOS Domino Circuits

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ABSTRACT

We investigate defects in CMOS domino gates and derive the test conditions for them. Very-Low-Voltage Testing can improve the defect coverage, which we define as the maximum detectable resistance, of intra-gate and inter-gate resistive shorts. We also propose a new keeper design for CMOS domino circuits. The new keeper design has low performance impact and is best useful for small CMOS domino gates. Keepers can eliminate the floating nodes in CMOS domino logic gates.

1. INTRODUCTION

This paper investigates the problems associated with testing resistive shorts in CMOS domino circuits. We propose methods to detect resistive shorts in CMOS domino circuits and also show a new keeper design that can improve the testability of CMOS domino circuits without having a significant impact on the performance.

CMOS domino circuits are susceptible to leakage, noise, and charge-sharing problems [1-2]. Figure 1 shows a CMOS domino circuit without any keeper and internal prechargers. To ensure that CMOS domino circuits will function correctly, designers usually add keepers to eliminate leakage and noise problems, and add internal prechargers to eliminate charge sharing problems. Figure 2 shows an example of a CMOS domino circuit with a keeper and an internal precharger [3-4].

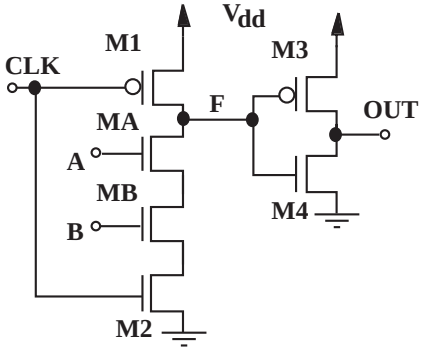

Figure 1 CMOS Domino Circuit

In Fig. 2, the keeper can hold the value at node F when the clock signal goes high and both inputs stay low throughout the evaluation phase. In this paper, node F in any CMOS domino circuit is referred to as a *dynamic node*. Without the keeper, the charge at the dynamic node can be discharged through leakage or be corrupted by noise. This can cause the logic value at the output to change to an incorrect value. During the precharge phase, the clock signal is low and thus turns on the PMOS internal precharger. The internal node can be precharged to V_{dd} so that the charge-sharing problem can be avoided.

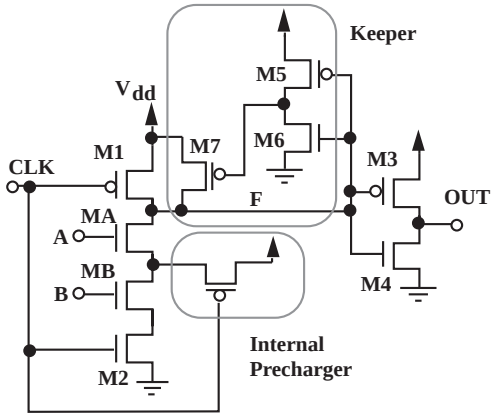

Figure 2 CMOS Domino Circuit with a Keeper

We first analyzed intra-gate and inter-gate resistive shorts in CMOS domino circuits without keepers. Some intra-gate shorts, such as gate oxide shorts can only cause small delay faults at normal voltage. We found that these shorts can become stuck-at faults at very low voltage. We have proposed VLV testing for static CMOS circuits [5-7]. The supply voltage for VLV testing should be $2V_t$ to $2.5V_t$ for static CMOS circuits, where V_t is the threshold voltage of a transistor [6-7]. For inter-gate resistive shorts, *the defect coverage of resistive shorts*, which we defined as the maximum detectable resistance of a short, can be improved by making the supply voltage about 40% higher than the normal operating voltage or by reducing the supply voltage to about $2V_t$. The defect coverage of inter-gate resistive shorts in CMOS domino circuits can also be improved by increasing the temperature.

I_{DDQ} testing is impractical for CMOS domino circuits without any keepers because of the potential floating node problem on any dynamic nodes. Section 6 describes this problem in detail. Keepers, circuits that can alleviate leakage and noise problems in CMOS domino circuits, can effectively remove the floating node problem and thus make these gates I_{DDQ} testable [3]. If all the CMOS domino circuits in a CUT are implemented with keepers, there will not be any floating nodes in the defect-free domino circuits. Therefore, CMOS domino circuits with keepers will not draw any static current and we can keep the CUT in a desired state. However, keepers are not always used in CMOS domino circuits because they add parasitic capacitance at the critical nodes, reducing the performance of these gates [8].

Keepers are seldom used in small CMOS domino circuits because of the significant performance impact. We propose a new keeper design for small CMOS domino circuits, one that has much less of a performance impact than other keeper designs. The detailed structure, simulation results, and comparison are provided in Sec. 5.

This paper is organized as follows. Section 2 lists the defects in CMOS domino circuits. Section 3 analyzes intra-gate resistive shorts in CMOS domino circuits. Section 4 investigates the defect coverage of inter-gate resistive shorts in CMOS domino circuits. Section 5 shows a new keeper design for small CMOS domino logic gates and compares it to other existing keeper designs. Section 6 investigates defects causing keepers to malfunction. Section 7 proposes the test conditions for detecting defective internal prechargers. Section 8 concludes the paper.

2 DEFECTS IN CMOS DOMINO CIRCUITS

Table 1 lists the defects and their corresponding failure modes in CMOS domino circuits. An intra-gate resistive short could be one of the shorts listed in the CrossCheck fault model [9], i.e., *a short between an interconnect and power (STP), a short between an interconnect and ground (STG), a short within a FET (SHF), or a short between two interconnects within a cell (SHI)*. An open defect could be one of the opens listed in the CrossCheck fault model, i.e., *an open within a FET (OPF) or an open interconnect within a cell (OPI)*. In the table, the defects in keepers and internal prechargers are separated from the defects in the other transistors in CMOS domino circuits. We classify the defects in this way because not all CMOS domino circuits necessarily have keepers and internal prechargers. To simplify the discussion, we consider only these defects that cause keepers or internal prechargers to disappear in CMOS domino circuits. The other defects in keepers or internal prechargers can degrade the effectiveness of the keepers or internal prechargers.

Depending on their resistance, intra-gate or inter-gate resistive shorts can increase the propagation delay of a gate, cause an input node or an output node to be stuck at some logic value, reduce noise margin, or draw excessive current. Reduced noise margin means that the signal at the output of the circuit is degraded. Reduced noise margin is a more complicated problem for CMOS domino circuits than for static CMOS circuits. If the defective gate with reduced noise margin at its output is followed by another CMOS domino circuit, it can cause that gate to switch to an incorrect logic state and if this switch occurs, the defect can be detected. However, if the defective gate is followed by a static CMOS gate or a latch, it may not cause the following gate to switch incorrectly and thus may not be detected.

Open defects (both OPF and OPI) cause fewer problems in CMOS domino circuits than in static CMOS circuits. Because CMOS domino circuits precharge in every cycle, one can detect most open defects, except the ones in PMOS precharge transistors, by using a single test vector. Researchers have studied and proposed methods to detect opens in CMOS domino circuits [10-11].

Table 1 Defects and Corresponding Failure Modes in CMOS Domino Circuits

Defects	Failure Modes
Intra-gate resistive shorts: Shorts between an interconnect and power (STP) Shorts between an interconnect and ground (STG) Shorts within a FET (SHF) Shorts between two interconnects within a cell (SHI)	Increased gate delay, stuck-at faults, reduced noise margin, or leakage
Inter-gate resistive shorts	Increased gate delay, stuck-at faults, reduced noise margin, or leakage
Opens within a FET (OPF) Open interconnects within a cell (OPI)	Stuck-at faults or stuck-open faults
Missing keepers	Coupling noise or leakage
Missing internal prechargers	Charge sharing or leakage

Missing keepers or internal prechargers do not always cause CMOS domino circuits to switch incorrectly. The defective CMOS domino circuits can fail intermittently instead. Because keepers are used to avoid leakage and noise problems in CMOS domino circuits, missing keepers result in the defective CMOS domino circuits malfunctioning due to leakage or noise. Similarly, because internal prechargers are used to eliminate charge-sharing problems, missing internal prechargers can make the defective CMOS domino circuits susceptible to charge-sharing problems. The issues in testing missing keepers and internal prechargers are discussed in Sec. 6 and 7.

Since other researchers have studied and proposed methods to detect open defects in CMOS domino circuits [10-14], we focused on intra-gate resistive shorts, inter-gate resistive shorts, missing keepers, and missing internal prechargers in this study.

3 INTRA-GATE RESISTIVE SHORTS

We use the four shorts listed in the CrossCheck fault model in this section. In addition, we consider shorts with high and low resistance.

3.1 Shorts within a FET

We focus on gate-drain and gate-source shorts in all transistors of a CMOS domino circuit. Drain-source shorts are similar to transistor stuck-on faults. Researchers have reported methods for detecting transistor stuck-on faults [10-15]. Most drain-source shorts in transistors of a CMOS domino circuit, except the one in the NMOS clocked evaluation transistor (M2 in Fig. 1), can be detected by Boolean tests at normal operating voltage [16]. Consequently, we do not include drain-source shorts in this discussion.

In this study, we used CMOS domino circuits without keepers for the investigation of gate oxide shorts. However,

our conclusions can be directly applied to all CMOS domino circuits. Gate oxide shorts with low resistance can be detected by Boolean tests at normal operating voltage. Those that escape Boolean tests at normal operating voltage can be detected through VLV testing.

We injected gate oxide shorts in a 4-input AND gate. Figure 3 shows the simulated CMOS domino circuit. Figure 4 shows the simulation setup. All the inputs, except the clock signal, were buffered by CMOS domino buffers. The clock signals were buffered by static CMOS buffers. The OR gate was properly loaded. We assumed that the output is observable only in the evaluation phase. A 0.6 μm technology, whose normal operating voltage is 3.3V, was used for all simulations discussed in this section. The nominal threshold voltage for an NMOS transistor is 0.59V.

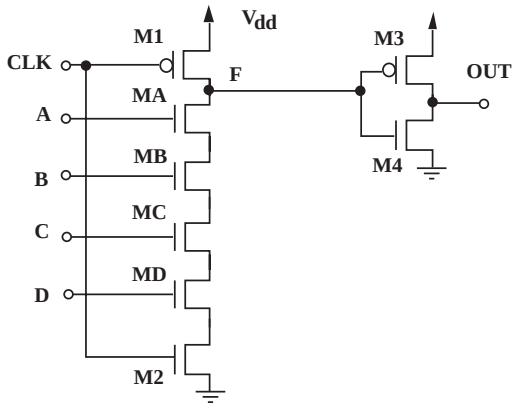

Figure 3 4-Input AND Gate

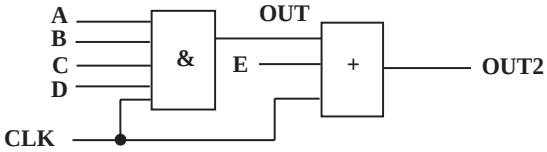

Figure 4 Simulation Setup

We can improve the defect coverage by reducing the operating voltage during testing. At low voltages, the equivalent resistance of a transistor increases while the resistance of a short remains almost the same [5-6]. Consequently, the fault effect of a resistive short is more significant at low voltages. For the defective gate discussed in this section, the voltage at the dynamic node is close to zero at low voltage for a short with high resistance. Thus, the defect behaves like a stuck-at-one fault at the output of the CMOS domino circuit. Table 2 lists the defect coverage of different SHFs at different supply voltages. The italicized rows indicate the supply voltage range proposed for VLV testing [6-7]. The detailed description of the test condition for each SHF can be found in Appendix A.

The gate-drain and gate-source shorts in the other NMOS transistors in the evaluation network behave similarly to the gate-drain and gate-source shorts in MA during the evaluation phase. The difference is that the shorts in the other transistors do not cause any fault effect during the precharge phase. However, they can be detected in a similar way. The defect coverage of gate-source short in M4 and gate-drain shorts in either M3 or M4 is larger than 10 KΩ at normal operating supply voltage.

Table 2 Defect Coverage of SHFs at Different V_{dd}

V_{dd} (V)	$\frac{V_{dd}}{V_t}$	Defect coverage(KΩ)						
		MA GD*	MA GS**	M1 GD	M1 GS	M2 GD	M2 GS	M3 GS
1.2	*2.0*	*≤20*	*≤13*	*≤14*	*≤2.6*	*≤5.3*	*≤5.0*	*≤15*
1.5	*2.5*	*≤17*	*≤6.4*	*≤5.1*	*≤1.1*	*≤1.7*	*≤1.7*	*≤8.2*
1.7	2.9	≤14	≤4.6	≤3.7	≤0.5	≤1.0	≤1.1	≤6
2.0	3.4	≤11	≤3.1	≤2.6	≤0.5	≤0.6	≤0.8	≤4.4
2.5	4.2	≤9	≤2.0	≤1.9	≤0.3	≤0.3	≤0.5	≤3.1
3.3	5.6	≤5	≤1.2	≤1.5	≤0.2	≤0.2	≤0.3	≤2.1

* GD: gate-drain short
** GS: gate-source short

The gate-source short in M1 is the only short in a CMOS domino circuit that requires a two-pattern test for detection. The first pattern should discharge the dynamic node and thus set the output of the domino circuit to be one in the evaluation phase. The second pattern should be set so that the output of the domino circuit does not switch from zero to one during the evaluation phase.

3.2 Shorts between an Interconnect and Power

All STPs in a CMOS domino circuit can be detected by a 100% SSF test set for the gate. The test condition for each STP can be found in Appendix A.

3.3 Shorts between an Interconnect and Ground

Except the STG at the drain node of the NMOS evaluation transistor, all the other STGs in a CMOS domino circuit can be detected by a 100% SSF test set for the gate. An STG at the drain node of the NMOS evaluation transistor can only increase the power consumption of the domino circuit. This STG cannot cause the domino circuit to fail functionally. Appendix A shows the test conditions of all the STGs in a CMOS domino circuit.

3.4 Shorts between Two Interconnects within the Cell

If an SHI occurs within a transistor of a CMOS domino circuit, it is the same as an SHF, whose test condition has been shown in Sec. 3.1 and Appendix A. We consider a short between an input/output and an internal node within the cell as an SHI too. Most SHIs can be detected by applying a 100% SSF test set. There are two types of SHIs that cannot be detected by a 100% SSF test set. One is an SHI between an input and a source node of any NMOS transistor in the evaluation network and the two defective NMOS transistors are not in the same transistor stack. The other is an SHI between the output and a source node of any NMOS transistor in the evaluation network. However, these two types of SHIs can be detected by a single vector. The test condition for each SHI in a CMOS domino circuit can be found in Appendix A.

3.5 Summary

All but one gate oxide short in a CMOS domino circuit can be provoked by the test vectors for stuck-at pin faults. Only one short, the gate-source short in the precharge PMOS transistor, requires a two-pattern test. We can improve the defect coverage of gate oxide shorts by using VLV Testing [5]. Based on the data shown in Table 2, the supply voltage for VLV Testing should be set between $2V_t$ and $2.5V_t$ [6-7].

All STPs and STGs and most SHIs in CMOS domino circuits can be detected by single stuck-at test vectors. There are two types of SHIs in CMOS domino circuits that cannot be detected by single stuck-at test vectors. Nevertheless, they can still be detected by a vector at the nominal supply voltage.

4 INTER-GATE RESISTIVE SHORTS

CMOS domino circuits dissipate more power than static CMOS circuits because the signals in CMOS domino circuits switch every cycle. Consequently, CMOS domino circuits increase the operating temperature faster than static CMOS circuits. Also, the noise margin of a CMOS domino circuit strongly depends on the transistor threshold voltage. As the temperature increases, the transistor threshold voltage decreases [17]. As a result, the noise margin of a CMOS domino circuit decreases as the operating temperature increases. Consequently, resistive shorts with high resistance, which cannot be detected at normal operating voltage and room temperature (25°C), may fail when the operating temperature increases due to power dissipation of CMOS domino circuits.

Figure 5 shows the simulated circuit. All four logic gates are implemented with CMOS domino circuits without keepers. A resistive short, shown as the thick line in Fig. 5, exists between the output nodes of two 2-input domino AND gates. We assumed that the resistance of the short does not change with changing temperature. The detailed description of the simulation setup and results can be found in Appendix B.

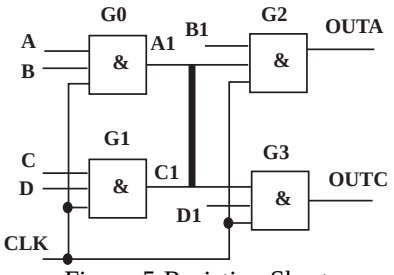

Figure 5 Resistive Short

The supply voltage used for testing resistive shorts in CMOS domino logic should be selected so that we can detect all the defects that can cause a circuit to fail at high operating temperature and normal operating voltage. Also, a defect-free circuit should still be functional at the selected supply voltage. Figure 6 shows the defect coverage of the short shown in Fig. 5 at different voltages and different temperatures. The gray region is the suggested supply voltage range for testing. The supply voltage should be either 40% higher than a normal operating voltage or about $2V_t$. The proposed supply voltage at very low voltage matches the one proposed in [6-7].

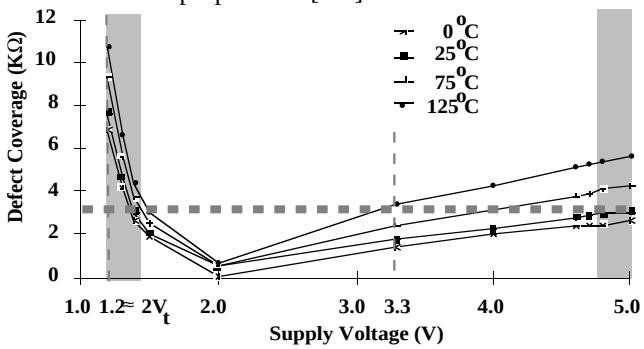

Figure 6 Desired Supply Voltage Range (in Gray)

We also did a similar study, in which we changed G2 and G3 to 4-input AND gates, and obtained similar results.

5 KEEPERS

When the clock signal of a CMOS domino circuit is low, the CMOS domino circuit is in *the precharge phase*. When the clock signal of a CMOS domino circuit is high, the CMOS domino circuit is in *the evaluation phase*. The dynamic node in a CMOS domino circuit, node F in Fig. 1, may become a floating node during the evaluation phase. For the CMOS domino circuit shown in Fig. 1, F becomes a floating node in the evaluation phase if A and B are held low. During an I_{DDQ} test or a slow functional test, the voltage at F for a defect-free gate can drop due to the leakage current through MA, MB, M1, and M2. If we wait for all the signals in the CUT to settle, the voltage at F may drop severely enough to either turn on both M3 and M4 or change OUT to an incorrect logic state. The former case causes static current in the CUT. For the latter case, we cannot set the CUT into a desired state and thus will lose fault coverage. Consequently, it is not only difficult to perform I_{DDQ} testing on CMOS domino circuits, but they also require high speed Boolean testing.

Keepers are the transistors that are added to a CMOS domino circuit to make dynamic node static. Keepers, which are used to eliminate leakage and noise problems, remove the floating node problem and make the operation of CMOS domino circuits static. Not only do keepers ensure CMOS domino circuits function correctly, they also help remove the two testing problems mentioned in the previous paragraph.

Keepers, however, can degrade the switching speed of CMOS domino circuits. The impact of keepers is not significant for the performance of complex CMOS domino circuits, but can be severe for that of small CMOS domino circuits, such as a 2-input OR gate or a 2-input AND gate. If these gates appear in critical paths, keepers usually are not used. However, if keepers are not used for all CMOS domino circuits in a CUT, the background current can still be too large to perform I_{DDQ} testing and we must test CUTs at-speed to avoid losing logic states in CMOS domino circuits without keepers.

We studied several keeper designs [3-4] and propose a new design specifically for small CMOS domino circuits. Figure 7 shows the new keeper design for a 2-input AND gate. Figure 8 shows the new keeper design for a 2-input OR gate. Both MKA and MKB in Fig. 7 and Fig. 8 are minimum-size PMOS transistors. Figure 9 is a keeper design that has been used for CMOS domino circuits with small channel width. In Fig. 2, MK1, MK2, and MK3 are minimum-size transistors. In Fig. 9, MK1 is a PMOS transistor with minimum gate width but large channel length. MK2 is a minimum-size PMOS transistor. We will refer to the new keeper design as keeper design A, the keeper implementation in Fig. 2 as keeper design B, and the keeper implementation in Fig. 9 as keeper design C. The operation of keeper design C is similar to that of keeper design B. The PMOS transistor with larger channel length is added to weaken the strength of the keeper. In this way, we can keep the extra loading at the output node at the level of the gate capacitance of a minimum-size PMOS transistor and also reduce the performance impact.

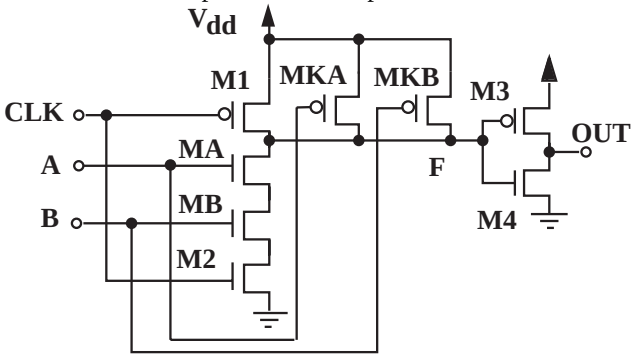

Figure 7 2-input AND Gate with Keeper Design A

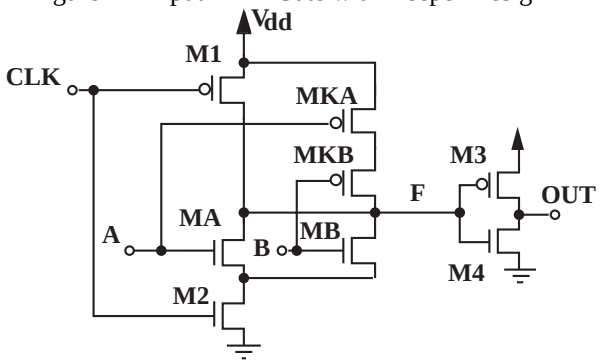

Figure 8 2-input OR Gate with Keeper Design A

The structure of a CMOS domino circuit with keeper design A is similar to that of a static CMOS logic gate. The difference is that the clock signal precharges the dynamic node to one during the precharge phase and the transistors are sized so that we optimize only single-end transitions. Keeper design A adds extra loading at the input of a CMOS domino circuit. However, since the PMOS transistors are very small, the keeper has minimal impact on the input loading. It adds only very small diffusion capacitance to the dynamic node, F in Fig. 1, of a CMOS domino circuit. Although keeper designs B and C do not add any extra loading at the input of a CMOS domino circuit, they add the loading somewhere else. Keeper design B adds gate capacitance and a small diffusion capacitance to the dynamic node of a CMOS domino circuit. Keeper design C adds gate capacitance to the output of a CMOS domino circuit and a small diffusion capacitance to the dynamic node. The other advantage of keeper design A is that it can correct an erroneous transition at slow speed.

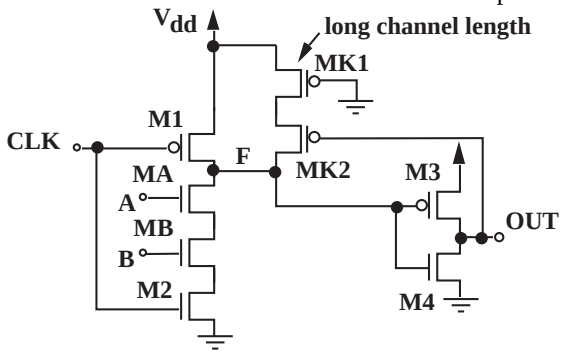

Figure 9 Keeper Design C

We simulated a 2-input AND gate, a 4-input AND gate, a 2-input OR gate, and a 4-input OR gate. Each gate was implemented with different keeper designs. The simulations were based on two sub micron technologies. One is a 0.35 μm LSI Logic G10p technology. The other is a 0.6 μm HP CMOS14TB technology. The simulated CMOS domino circuits with different keeper designs all have the same size except for their keepers. All internal nodes in the evaluation network were precharged to V_{dd} before the evaluation phase. We used the fanout-of-four rule at the output load of each gate, and we measured the propagation delay through each CMOS domino circuit.

Tables 3-6 show the simulation results. The number in each table is the propagation delay of a CMOS domino circuit with a keeper normalized by the propagation delay of the same domino circuit implemented without any keeper. The parameter λ is half of the feature size. The size listed in the first column of each table is the transistor size of an NMOS transistor in the evaluation network of each CMOS domino circuit.

Table 3 Simulation Results for a 2-Input AND Gate

size	Td (with keeper) / Td (without keeper)					
	0.35 μm technology			0.6 μm technology		
	Keeper A	keeper B	keeper C	Keeper A	keeper B	keeper C
3.1λ*	**1.06**	1.58	1.23	**1.07**	1.77	1.25
4.7λ	**1.02**	1.37	1.14	**1.02**	1.31	1.14
6.3λ	**1.00**	1.26	1.09	**0.99**	1.19	1.09
7.8λ	**0.99**	1.19	1.07	**0.98**	1.13	1.07
9.4λ	**0.98**	1.15	1.05	**0.97**	1.10	1.05
10.9λ	**0.97**	1.12	1.03	**0.97**	1.08	1.04
12.5λ	**0.96**	1.11	1.02	**0.97**	1.06	1.03
14.1λ	**0.96**	1.09	1.02	**0.97**	1.05	1.03
15.6λ	**0.96**	1.08	1.01	**0.97**	1.04	1.02

* $\lambda = 0.5 \times$ feature size

Table 4 Simulation Results for a 4-Input AND Gate

size	T_d (with keeper) / T_d (without keeper)					
	0.35 μm technology			0.6 μm technology		
	Keeper A	keeper B	keeper C	keeper A	keeper B	keeper C
6.3λ*	**1.13**	1.36	1.16	**1.10**	1.29	1.12
9.4λ	**1.08**	1.21	1.10	**1.04**	1.14	1.07
12.5λ	**1.05**	1.14	1.07	**1.02**	1.09	1.05
15.6λ	**1.03**	1.11	1.06	**1.00**	1.06	1.04
18.8λ	**1.02**	1.08	1.04	**0.99**	1.04	1.03
21.9λ	**1.02**	1.07	1.04	**0.99**	1.03	1.03
25.0λ	**1.01**	1.06	1.03	**0.98**	1.03	1.02
28.1λ	**1.01**	1.05	1.03	**0.98**	1.02	1.02
31.3λ	**1.00**	1.04	1.02	**0.98**	1.02	1.02

* $\lambda = 0.5 \times$ feature size

Table 5 Simulation Results for a 2-Input OR Gate

size	T_d (with keeper) / T_d (without keeper)					
	0.35 μm technology			0.6 μm technology		
	keeper A	keeper B	keeper C	keeper A	keeper B	keeper C
3.1λ*	**1.08**	1.33	1.16	**1.05**	1.37	1.13
3.9λ	**1.06**	1.26	1.13	**1.03**	1.23	1.09
4.7λ	**1.05**	1.21	1.11	**1.03**	1.16	1.07
5.5λ	**1.04**	1.18	1.09	**1.02**	1.12	1.06
6.3λ	**1.03**	1.15	1.08	**1.02**	1.10	1.05
7.0λ	**1.03**	1.13	1.07	**1.01**	1.08	1.04
7.8λ	**1.02**	1.11	1.06	**1.01**	1.07	1.04

* $\lambda = 0.5 \times$ feature size

Table 6 Simulation Results for a 4-Input OR Gate

size	T_d (with keeper) / T_d (without keeper)					
	0.35 μm technology			0.6 μm technology		
	keeper A	keeper B	keeper C	keeper A	keeper B	keeper C
3.1λ*	**1.14**	1.34	1.16	1.11	1.37	1.13
3.9λ	1.11	1.27	1.13	1.08	1.23	1.09
4.7λ	1.09	1.21	1.11	1.06	1.16	1.07
5.5λ	1.08	1.18	1.09	1.05	1.12	1.06
6.3λ	1.07	1.15	1.08	1.04	1.10	1.05
7.0λ	1.06	1.13	1.07	1.04	1.08	1.04
7.8λ	1.05	1.11	1.06	1.03	1.07	1.04

* $\lambda = 0.5 \times$ feature size

The results show that keeper design A has much less impact on the propagation delay of a CMOS domino circuit. For a 2-input AND gate and a 4-input AND gate, the propagation delay of a CMOS domino circuit using keeper design A can have similar or slightly smaller propagation delay than the same domino circuit without any keeper. The reason is as follows: When a CMOS domino circuit goes into the evaluation phase, the clock signal can push the dynamic node F to a voltage slightly higher than V_{dd} through the parasitic capacitance between the gate and drain of the PMOS precharge transistor. For a CMOS domino circuit without any keeper, the extra charge on the dynamic node can only leak through the very small substrate leakage of the precharge PMOS transistor and the NMOS transistor at the top of the evaluation network. There is not enough time for the extra charge to leak away before the CMOS domino circuit switches. Hence, during the evaluation phase, the dynamic node must discharge the extra charge coupled through the clock signal. On the other hand, the keeper can provide a path between the dynamic node and V_{dd}. Right after the clock signal goes high, the extra charge can be discharged through the PMOS transistors in the keeper. Consequently, it needs to discharge less charge on the dynamic node when the domino circuit switches. Thus, when the size of the NMOS transistors in the evaluation network is much larger than the size of the PMOS transistors in the keeper, a CMOS domino circuit with keeper design A can switch slightly faster than one without a keeper.

The results in Tables 3-6 show that the new keeper design (A) has less performance impact on a CMOS domino circuit than the other two keeper designs. We suggest that keepers be used in all CMOS domino circuits in a CUT. Depending on the applications, designers can use any keeper design that minimizes the performance penalty. Boolean tests should be used to test CUTs if keepers are not used in all CMOS domino circuits.

6 MISSING KEEPERS

Keepers are used in most CMOS domino circuits to eliminate leakage and reduce noise problems. They keep the dynamic nodes in CMOS domino circuits from floating. If all the domino circuits in a CUT have keepers, the CUT can be operated at low speed without losing logic states.

If a defect causes a keeper to disappear in a CMOS domino circuit, the defective gate becomes susceptible to leakage and noise problems. If the defective gate stays in the evaluation phase long enough, the leakage can discharge the dynamic node and thus change the logic state of the defective gate. The defective domino circuit can also fail due to the noise coupled to its dynamic node.

If all the CMOS domino circuits in a CUT have keepers, the defective keeper can be detected by testing the CUT slowly. However, if not all the CMOS domino circuits use keepers, the CUT cannot be operated at low frequencies. In this case, we can use the verification vectors generated by designers for verifying the effects of coupling noise. Because the magnitude of coupling noise is proportional to supply voltage, we can test the CUT at high voltage to maximize the effect of noise coupled to the dynamic node of the defective domino circuit.

7 MISSING INTERNAL PRECHARGERS

If one or more nodes in the evaluation network (e.g., the source node of MA in Fig. 2) is not precharged to V_{dd}

before a domino circuit goes into the evaluation phase, a charge-sharing problem may occur during the evaluation phase if all the inputs of the domino circuit are held at V_{dd} except the input to the bottom transistor in the evaluation network (e.g., input B in Fig. 2). Keepers, however, can hardly help the charge-sharing problem since they are too weak to charge all the internal nodes to V_{dd}. Internal prechargers, such as the one shown in Fig. 2, are often used to remove the charge-sharing problem [4].

A defect that causes the internal prechargers to disappear makes the defective CUT susceptible to the charge-sharing problem. This problem, similar to the coupling-noise and leakage problem, does not always cause the defective CUT to fail immediately.

The test vector that sets all but the bottom NMOS transistors in the evaluation network to one is the vector that makes the CUT most vulnerable to charge sharing. This is the same test vector that detects a stuck-at-1 fault at the input node that is connected to the bottom-most transistor in the evaluation network. Thus, a 100% single stuck-at test set can be used as the test set for detecting charge sharing. Moreover, because the voltage drop caused by charge sharing is proportional to supply voltage, we can put the defective CUT into the worst-case charge-sharing condition by running 100% single stuck-at test vectors at the highest operating voltage.

8 CONCLUSIONS

We found that most gate oxide shorts with low resistance in a CMOS domino circuit can be detected by Boolean tests at normal voltage. Only one gate oxide short requires a two-pattern test for detection. VLV Testing can be used to improve the defect coverage of gate oxide shorts. We can improve the defect coverage of inter-gate resistive shorts in CMOS domino circuits by either making the supply voltage 40% higher than the normal operating voltage or making it as low as $2V_t$ for the technology used in this study.

We suggest that keepers be used in all CMOS domino circuits. Not only can keepers eliminate leakage and noise problems, they also remove the floating node problem in CMOS domino circuits and thus make CMOS domino circuits more testable. Keepers also make CMOS domino circuits consume very small static currents and make them IDDQ testable.

One can detect missing keepers by testing CUTs slowly if all CMOS domino circuits used in the CUTs have keepers. One can detect missing internal prechargers by running 100% single stuck-at test sets at the highest operating voltage.

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Appendix A Intra-Gate Resistive Shorts

A.1 SHF

Gate-drain short in MA (Fig. 3)

We should set A to be zero during the evaluation phase to provoke this defect. During the precharge phase, there is a conducting path between V_{dd} and ground through the short, the precharge PMOS transistor, and the NMOS transistor in the inverter of the preceding domino gate. If the short has very low resistance, the voltage level at the dynamic node in the defective gate is close to zero. The output of the defective gate is one and that of a defect-free gate is zero. If A is set to be zero during the evaluation

phase, the charge at the dynamic node in the defective gate can discharge through the short. Thus, for a gate-drain short with low resistance, the output of the defective gate will switch to one and that of a defect-free gate remains zero. The erroneous transition should finish within a cycle and we should therefore be able to detect the short. If the defective gate is the first gate in a critical path, the time from the rising edge of the clock signal to when the erroneous transition occurs at the output of the defective gate should be shorter than the propagation delay of a defect-free gate for successful detection.

We can improve the defect coverage by reducing the operating voltage during testing. Table 2 lists the defect coverage of the gate-drain short at different supply voltages.

The gate-drain shorts in the other NMOS transistors in the evaluation network behave similarly to the gate-drain short in MA during the evaluation phase. The difference is that the shorts in the other transistors do not cause any fault effect during the precharge phase.

Gate-source short in MA (Fig. 3)

We should set A to be one during the evaluation phase to provoke the defect. To sensitize the fault effect to the output of the domino gate, the other input signal should also be set to one during the evaluation phase.

If the short resistance is low, e.g., 1 KΩ, the voltage level at node A can be pulled below the threshold voltage of an NMOS transistor at normal operating supply voltage. The dynamic node cannot be discharged during the evaluation phase and the defect behaves as a stuck-at-zero fault at the input node of the defective transistor. However, for high short resistance, the defect can only increase the propagation delay of the defective gate.

The fault effect of the gate-source short can become significant at voltages well below the normal operating voltage. Defects with high short resistance can behave like stuck-at faults or large delay faults. The gate-source shorts in the other NMOS transistors in the evaluation network behave similarly to the one in MA.

Gate-source short in M3 (Fig. 3)

We should set all the inputs of a CMOS domino gate to be one during the evaluation phase to provoke the defect. For a defect with low short resistance, the defect behaves like a stuck-at-one fault at the output of the defective CMOS domino gate. However, the short can only increase the propagation delay of the defective gate if it has high resistance. The defect coverage of this short can also be improved by using VLV Testing.

Gate-source short in M4 (Fig. 3)

We should set the inputs of the CMOS domino gate so that the output node will not switch during the evaluation phase. The defect behaves like a stuck-at-one fault at the output of the CMOS domino gate. The short provides a path between the dynamic node and ground. Consequently, the charge at the dynamic node will discharge right after the domino gate enters the evaluation phase. The defect coverage of a Boolean test at normal operating supply voltage is larger than 15 KΩ.

Gate-drain short in either M3 or M4 (Fig. 3)

We should set the inputs of a CMOS domino gate in such a way that its output node will not switch during the evaluation phase. The defect coverage of a Boolean test at normal supply voltage is larger than 10 KΩ.

Gate-drain short in M1 (Fig. 3)

We should set the inputs of a CMOS domino gate and its following domino gate so that their outputs will not switch during the evaluation phase. The fault effect can only be observed at the output of the following CMOS domino gate. If the short resistance is low, e.g., 500 Ω, the dynamic node stays at zero during the precharge phase. The output of the CMOS domino gate is one before the gate enters the evaluation phase. When the clock goes high at the beginning of the evaluation phase, the dynamic node can be charged to V_{dd} through the short. The output of the defective domino gate can switch to its defect-free value, zero. Before the output node returns to its defect-free value, the following domino gate has been triggered by the erroneous logic value at the output of the defective domino gate right after the clock has gone high. Thus, we can observe the fault effect at the output of the domino gate following the defective domino gate. If the short resistance is high, the short can be detected at very low voltage.

If the defective gate is followed by a latch or a static CMOS gate, the short cannot be detected. It is unlikely that the short can cause the defective CUT to malfunction if the defective gate is followed by a latch or a static CMOS gate. For a short with low resistance, the output of the defective domino gate will either be a correct logic value or the gate will switch faster than a defect-free one. For a short with high resistance, the output of the defective domino gate will also either be a correct logic value or the gate will switch slightly slower than it is supposed to.

Gate-source short in M1 (Fig. 3)

This is the only short in a CMOS domino gate that requires a two-pattern test for detection. The first pattern should discharge the dynamic node and thus set the output of the domino gate to be one in the evaluation phase. The second pattern should be set so that the output of the domino gate does not switch from zero to one during the evaluation phase. If the short has low resistance, it can effectively turn off the precharge PMOS transistor during the precharge phase. Consequently, the dynamic node cannot be charged to V_{dd} in the second cycle. The output of a defective gate should remain at V_{dd} in the second cycle. If the resistance of the short is large, the dynamic node can still go to V_{dd} during the precharge phase. Consequently, a defective CUT with large short resistance can still function correctly at normal operating voltage. The defect coverage can be improved by testing the CUT at very low voltage.

Gate-drain and gate-source short in M2 (Fig. 3)

To detect either of the shorts, we should set the inputs so that the output of a CMOS domino gate switches from zero to one during the evaluation phase. If the resistance of the short is very small, it can prevent the dynamic node from discharging. Thus, the defect behaves as a stuck-at-zero fault at the output of a CMOS domino gate. However,

the defect coverage is poor at normal operating voltage. We can improve the defect coverage of either short by reducing the supply voltage during testing.

A.2 STP

If an STP occurs at the input or output node of a CMOS domino gate, the domino gate behaves as if it had a stuck-at-one fault at either its input or output. An STP at the dynamic node also behaves as a stuck-at fault. If an STP occurs at the clock signal line, the domino gate cannot be precharged to V_{dd} during the precharge phase. Thus, it behaves like a stuck-at-one fault at the output of the domino gate. An STP at the drain node of the NMOS evaluation transistor or at the dynamic node can disable the dynamic node to discharge. Consequently, it behaves like a stuck-at-zero fault at the output of the domino gate.

An STP at one of the nodes in the NMOS evaluation network behaves like a stuck-at-zero fault at the gate node of the NMOS transistor whose drain node has the STP. For example, if there is an STP at the drain node of the MB transistor in Fig. 3, it behaves like a stuck-at-zero fault at node B.

A.3 STG

If an STG exists at the input or output node of a CMOS domino gate, it behaves like a stuck-at-zero fault at the input or output node of the domino gate. An STG at the gate or drain node of the PMOS precharge transistor in a CMOS domino gate causes the output of the domino gate to be stuck at zero in the evaluation phase. An STG at the dynamic node of a CMOS domino gate behaves like a stuck-at-one fault at the output of the domino gate. If an STG occurs at the gate node of the NMOS evaluation transistor, it prevents the dynamic node of the domino gate from discharging. Thus, it behaves as a stuck-at-zero fault at the output of the domino gate. An STG at the drain node of the NMOS evaluation transistor can only increase the power consumption of the domino gate. This STG cannot cause the domino gate to fail functionally.

An STG in the NMOS evaluation network can be detected by a vector for the stuck-at-one fault at the gate node of the NMOS transistor whose drain node has the STG.

A.4 SHI

Short between an input and a source node of any NMOS transistor in the evaluation network

If the NMOS transistor with the faulty input and the NMOS transistor with the faulty source node are in the same transistor stack, the short can be detected in the same way a gate-source short in any NMOS transistor in the evaluation network can be detected. This has been shown in Sec. A.1.

However, if the two defective NMOS transistors are not in the same transistor stack, as shown in Fig. A-2, there is no equivalent or dominant single stuck-at fault for the SHI. By applying the vector shown in Fig. A-2, we can discharge the charge on the dynamic node through MA and the SHI to ground. Consequently, the output node of a defective gate becomes V_{dd} and that of a defect-free gate remains at 0V. However, the vector for detecting this SHI is not a single stuck-at fault vector. The defect coverage of this SHI at different supply voltages is similar to that of a gate-drain short in MA of Fig. 3.

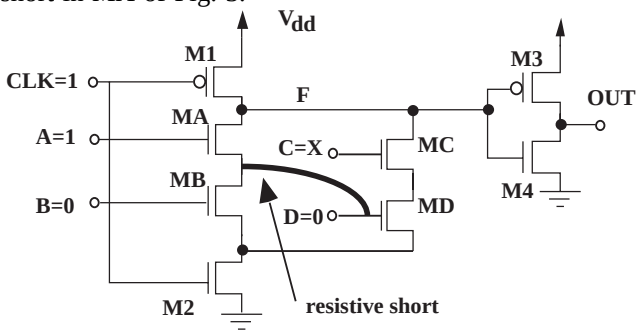

Figure A-2 An SHI

Short between the output and a source node of any NMOS transistor in the evaluation network

Figure A-3 shows an SHI between the output node of a CMOS domino gate and the source node of an NMOS transistor in the evaluation network. To detect the SHI, we can set the input of all the NMOS transistors between the dynamic node and the defective node to be 1 and the rest of the inputs to be 0. There is no fault effect during the precharge phase. During the evaluation phase, the charge at the dynamic node can discharge through MA, MB, and the short to the output node. Because the sizes of M3 and M4 are usually skewed so that the output node is very sensitive to the voltage level at the dynamic node, the output node of the defective domino gate rises quickly after that at the dynamic node falls. The output node cannot switch to its full-swing value and can only have a degraded signal instead. Nevertheless, the degraded signal can make the next domino gate switch erroneously. The defect coverage of the SHI at the nominal supply voltage is larger than 10 KΩ. Although the SHI can be detected by only one vector, the vector is not a single stuck-at fault vector.

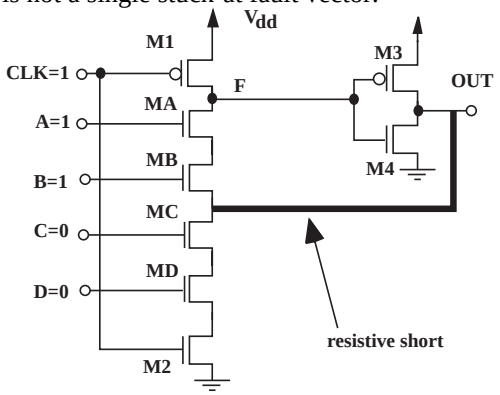

Figure A-3 An SHI

Input-output

An SHI between an input node and the output node of a CMOS domino gate turns the CMOS domino gate into a buffer to the defective input node. It can be detected by applying a vector that can distinguish between the function of a defective domino gate and that of a defect-free domino gate.

Short between the source nodes of two NMOS transistors in the evaluation network

An SHI between two nodes in the evaluation network of a CMOS domino gate changes the function of the defective domino gate. If the SHI connects two nodes in the same transistor stack, it behaves as a stuck-at-one fault at the gate node of any NMOS transistor between the short. For example, if there is a short between the source node of MA and the source node of MC in Fig. 3, the SHI behaves as a stuck-at-one fault at either B or C. If the SHI connects two nodes between two different transistor stacks, we can detect the short by applying the vector that distinguishes the Boolean function of the defective gate from that of a defect-free gate.

Clock signal-output

An SHI between the clock signal and the output node in a CMOS domino gate behaves as a stuck-at-one fault at the output node of the domino gate in the evaluation phase.

Clock signal-input

An SHI between the clock signal and any of the input node of a CMOS domino gate behaves as a stuck-at-one fault at the faulty input node during the evaluation phase.

Clock signal-drain node of any NMOS transistor in the evaluation network

An SHI between the clock signal and the drain of any NMOS transistor in the evaluation network behaves similar to an STP at the drain node of the defective NMOS transistor in the evaluation phase. Consequently, it behaves as a stuck-at-zero fault at the gate node of the defective NMOS transistor in the evaluation phase.

Clock signal-dynamic node, Output-dynamic node, Clock signal-drain node of the NMOS evaluation transistor

These SHIs behave similarly to other shorts that have been discussed in Sec. A.1.

Appendix B Inter-Gate Resistive Shorts

B.1 Defect Coverage at Different Temperatures

Figure 5 shows the simulated circuit. The simulation is based on the same 0.6 μm technology used in previous tests. All internal nodes were charged to the full-swing value during the precharge phase. In the evaluation phase, A, B, B1, and D1 were switched from 0 to 1. At the same time, C and D were held at 0. The resistive short was detected if OUTA and OUTC meet one of the following criteria:

A. OUTC changes from 0 to 1;

B. OUTA does not change from 0 to 1 or it changes ten times slower than expected.

We performed the same simulation at four temperatures, 0°C, 25°C, 75°C, and 125°C. Figure B-1 shows the defect coverage of the resistive short shown in Fig. 5 at different temperatures and at normal operating voltage 3.3V.

Figure B-1 shows that the defect coverage of the resistive short increases as the temperature increases when the supply voltage is held constant. For the simulated circuit, a short with resistance greater than 1.5 KΩ cannot be detected at room temperature (25°C). However, the defective CUT will fail at a higher operating temperature. Thus, the defective circuit can pass at room temperature but fail in the system when the operating temperature becomes higher than room temperature. This can make such a defective circuit fail intermittently or fail early in its lifetime.

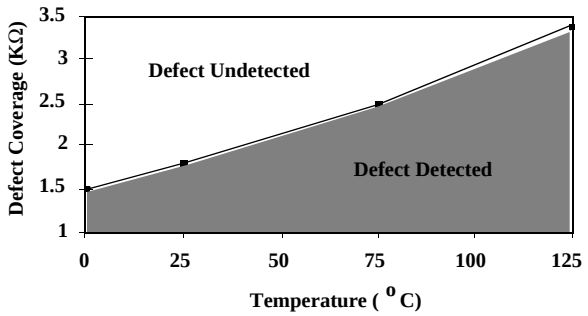

Figure B-1 Defect Coverage of the Short in Fig. 5 at Different Temperatures for V_{dd} = 3.3V

B.2 Defect Coverage at Different Voltages

The results in Fig. 6 are explained qualitatively below. At high voltage, the fault effect of the resistive short can be observed at OUTC in Fig. 5. Noise can couple from A1 through the resistive short to C1. If the coupled noise at C1 becomes larger than the threshold voltage of an NMOS transistor, it can cause G3 to switch. Thus, OUTC can switch from 0 to 1 unexpectedly. The magnitude of the coupled noise can be approximated by Equation B-1. V_n is the magnitude of the coupled noise. R_S is the resistance of the resistive short. R_M is the equivalent resistance of the pull-down transistor (M4 in Fig. 3) of G1. Since both inputs of G1 are zeros, R_M is almost a constant. V_{dd} is the supply voltage. Based on Equation B-1, the coupled noise is proportional to the supply voltage. Thus, the defect coverage improves when the supply voltage increases.

$$V_n = \frac{R_M}{R_s + R_M} \times V_{dd} \qquad \text{Equation B-1}$$

At very low voltage, the effect of the resistive short becomes severe because the equivalent resistance of a transistor increases significantly at very low voltage [5] [6]. A1 is pulled down by the pull-down transistor (M4 in Fig. 3) of G1 to be smaller than the threshold voltage of a transistor at very low voltage. Thus, G2 cannot switch or can only switch slowly. Consequently, we observe the fault effect at OUTA. Figure C-8 shows that the supply voltage should be as low as $2V_t$ to improve defect coverage significantly.

However, if the supply voltage is reduced from its normal operating value but not made as low as $2V_t$, the defect coverage becomes worse than it is at the normal operating voltage. When the supply voltage is in this range, the coupled noise at C1 is too small to turn on G3 and the weakened signal at A1 is still much larger than the threshold voltage of a transistor and thus cannot turn off G2.