Quantitative Analysis of Very-Low-Voltage Testing

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Abstract

Some weak static CMOS chips can be detected by testing them with a very low supply voltage -- between 2 and 2.5 times the threshold voltage V_t of the transistors. A weak chip is one that contains a flaw -- an imperfection that does not interfere with correct operation at rated conditions but which may cause intermittent or early-life failures. This paper considers several types of flaws and derives the test conditions for them. It also proposes two approaches for determining the appropriate test speed for very-low-voltage testing.

1. Introduction

Very-low-voltage (VLV) testing is an alternative to burn-in for detecting weak CMOS IC's [1]. Weak IC's contains *flaws* [1], defects that do not cause functional failures at normal operating conditions but degrade the IC's performance, reduce noise margins, or draw excess supply current. Hao and McCluskey showed that weak IC's cause problems with reliability and must be detected before they are shipped [1]. Although weak IC's may pass production tests, they can fail to work in the field at different operating conditions, thus causing intermittent failures. Furthermore, weak IC's may consume extra power if the defect causes an abnormal static current flow, which makes them unacceptable in low-power applications. However, the detectability of these defects depends on the test conditions. A general survey of various testing techniques for detecting weak CMOS IC's appears in [1].

Hao and McCluskey have investigated the voltage dependence of two major causes of weak IC's, resistive shorts and threshold voltage shifts, and proposed VLV testing [1]. Based on the difference of the electrical characteristics at different supply voltages, VLV testing can detect some defects that are undetectable at the normal supply voltage. The experimental results in [2] indicated that VLV testing detected some suspect dies that passed normal voltage tests and current tests. Not only can this technique be used for CMOS digital circuits, but Bruls also applied it to test a class AB amplifier developed in a 1.0μm double metal CMOS technology and a bipolar ring oscillator manufactured in a BiCMOS process [3].

This paper presents a methodology for determining the supply voltage and test speed for VLV testing. Defects were simulated in various static CMOS circuits. All simulations were done in HSPICE. Three technologies were used in these simulations. Most simulations were based on MOSIS HP CMOS26B 0.8μm technology. The normal operating voltage of this technology is 5V. Some simulations in Section 2 were based on MOSIS HP CMOS14TB 0.6 μm technology, whose normal operating voltage is 3.3V. A 0.26μm low-voltage technology, whose operating voltage can be as low as 1V to 1.5V, was also used to investigate the effectiveness of VLV testing for low-voltage technologies.

The supply voltage study investigates the tradeoffs among three items: the flaw coverage, test time, and noise margin. *Flaw coverage* is the detectable range of a defect, such as the detectable resistance of a resistive short. The flaws considered in this paper include gate oxide shorts and metal shorts. We have also investigated threshold voltage shifts and delay flaws. A circuit has a *delay flaw* if there is a timing failure but the circuit continues to work at the designed speed [4]. However, due to the page limitation of the paper, we will only discuss the results of gate oxide shorts and metal shorts. A subsequent paper will include the detailed analysis of threshold voltage shifts and delay flaws. Based on the results of a thorough analysis, we conclude that the supply voltage for VLV testing for these technologies should be set in the range of $2V_t$ to $2.5V_t$, where V_t is the threshold voltage of a MOS transistor.

The test speed for a certain supply voltage must be determined such that the test neither passes too many defective dies nor fails good dies. Researchers have shown that the delay-voltage scaling ratios of various CMOS gates are similar [5]. However, the interconnection delay remains almost the same at different supply voltages [6]. Also, because the threshold voltages of NMOS and PMOS transistors are sometimes different, the delays of the rising and falling transitions may scale differently. This paper proposes two methods to determine the test speed for VLV testing.

This paper is organized as follows. Section 2 describes tradeoffs in choosing the supply voltage for VLV testing. Section 3 discusses how the circuit speed varies when the supply voltage is reduced and proposes two approaches to find the test speed for VLV testing. Section 4 shows the effectiveness of VLV testing for low-voltage technologies. Section 5 concludes the paper.

2. Supply voltage selection

In this section, we will show that the supply voltage for VLV testing should be between 2 and 2.5 times the threshold voltage V_t of the transistors for the technologies used in this paper. This study investigates the tradeoffs among the flaw coverage, test time, and noise margin at various supply voltages. For other technologies, the same techniques should be used to obtain the appropriate value for supply voltage.

2.1 Flaw coverage

Researchers have shown that the resistance of a short may change with time and cause reliability problems for CMOS IC's [7] [8]. We consider two kinds of resistive shorts in this section, gate oxide shorts and metal shorts.

2.1.1 Gate oxide shorts. The analysis shown in this subsection is based on NMOS gate oxide shorts, which are unexpected connections between the gate and either the drain, source, or channel (substrate, p-well, n-well) in an NMOS transistor that are caused by pinholes in the gate oxide layer. We will also discuss the voltage dependency of PMOS gate oxide shorts at the end of this subsection.

Hao and McCluskey showed that NMOS gate oxide shorts can be modeled as resistive shorts [9]. Figure 1 shows a NAND gate with a gate-to-source short in the NMOS transistor M3. The input and output nodes of all the circuits used in this paper were buffered by inverters. Figure 2 shows the relationship between the resistance of a MOS transistor and the supply voltage for the 0.8μm technology. *The resistance of a MOS transistor* is measured as the voltage drop between the drain and source divided by the current flowing into the drain when a short exists within a transistor and the gate voltage of the transistor is set to a high voltage value. The supply voltage shown in Fig. 2 is scaled by the threshold voltage of an NMOS transistor. The transistor used in Fig. 2 is M3 of the NAND gate in Fig. 1. In Fig. 2, the resistance of the resistive short varies from 1KΩ to 5KΩ. Figure 3 shows the same information as Fig. 2, but for the 0.6μm technology.

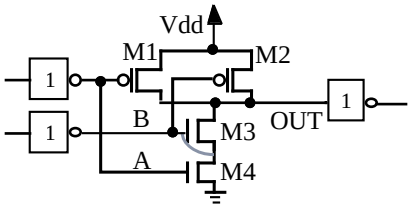

Figure 1 NMOS gate oxide short

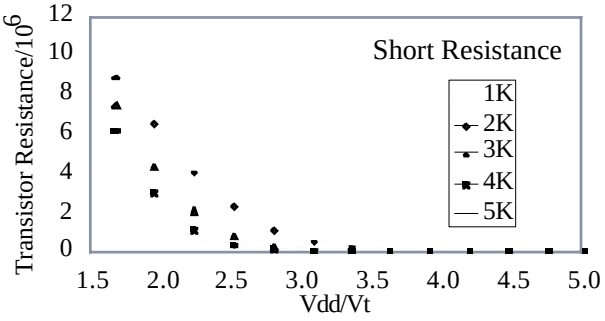

Figure 2 The equivalent resistance of an NMOS transistor for the 0.8μm technology

When there is an unexpected connection between gate and source (or drain) of a transistor, the gate voltage can be pulled down to a value lower than a normal supply voltage value. The transistor stays in either the saturation region or triode region. As a result, the resistance of a transistor increases as the supply voltage is reduced. Moreover, the gate voltage is smaller when the resistance of the short is smaller, which causes less current flowing through the transistor. Consequently, the resistance of a transistor is larger when the short resistance is smaller at the same voltage. On the other hand, the short resistance remains almost the same at different voltages. Based on the above observations, we can make a CMOS circuit with a gate oxide short fail to work and still keep a fault-free CMOS circuit functioning correctly at a reduced voltage [1] [3]. As shown in Fig. 2, a MOS transistor has a nonlinear resistance. The resistance of a MOS transistor increases monotonically as the supply voltage decreases. The improvement of the flaw coverage of the defect strongly depends on how much the resistance of a transistor increases at a reduced supply voltage. The more the resistance of a transistor increases, the more a resistive short affects the circuit-under-test. The result is that the electrical characteristics of a faulty gate change significantly at very low voltage. It is not necessary for the defect resistance of to be a constant. VLV testing can still detect a resistive short if the resistance of the short increases at a slower rate than the resistance of a transistor does as the supply voltage is reduced [1].

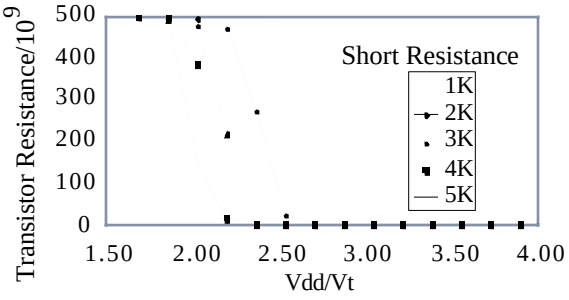

Figure 3 The equivalent resistance of an NMOS transistor for the 0.6μm technology

Figures 2 and 3 both show that the resistance of an NMOS transistor with the short resistance larger than 2KΩ starts to increase significantly when the supply voltage is approximately between $2V_t$ and $2.5V_t$. Hence, to detect a gate oxide short with a larger resistance, we must reduce the supply voltage until it is low enough to make the resistance of a transistor change significantly.

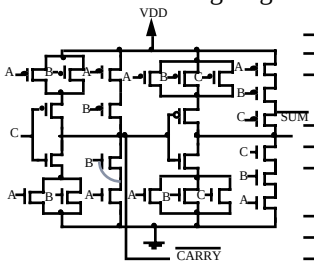

Figure 4 Static CMOS full adder

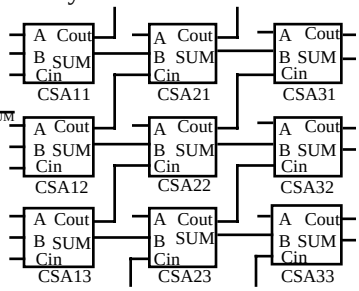

Figure 5 Simulation setup for the detectable resistance range of an NMOS gate oxide short

Simulations of a 3-stage carry save adder show how the detectable resistance of an NMOS gate oxide short changes as the supply voltage is reduced. The adder is a static

CMOS full adder [10], which is shown in Fig. 4. Figure 5 shows the circuit simulated. An NMOS gate-to-source short, as shown by a thick gray line in Fig. 4, was injected into CSA22. Table 1 lists the flaw coverages of the short for the circuits shown in Fig. 1 and 5 based on the 0.8μm technology. The results in Table 1 show that VLV testing is effective for both basic and complicated gates.

Hawkins and Soden proved that the resistance of a gate oxide short can be as high as 4.7KΩ [7]. To detect an NMOS gate oxide short with 5KΩ resistance, the supply voltage should be as low as 1.6V, which is $2.25V_{tn}$. Additionally, all possible NMOS gate-drain and gate-source shorts in the full adder cell of Fig. 4 were then exhaustively simulated. By setting the supply voltage to be 1.5V ($2.11V_{tn}$), all shorts with a resistance smaller than 5KΩ were detected by Boolean tests.

Table 1 The flaw coverage of an NMOS gate oxide short by Boolean tests (V_{tn}=0.7144V)

Supply Voltage		Flaw Coverage	
V_{dd}	V_{dd}/V_{tn}	NAND Gate in Figure 1	Adder Cells in Figure 5
1.4	1.97	≤ 10KΩ	≤ 8KΩ
1.6	2.25	≤ 6KΩ	≤ 5KΩ
1.8	2.53	≤ 5KΩ	≤ 3.5KΩ
2.0	2.81	≤ 4KΩ	≤ 2KΩ
3.0	4.22	≤ 2KΩ	≤ 1KΩ
5.0	7.03	≤ 1KΩ	≤ 0.5KΩ

Based on these results, we suggest that the supply voltage of VLV testing be $2V_t$ to $2.5V_t$ for NMOS gate oxide shorts. The supply voltage can be adjusted within this range to accommodate other considerations.

Turning to PMOS gate oxide shorts, their behavior is more complicated than that of NMOS gate oxide shorts because of the different doping polarities between the gate and either the drain, source or conducting channel [11] [12]. Hao and McCluskey have analyzed the voltage dependency of PMOS gate-drain and gate-source shorts, which were modeled by a diode in series with a resistor [12]. Depending on the saturation current of the diode in the model, the effects of the shorts can be either enhanced or reduced at low voltage.

We investigated the voltage dependency of a PMOS gate-channel short. The short was modeled as the circuit shown in Fig. 6, which was proposed by Syrzycki [11]. A PMOS gate-channel short was injected into the second inverter of the buffer chain shown in Fig. 7. Each inverter was sized to drive another inverter four times the size of its own. The gate width of the faulty PMOS transistor is 4μm. The simulation results indicate that the PMOS gate-channel short causes the output of the faulty inverter to be stuck-at 0 at 5V when R_{gos} is 0.1KΩ, where R_{gos} is the resistance shown in Fig. 6. Nonetheless, when R_{gos} increases to 5KΩ, the short can only increase the propagation delay of the faulty gate by 60% at the normal operating voltage, which makes the short unlikely to be detected if the faulty gate is in the short path (non-critical path). On the other hand, at 1.5V, which is in the suggested supply voltage range for resistive shorts, the simulation results show the gate delay of the faulty gate increases to be 2.88 times that of the fault-free gate. For an inverter with a larger W/L ratio, at low voltage the delay ratio between a faulty gate with a PMOS gate-channel short and a fault-free gate still increases, but not as significantly as a small inverter. On the other hand, Syrzycki showed that PMOS gate oxide shorts can increase the static current and be detected by a current test [11].

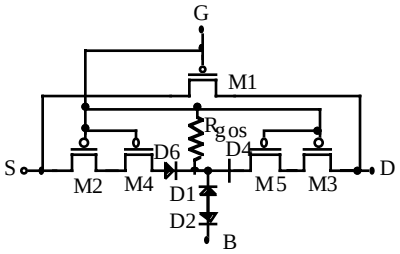

Figure 6 PMOS gate-channel short [11]

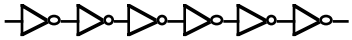

Figure 7 A CMOS buffer chain

Consequently, VLV testing can make the effect of a PMOS gate oxide short more severe in a small gate and when R_{gos} is large. The results in [2] showed that there were some test escapes for a very-low-voltage test but these dies were detected by a current test. On the other hand, the results in [2] also showed that there were some suspect dies that were only detected by VLV testing. This implies that VLV testing and I_{DDQ} testing do not target exactly the same defects.

2.1.2 Metal shorts. Metal shorts are unexpected metal connections between two nodes. In this subsection, we determine the supply voltage for VLV testing based on the improvement of the flaw coverage of a metal short at different voltages. Similar to gate oxide shorts, the supply voltage for VLV test should be set in the range that the equivalent resistance of a transistor increases significantly.

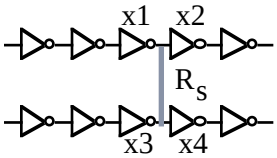

Fig. 8 A metal short

Figure 8 shows the simulation setup. The gray line that connects the outputs of gates x1 and x3 is a resistive short with resistance R_S. Two sets of simulations were done. For one set of simulations, the inverters in both inverter chains have the same size. For the other set of simulations, each inverter in the bottom inverter chain were sized to be four times bigger than the corresponding inverter in the upper inverter chain. Tables 2 and 3 show the simulation results. The results show that the flaw coverage of a metal short that connects two gates with different sizes is larger than one that connects two gates with the same size. We will only discuss the case that has a metal short connecting gates with different sizes because it occurs more often in reality.

The results show that the flaw coverage of a metal short improves to 5KΩ when the supply voltage is 1.6V for the 0.8µm technology, which is $2.25V_{tn}$, and is 1.3V for the 0.6µm technology, which is $2.20V_{tn}$. Researchers have shown that 98.3% of resistive shorts are below 5KΩ [13]. Consequently, the supply voltage for VLV testing should be in the range of $2V_t$ and $2.5V_t$, where V_t is the smaller between V_{tn} and $|V_{tp}|$.

Table 2 Flaw coverages of a metal short by Boolean tests (0.8µm technology, V_{tn} = 0.7144V, V_{tp} = - 0.9002V)

Supply Voltage			Flaw Coverage	
V_{dd}	V_{dd}/V_{tn}	$V_{dd}/\|V_{tp}\|$	Same Size	Different Size
1.4	1.97	1.56	≤ 6KΩ	≤ 6.5KΩ
1.6	2.25	1.78	≤ 4KΩ	≤ 5KΩ
1.8	2.53	2.00	≤ 2KΩ	≤ 3KΩ
2.0	2.81	2.22	≤ 1KΩ	≤ 2KΩ
3.0	3.51	2.78	≤ 0.5KΩ	≤ 1KΩ
5.0	7.03	5.55	≤ 0.5KΩ	≤ 0.5KΩ

Table 3 Flaw coverages of a metal short by Boolean tests (0.6µm technology, V_{tn} = 0.59V, V_{tp} = - 0.84V)

Supply Voltage			Flaw Coverage	
V_{dd}	V_{dd}/V_{tn}	$V_{dd}/\|V_{tp}\|$	Same Size	Different Size
1.2	2.03	1.43	≤ 6KΩ	≤ 6KΩ
1.3	2.20	1.55	≤ 4KΩ	≤ 5KΩ
1.4	2.37	1.67	≤ 2KΩ	≤ 2KΩ
1.6	2.71	1.90	≤ 1KΩ	≤ 1.5KΩ
2.0	3.39	2.38	≤ 0.5KΩ	≤ 1KΩ
3.3	5.59	3.93	≤ 0.5KΩ	≤ 0.5KΩ

2.2 Test time

The propagation delay of a CMOS gate becomes much longer at a reduced supply voltage. While reducing the supply voltage can improve the flaw coverage, it also increases the test time. As a result, the supply voltage should not be arbitrarily small.

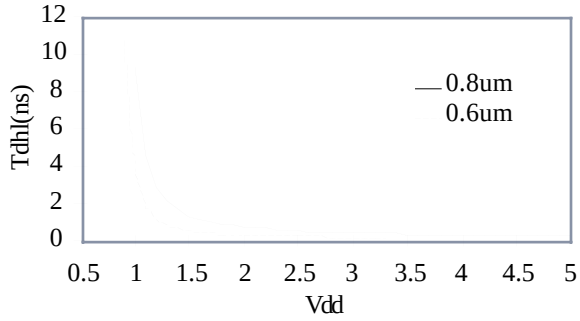

Figure 9 Propagation delay of a CMOS inverter

Although the propagation delay increases monotonically as the supply voltage is reduced, the propagation delay of a CMOS gate does not change very much for a wide range. Figure 9 shows the propagation delay of an inverter at different voltages for two different technologies. If the supply voltage is selected so that it is around the value where the propagation delay starts to change significantly, not only can we improve the flaw coverage, but we can also keep the test time cost as low as possible for VLV testing. Figure 9 show that the propagation delay of a CMOS inverter starts increasing significantly at around 1.5V for the 0.8µm technology, which is $2.11V_{tn}$, and 1.3V for the 0.6µm technology, which is $2.20V_{tn}$. As a result, the supply voltage proposed in the previous subsection is also valid as far as the test time is concerned.

2.3 Noise margins

Equations 1 and 2 show the noise margins of a CMOS inverter [10]. The strengths of the NMOS and PMOS transistors are assumed to be equal in these equations. The threshold voltages of an NMOS transistor and a PMOS transistor are assumed to be approximately the same.

$$NM_L = \frac{3V_{dd} - 3|V_{tp}| + 5V_{tn}}{8} \quad (1)$$

$$NM_H = \frac{3V_{dd} + 5|V_{tp}| - 3V_{tn}}{8} \quad (2)$$

Based on Equations 1 and 2, relative noise margins improve at low voltage because V_t / V_{dd} increases [16]. As discussed in [16], internal noise scales at least as fast as the supply voltage. For long channel devices, capacitive coupling noise scales as V_{dd}, resistive coupling noise scales as V^2_{dd}, and inductive coupling noise scales as V^3_{dd}. For short channel devices, capacitive, resistive, and inductive coupling noises all scale as V_{dd}. Relatively, internal coupling noise does not get worse at low voltage.

Unlike coupling noise, thermal noise does not scale at different voltages. Burr showed that the thermal noises are as small as 100µV [16]. Practically, thermal noise is not a concern when the supply voltage is above 1V.

However, the results of VLV testing are sensitive to external noise. Because absolute noise margins decrease at low voltage, the testing environment must be controlled so that external noises are isolated. The supply voltage must be larger than the magnitude of external noise.

2.4 The supply voltage for VLV testing

Based on previous discussions, the supply voltage for VLV testing should be set in the range of $2V_t$ to $2.5V_t$ for the technologies used in this paper, where V_t is the smaller of V_{tn} and $|V_{tp}|$. The supply voltage used in [2] for VLV testing is in the range proposed in this paper. In [2], the supply voltage was selected by doing a Shmoo plot on a good die. 1.7V was then chosen considering both noises and test time. The results published in [2] indicated that there were some dies that failed only VLV testing.

It is important to point out that, at the supply voltage for VLV testing, fault-free circuits should still be functional. At low voltage, the transistors in a stack will turn on in sequence. Due to the body effect, some transistors in high stacks can have higher threshold voltages. If the supply voltage is too low, some gates will have a very long propagation delay or may not switch at all. The circuits simulated in this paper have varieties of transistor stacking depth. The highest transistor stack has three transistors. All

fault-free circuits were verified to be functional within the proposed voltage range.

However, suppose a CMOS gate has unbalanced NMOS and PMOS transistor stacks. In this case, although the gate can be sized to have the same delays for rising and falling transitions at the normal operating voltage, they will be different at low voltage. For example, a 3-input NAND gate has three NMOS transistors in series and three PMOS transistors in parallel. As the supply voltage is reduced, the falling transition will slow down more seriously than the rising transition. Since the clock frequency is determined by the propagation delay of the slower transition at low voltage, the slack appearing in the path for the other transition will be larger. Consequently, for timing tests at low voltage, the flaws provoked by test signals propagating through the stacking transistors are more detectable than those provoked by test signals propagating through non-stacking transistors.

3. Determining the test speed

This section analyzes the delay-voltage relationship of a CMOS device and proposes some ways to determine the test speed of VLV testing.

3.1 Delay-voltage relationship analysis

The relationship between the test speed and supply voltage depends on how the critical path delay of a circuit changes as the supply voltage is changed. Some researchers have studied this relationship [5] [6]. Horowitz *et al.* showed that the delay-voltage relationship of a CMOS circuit is predictable. They used circuits of various sizes to show that CMOS circuits with the same process technology have similar speed-voltage scaling ratios. The maximum deviation is within 15%. The *delay-voltage scaling ratio* is the ratio between the propagation delay at any voltage and that at the normal operating voltage.

However, because the threshold voltages of NMOS and PMOS transistors are different for some technologies, the delays of rising and falling transitions may scale differently as the supply voltage decreases. To predict the circuit speed at different voltages more accurately, the delays of rising and falling transition should be scaled by different delay-voltage scaling ratios.

As the switching speed of an integrated circuit increases, the interconnection delay becomes important. Wagner and McCluskey showed that, unlike the gate delay, the interconnection delay of an integrated circuit is independent of the supply voltage [6]. Because of the difference between the delay-voltage scaling ratios of the CMOS gate delays and the interconnection delays, the critical paths may be different at different supply voltages if there are other paths whose delays are shorter but similar to those of the critical paths at the normal operating voltage.

3.2 Proposed methods

The discussion in the previous subsection leads us to propose two different methods to set the test speed of each circuit-under-test at low voltage.

3.2.1 Constant scaling factor. A simple, efficient, but conservative way to determine the test speed at low voltage is to use the pre-characterized delay-voltage scaling ratio of a CMOS basic gate, such as an inverter, to calculate the test speed at each supply voltage with Equation 3.

$$T_d = (ar_{lh} + (1-a)r_{hl})T_{do}(1+e) \quad (3)$$

T_d is the critical path delay at any voltage. T_{do} is the critical path delay at the normal operating voltage. a is the proportion of the critical path delay that is due to rising transitions. r_{lh} is the delay-voltage scaling ratio of a rising transition of a CMOS gate. r_{hl} is the delay-voltage scaling ratio of a falling transition of a CMOS gate. e is the error control bound. The *error control bound* is the extra delay added to the calculated speed to overcome the variation of normalized speeds in different circuits, including the variation due to stacking transistors.

Since the delay-voltage scaling ratio of the interconnection delay is replaced by that of a CMOS gate delay, the test speed determined from this method guarantees that the test will not fail good circuits. Although the critical path may not be the same at low voltage, the test speed will be slower than any clock rates for possible new critical paths since the interconnection delay is scaled too.

This method can be applied to all Boolean tests. It can also be used for a timing test when the interconnection delay is insignificant in the circuit-under-test.

3.2.2 Critical paths at different supply voltages. Section 3.1 concludes that the interconnects and CMOS gates have different delay-voltage scaling ratios. As a result, the test speed determined by the previous subsection may not be the optimum test speed. Although using this test speed will not fail any good circuits, the test may miss some defects that cause timing failures. Thus, to improve the flaw coverage of timing failures, we need to analyze the circuit-under-test to find the new critical path and the test clock frequency at low voltage.

If there are n paths that have similar propagation delays to the critical path at the normal operating voltage, we can use Equations 4 and 5 to find the new critical path delays at different voltages.

$$T_{di} = ((a_i r_{lh} + (1-a_i)r_{hl})(1-k_i)T_{doi} + k_i T_{doi})(1+e) \quad (4)$$

$$T_d = \max(T_{di}, i = 0,\ldots,n) \quad (5)$$

T_{di} is the propagation delay of path i at a low voltage. T_{doi} is the propagation delay of path i at the normal operating voltage. k_i is the proportion of the delay in path i that is due to interconnections. a_i is the proportion of the delay in path i that is due to rising transitions. Other parameters have the same meanings as used in Equation 3.

4. VLV testing for low-voltage technologies

One of the trends in today's IC market is to reduce the supply voltage [16] [17]. The effectiveness of VLV testing is based on the observation that the difference of the electrical characteristics between a faulty circuit and a fault-

free circuit can be increased by reducing the supply voltage. It is shown that the difference is more significant as the supply voltage is closer to the threshold voltage of a MOS transistor. The discussion in Section 2 concludes that the supply voltage for VLV testing should be in the range of $2V_t$ to $2.5V_t$. For high performance CMOS designs, the threshold voltage is reduced so that the designs will not have severe speed degradation [15] [17]. Mii *et al.* showed that there will be excessive delays if $V_t > V_{dd}/4$.

We studied VLV testing for a low-voltage technology, whose normal operating voltage is 1V to 1.5V. The technology has two different processes. One has a normal threshold voltage, around 0.5V. The other one has an ultra-low threshold voltage, around 0.25V. By setting the supply voltage at $2V_t$, the flaw coverages of the defects shown in Fig. 1 and 8 can be summarized in Table 4. For an AC test, we assume that a short is detectable if the propagation delay of a defective gate is more than three times that of a defect-free gate. The static current of an inverter is 0.789nA for the process with a normal threshold voltage and 0.93μA for the process with a low threshold voltage. Consequently, the background current level is too high for a current test.

Table 4 The flaw coverage of the shorts in Figure 1 and 8 for a low-voltage technology when $V_{dd}=2V_t$

	Short in Fig. 1		Short in Fig. 8	
Technology	DC Test	AC Test	DC Test	AC Test
Low V_t	≤ 1.2KΩ	≤ 1.6KΩ	≤ 1KΩ	≤ 1.5KΩ
Normal V_t	≤ 1.6KΩ	≤ 2.6KΩ	≤ 1KΩ	≤ 1.5KΩ

5. Summary

We have shown that the supply voltage for VLV testing should be in the range of $2V_t$ to $2.5V_t$ for the technologies used in this paper. The supply voltage can be adjusted within this range to accommodate practical considerations, such as the magnitude of the external noise around the test environment. Two methods were proposed in this paper to determine the test speed for VLV testing. We also investigated the effectiveness of VLV testing for low-voltage technologies. By using $2V_t$ as the supply voltage during testing, we found reasonable defect coverage for gate oxide shorts and metal shorts. The static current for the low-voltage technology used in this paper is too high to perform a current test.

In conclusion, VLV testing is effective for detecting flaws that cause early life failures and intermittent failures. It does not add to the cost of an IC in either area or performance. Furthermore, it is non-destructive to a circuit-under-test and does not require a waiting time such as is typical for burn-in. The methodology presented in this paper for deciding the supply voltage and test speed for VLV testing can be applied to other technologies.

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