SHOrt Voltage Elevation (SHOVE) Test for Weak CMOS ICs

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ABSTRACT

A stress procedure for reliability screening, SHOrt Voltage Elevation (SHOVE) test, is analyzed here. During SHOVE, test vectors are run at higher-than-normal supply voltage for a short period. Functional tests and IDDQ tests are then performed at the normal voltage. This procedure is effective in screening oxide thinning, which occurs when the oxide thickness of a transistor is less than expected, as well as via defects. The stress voltage of SHOVE testing should be set such that the electric field across an oxide is approximately 6MV/cm. The stress time can be calculated by using the "effective oxide thinning" model. We will also discuss the requirements on input vectors for stressing complementary CMOS logic gates and CMOS domino logic gates efficiently.

1. Introduction

SHOVE testing aims at screening early-life failures and intermittent failures so that we can improve the quality level of CMOS ICs at low cost. In conjunction with other testing techniques, such as IDDQ testing [1] and Very-Low-Voltage (VLV) Testing [2] [3] [4], we can ensure CMOS IC quality without performing burn-in. During SHOVE, test sets, such as single stuck-at or pseudo stuck-at test sets, are run at higher-than-normal supply voltage for a short period. After SHOVE, some defects can only be detected by functional tests and some can only be detected by IDDQ tests. Thus, functional tests and IDDQ tests should be performed at normal operating voltage after SHOVE. Figure 1 shows the procedure for SHOVE testing. It has been found that IDDQ values of some circuits-under-test (CUTs) increase significantly after SHOVE [5] [6]. SHOVE testing is useful at wafer sort. It can screen out weak parts during a wafer-level test and avoid the cost of packaging them. This procedure has been widely practiced in industry [5] [7]. Some data which showed the correlation between the effectiveness of burn-in and SHOVE testing were reported recently [8] [9]. However, no detailed analysis has been found in any published literature. This paper will provide a theoretical study of SHOVE testing.

Although burn-in can provoke various defects and improve the reliability of CMOS ICs [10], it increases the production cost and lengthens the test time. IDDQ testing can detect weak parts, which are ICs with low mean-time-to-failure (MTTF) [11], by measuring their quiescent currents. On the other hand, VLV testing can make weak parts fail functional tests at very low voltage. Both IDDQ testing and VLV testing do not change the characteristics of a CUT. Unlike IDDQ testing and VLV testing, SHOVE testing detects weak parts by changing their characteristics.

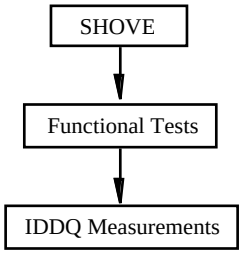

Figure 1 SHOVE testing procedure

Oxide defects are one of the major causes of reliability problems for CMOS ICs [10]. Particulate contamination, crystalline defects in the substrate, spot defects, localized thin regions, or surface roughness can cause localized weak spots in an oxide [12] [13]. Moreover, the quality and lifetime of a gate oxide strongly depend on its thickness [13]. *Oxide thinning* occurs when the oxide thickness of a transistor is physically or effectively thinner than expected. Oxide thinning can be due to localized thin spots, traps in the oxide, surface asperity, or locally reduced tunneling barrier height [14]. It can shorten the lifetime of a gate oxide, increase oxide leakage current, or cause time-dependent dielectric breakdown. As a result, it can cause early-life failures and must be detected. It is found that oxide thinning can cause stress-induced oxide leakage or become a gate oxide short after SHOVE and thus increase the IDDQ values of the defective CUT.

SHOVE can also make some via defects become opens, which can then be detected by either IDDQ measurements or functional tests depending on the characteristics of the resulting opens [8] [9]. SHOVE, however, is less effective in stressing electromigration. Instead of using SHOVE tests, temperature stress is more effective for stressing metalization because electromigration has high temperature activation energy [10]. On the other hand, temperature stress has less effect on oxide defects because of their low temperature activation energy [10].

To stress defective oxides effectively and still avoid damaging flawless oxides or causing latchup, the electric field across the oxides, E_{OX}, must be carefully controlled. Fowler-Nordheim tunneling currents may occur across flawless oxides if E_{OX} is larger than a critical value. The excess tunneling currents flowing through gate oxides can

damage the oxides. The damage can cause increased oxide leakage currents even after the supply voltage is reduced to the normal operating voltage. A *critical* E_{OX} is the maximum E_{OX} that does not cause large tunneling current across an oxide. Based on various published measurement data, the critical E_{OX} is approximately 6MV/cm [15] [16] [17] [18] [19]. E_{OX} at the normal operating voltage for different technologies is always well below this value [20] [21] [22] [23]. By applying the critical E_{OX} across the flawless oxide during SHOVE, we can maximize the stress effects on the defective oxides, minimize the stress time, and avoid damaging flawless oxides.

In a CMOS IC, each transistor must be stressed for enough time during SHOVE. To effectively stress an NMOS transistor, the gate of the transistor should be held at the stress voltage and the drain and source of the transistor at 0V. Similarly, to effectively stress a PMOS transistor, the gate of the transistor should be held at 0V and the drain and source of the transistor at the stress voltage. Both single stuck-at and pseudo stuck-at test sets can be the stress vectors for SHOVE testing for fully complementary static CMOS logic. We also investigate the toggle probability of various test sets in a CUT. For pseudo stuck-at test sets, some nodes were in logical one or zero for one or two vectors only. Thus, each vector must be held for at least the stress time for a transistor to make sure all transistors in a CMOS IC are stressed for enough time. We also discuss the stress vectors for domino-type dynamic logic. The stress speed should be the reciprocal of the stress time for a transistor in this case. The stress time of a transistor is the time to effectively stress an oxide.

This paper is organized as follows. Section 2 examines the behavior of oxide thinning and via defects during and after SHOVE. Section 3 discusses the stress voltage. Section 4 investigates the stress vectors. Section 5 analyzes the stress time and stress speed. Section 6 concludes this paper.

2. Oxide Thinning And Via Defects

SHOVE testing can increase the leakage current or cause oxide breakdown in a defective oxide whose thickness is less than expected. Oxide thinning shortens the lifetime of an oxide. As the oxide thickness is decreased in advanced technologies [21] [22] [23] [24], oxide thinning becomes a more serious problem. Furthermore, as the number of metal layers increases in most advanced technologies, via defects are more likely to occur. SHOVE testing can make some via defects become opens.

Several models have been proposed to predict the lifetime of an oxide and the onset criteria of oxide breakdown. Lee *et al.* proposed using "effective oxide thinning" to characterize time-dependent-dielectric-breakdown [13]. Sune *et al.* proposed a statistical description of oxide breakdown based on neutral trap generation in the oxide during wearout [25]. Dumin *et al.* found out that breakdown occurred locally when the local density of traps exceeded a critical value and the product of the electric field and the higher leakage currents through the traps exceeded a critical energy density [17]. We use the "effective oxide thinning" model to estimate the lifetime of an oxide in this paper because this model shows the relationship among the voltage across an oxide, effective oxide thickness, and oxide lifetime more directly than other models. Equation 1 shows the relationship among these parameters. X_{eff} is the effective oxide thickness, V_{OX} is the voltage across the oxide, t_{BD} is the time-to-breakdown of the oxide, τ_0 is determined by the intrinsic breakdown time under an applied voltage of V_{OX}, and G is the slope of $\log(t_{BD})$ versus $1 / E_{OX}$.

$$t_{BD} = \tau_0 \exp(\frac{GX_{eff}}{V_{ox}}) \quad (1)$$

Figure 2 shows the lifetime of a defective oxide at different voltages for three different technologies. The oxide thickness of the 2V technology is 6.5nm, that of the 3.3V technology is 9nm, and that of the 5V technology is 15nm. The thickness of the defective oxide is assumed to be 40% that of a flawless oxide. Because of the exponential relationship between the oxide lifetime and oxide thickness, the lifetime of an oxide starts decreasing significantly when its thickness is more than 50% thinner than that of a flawless oxide. We assumed that the voltage across the oxide is approximately the same as the supply voltage. t_{BD} was calculated by using Equation 1. G is 350 MV/cm and τ_0 is 10 picoseconds [13].

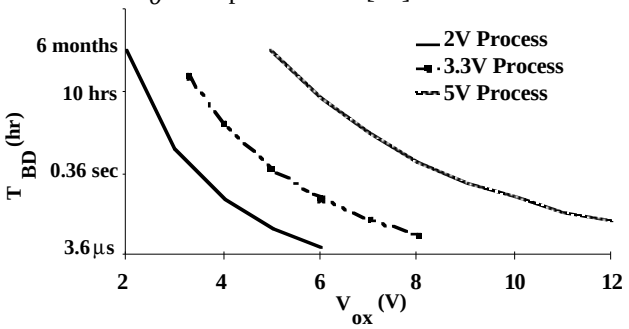

Figure 2 Lifetime of defective oxides for three different technologies

Figure 2 shows that the lifetime of a defective oxide decreases significantly as the supply voltage is increased. Moreover, the amount of supply voltage increment is relative to the normal operating voltage for each technology. The stress time at high voltage is much shorter than that at normal voltage. Due to the short stress time, the damage in a flawless oxide is negligible.

The poly gate and channel region of a MOS transistor are highly doped. The energy barrier width is very thin at the defective site. Consequently, tunneling current occurs at the thin spot when an electric field is applied across the oxide. The magnitude of the tunneling current increases significantly as the supply voltage increases over its

normal value [15] [16] [29]. Large tunneling currents can cause damage in an oxide layer and thus increase oxide leakage current. The failure mechanisms that cause the stress-induced oxide leakage can be localized defects [30], localized positive charges [31], or trap states near the injecting surface [15] [27]. These mechanisms further make X_{eff} in Equation 1 smaller and thus shorten the lifetime of an oxide. If the oxide thickness at the defect spot is very thin or the CUT is stressed for enough time, oxide breakdown may occur. Both stress-induced oxide leakage and oxide breakdown can significantly increase the quiescent current of a defective CUT.

Via defects can cause high leakage, timing failure, or functional failure depending on the failure modes [10]. Missing vias between two metal layers can cause functional failure. On the other hand, via undercut can cause a short circuit between two metal layers and thus increase the leakage. The short can also cause timing or functional failure depending on the resistance of the short.

The transient current during SHOVE can make some via defects become opens and thus cause functional failure or leakage. These via defects have high resistance before becoming opens. These defects increase the propagation delay of the signals passing through the vias. They can cause intermittent failure or early-life failure. Therefore, they need to be detected to ensure IC quality. Because the open vias after SHOVE may either cause functional failure or high leakage, both IDDQ tests and functional tests should be performed after SHOVE to be able to catch these defects.

SHOVE could burn off unexpected shorts between two metal layers and heal the CUTs if the shorts are thin wires or spot defects. These shorts have high resistance. Thus, it is more likely that the heat generated by the transient or static current across the shorts during SHOVE can burn off the shorts.

We only consider the characteristics of an oxide to determine the parameters for SHOVE tests because the lifetime of an oxide is more sensitive to voltage than that of a via.

3. Stress Voltage

The stress voltage should be set such that it will only cause damage in the defective CUTs and avoid damaging flawless CUTs. Because the damage to an oxide at high voltage is mainly due to the tunneling current flowing through the oxide, the stress voltage should be selected so that the oxide tunneling current is very small in a flawless oxide but large in a defective oxide. Two types of tunneling mechanisms, Fowler-Nordheim tunneling and direct tunneling, can appear across an oxide. For most 3.3V and 5V technologies, the oxide thickness of a MOS transistor is larger than 6nm [20] [21] [22] [23]. Moreover, direct tunneling currents exist in a thin SiO_2 film whose thickness is less than 6nm [32]. Consequently, Fowler-Nordheim tunneling currents dominates in the flawless oxide at high voltages for most 3.3V and 5V technologies. We will determine the stress voltage based on the behavior of Fowler-Nordheim tunneling current.

The magnitude of Fowler-Nordheim tunneling current strongly depends on E_{ox} [32]. Based on various published measurement data, the magnitude of the Fowler-Nordheim tunneling current across an oxide becomes significant when E_{ox} is larger than 6MV/cm [15] [16] [17] [18] [19]. Figure 3 shows the qualitative relationship between the Fowler-Nordheim tunneling current and E_{ox}. If the stress voltage is selected so that E_{ox} is approximately 6MV/cm in a flawless oxide, the tunneling current can flow through the defective site and increase the trap density at the thin spot during SHOVE. Table 1 shows the lifetime of a flawless oxide for the 3.3V technology used in Fig. 1 based on Equation 1. The lifetime of an oxide decreases significantly when the oxide is constantly stressed by an electric field stronger than 6 MV/cm. On the other hand, a slight increment in E_{ox} does not change the lifetime of an oxide significantly. Moreover, due to the short stress time, SHOVE testing can have little effect on the oxide quality of a defect-free CUT. Table 2 lists E_{ox} at normal operating voltages for several technologies. For these technologies, E_{ox} at the normal operating voltage is well below 6MV/cm. In Table 2, V_{dd} is the supply voltage and X_{ox} is the oxide thickness.

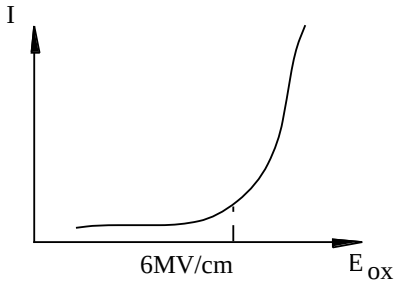

Figure 3 Fowler-Nordheim tunneling current vs. E_{ox}

Table 1 Lifetime of a flawless oxide for a 3.3V technology

V_{ox}	E_{ox}(MV/cm)	t_{BD}
3.3	3.67	9×10^{22} yrs
4.0	4.44	5×10^{15} yrs
5.0	5.56	7×10^{8} yrs
6.0	6.67	20,000 yrs
7.0	7.78	11 yrs
8.0	8.89	14 days

Based on Equation 1, the higher the stress voltage, the shorter the stress time required. The stress voltage should be selected so that it can maximize the effect of the stress on the oxide layers of CUTs, shorten the stress time, and still avoid damaging flawless oxides. The stress time can be reduced significantly by using the maximum allowed voltage during SHOVE.

Consequently, depending on the oxide thickness of a technology, the stress voltage for SHOVE testing can be

determined. Equation 2 shows the maximum stress voltage for SHOVE testing. The unit of X_{ox} is nm.

Table 2 Maximum E_{ox} at normal operating voltages

Technologies	V_{dd} (V)	X_{ox}(nm)	E_{ox}(MV/cm)
[20]	5	15	3.33
[21]	3.3	8.5	3.88
[22]	2.5	7	3.57
[23]	2	6.5	3.08

$$V_{stress} = T_{ox} \times 0.6V / nm \quad (2)$$

4. Stress Vectors

To thoroughly stress all the transistors in a CMOS IC and avoid long stress time, stress vectors must be selected so that the voltage across the oxide layer of a transistor is maximized. For an NMOS transistor, its source, drain, and substrate should be held at 0V, at the same time, the gate of the transistor should be held at the stress voltage. For a PMOS transistor, its source, drain, and substrate should be held at the stress voltage and the gate of the transistor be held at 0V. Consequently, to effectively stress an NMOS transistor in a fully complementary CMOS logic gate, the stress vector should connect the logic gate output and ground through the pull-down path that contains the target NMOS transistor. Similarly, to effectively stress a PMOS transistor in a fully complementary CMOS logic gate, the stress vector should connect the logic gate output and the supply voltage through the pull-up path that contains the target PMOS transistor.

To provoke a stuck-at-1 fault at the input of a complementary CMOS logic gate and propagate the fault effect to the output of the logic gate, the stuck-at vector will place a logical 0 at the gate of a PMOS transistor whose gate is connected to the faulty input node. In this way, the vector connects the output of the logic gate to the supply voltage through the PMOS transistor whose input gate is connected to the faulty input node. Thus, the PMOS transistor is put into the stress condition described in the previous paragraph. To provoke a stuck-at-0 fault at the input of a complementary CMOS logic gate and propagate the fault effect to the output of the logic gate, the stuck-at vector will place a logical 1 at the gate of an NMOS transistor whose gate is connected to the faulty input node. Similar to the vector for a stuck-at-1 fault at the input of the logic gate, the vector connects the output of the logic gate to ground through the NMOS transistor whose gate is connected to the faulty input node. As a result, the NMOS transistor is put into the stress condition mentioned in the previous paragraph. Moreover, a 100% single stuck-at test of a complementary CMOS logic gate can toggle all input nodes of the logic gate. Thus, a 100% stuck-at test set for a complementary CMOS logic gate can put each transistor in the required stress condition at least once. Thus, both 100% single stuck-at test sets and pseudo stuck-at test sets can be used as the stress vectors for SHOVE. The latter are more suitable than the former because of their shorter test lengths. On the other hand, IDDQ test sets that target inter-gate bridging faults are not suitable for SHOVE testing. Figure 4 shows a fully complementary CMOS gate. Table 3 shows how transistors are stressed by stress vectors. The four italicized rows constitute a 100% stuck-at test set. All transistors are stressed by this stuck-at test set.

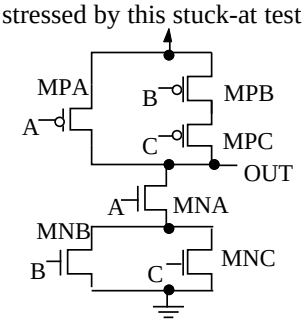

Figure 4 Fully complementary CMOS logic gate

Table 3 Stress vectors and the stressed transistors for a fully complementary CMOS logic gate

A	B	C	MPA	MPB	MPC	MNA	MNB	MNC
0	0	0	X*	X	X			
0	0	1	X					X
0	1	0	X				X	
0	***1***	***1***	***X***				***X***	***X***
1	***0***	***0***		***X***	***X***			
1	***0***	***1***				***X***		***X***
1	***1***	***0***				***X***	***X***	
1	1	1				X	X	X

* the transistor is stressed when the vector is applied

Table 3 shows that all-zero vectors can stress all PMOS transistors and all-one vectors can stress all NMOS transistors at once for the circuit shown in Fig. 4. To stress all transistors evenly and reduce the stress time for fully complementary CMOS logic gates, all-one and all-zero vectors can perform better than stuck-at test sets as the stress vectors.

We can modify the algorithm for line justification used in existing ATPG programs to generate all-zero and all-one vectors. To justify the output value of a logic gate, the inputs of the logic gate should be set to either all ones or zeros. For example, if we want to set the output of a 2-input OR gate to be logical one, we should put logical ones on both inputs of the gate. In existing ATPG programs, only one of the two inputs is set to logical one. The signal needs not to be propagated to a primary output. However, justification is more complicated than existing ATPG programs and may be impossible due to the structure of a CUT.

For CMOS domino logic, an all-one vector is sufficient to put all transistors in a domino logic gate in the stress condition if a signal and its complement do not appear at the inputs of the same logic gate. Otherwise, a test set that detects all stuck-at-0 faults at the logic gate

inputs can put all transistors in the stress condition at least once. Figure 5 shows a CMOS domino logic gate. Keepers can be put at proper internal nodes to ensure enough noise margin and avoid charge sharing problems [33]. To simplify the discussion, the keepers do not appear in the domino logic gate we use in this paper. However, the conclusion can be extended to the domino logic gate which has keepers implemented.

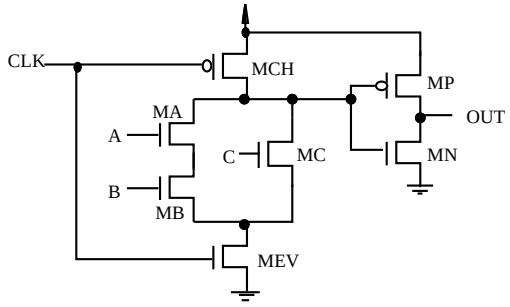

Figure 5 CMOS domino logic

During the precharge phase, the precharge PMOS transistor (transistor MCH) and the NMOS transistor in the output inverter of a domino logic gate (transistor MN) are stressed. During the evaluation phase, if all the inputs are logic one, all transistors in the evaluation branches (transistor MA, MB, MC, and MEV) and the PMOS transistor in the output inverter of a domino logic gate (transistor MP) are in the stress condition. If the inputs of a domino logic gate cannot be all ones at the same time, we can put each transistor in the stress condition at least once by discharging each evaluation branch individually. For the logic gate shown in Fig. 5, setting ABC to be 110 can discharge the evaluation branch containing transistor MA and MB. This pattern, which detects stuck-at-0 faults at input A and B, can stress transistor MA, MB, MEV, and MP. Also, setting ABC to be 001 can discharge the evaluation branch containing transistor C. This pattern, which can detect stuck-at-0 fault at input C, can stress transistor MC, MEV, and MP. Table 4 lists the stress vectors for CMOS domino logic.

Table 4 Stress vectors for CMOS domino logic

Input Condition	MCH	MEV	MP	MN	MA	MB	MC
Precharge	X*			X			
Evaluation (ABC = 111)		X	X		X	X	X
Evaluation (ABC = 110)		X	X		X	X	
Evaluation (ABC = 001)		X	X				X

* the transistor is stressed during the described input condition

5. Stress Time And Stress Speed

Each transistor in a CMOS IC must be stressed long enough to make sure the defective oxide deteriorates significantly so that either oxide breakdown or stress-induced oxide leakage occurs in the defective oxide. To optimize the stress effect of each stress vector and thus reduce the total stress time, each signal should be held at its full-swing signal level for enough time. In this way, transistors can be in the condition mentioned in Sec. 4 and thus be stressed efficiently by the stress vectors.

If a transistor can be stressed more than once during SHOVE by different stress vectors, we can reduce the overall stress time for a CMOS IC. Equation 3 shows the stress time of a CMOS IC. In Equation 3, T_{sl} is the overall stress time of a CMOS IC, n is the number of stress vectors, T_{st} is the stress time for each transistor at the applied stress voltage, and m is the minimum number of vectors that stress a transistor for all transistors in the CUT. T_{st} can be calculated by using Equation 1.

$$T_{sl} = n \times T_{st} / m \qquad (3)$$

To determine an appropriate value for m, we investigated a CUT which was used in an experiment [34]. The CUT was implemented by using only elementary CMOS logic gates. It has 380 gates, 24 inputs, 12 outputs, and 283 internal nodes. Seven 100% single stuck-at test sets and two pseudo stuck-at test sets were used in this study. We simulated all test sets and recorded how each node toggled.

For each of the two pseudo stuck-at test sets, there was at least one node that was in the logic zero state only once after we ran through all test vectors. Thus, m should be 1 for these two test sets. The stress speed for this CUT should be the reciprocal of the stress time for a transistor if pseudo stuck-at test sets are used. For 5 out of the 7 100% single stuck-at test sets, each node was in logic zero or logic one state at least twice among all test vectors. As a result, m can be set at 2 for these test sets. Nevertheless, 97% of the nodes were in logic zero or logic one more than 4 times among all vectors in all 7 100% single stuck-at test sets. Although some of the transistors may be set in the stress condition for most stress vectors, the overall stress time is still very short due to the short stress time applied for each vector. For one of the pseudo stuck-at test set, the test set length is 27. Based on the parameters referenced in this paper, if the stress voltage is 10V for a 5V technology, T_{st} is 0.01 sec for screening defective oxides whose thickness is thinner by 60%. On the other hand, the lifetime of a flawless transistor is 1.75×10^8 years if it is constantly operated at 10V. The overall stress time is still less than a second, which can hardly overstress any transistor.

6. Conclusion

SHOVE testing, VLV testing, IDDQ testing, and burn-in all aim at improving the quality level of CMOS ICs. We have shown that SHOVE testing can detect weak CMOS ICs caused by oxide defects and via defects. SHOVE testing requires shorter test time than burn-in and

does not need extra instruments. Consequently, SHOVE testing is an alternative to burn-in and can be used with VLV testing and IDDQ testing to improve the quality level of CMOS ICs and reduce the production cost.

Acknowledgments

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