Experimental Results for IDDQ and VLV Testing

Jonathan T.-Y. Chang[*], *Chao-Wen Tseng*[*], *Yi-Chin Chu*[*], *Sanjay Wattal*[*], *Mike Purtell*[**], *and Edward J. McCluskey*[*]

[*]Center for Reliable Computing
Stanford University
Gates Hall 2A
Stanford, CA 94305

[**]Advantest America R&D Center, Inc.
3201 Scott Boulevard
Santa Clara, CA 95054

Abstract

An experimental test chip was designed and manufactured to evaluate different test techniques. Based on the results presented in the wafer probe, 309 out of 5491 dies that passed the Stage 1 tests were packaged for further investigation. This paper describes the experimental setup and the preliminary results for the final package test. We focus on the correlation among various defect classes, including IDDQ failures, Very-Low-Voltage (VLV) failures, timing-independent combinational (TIC) defects, and non-TIC defects. We used 2 supply voltages for VLV tests. Two test speeds were used at each supply voltage. 9 dies failed only the VLV Boolean tests, and 7 of these were confirmed to have had high IDDQ measurement results. We also investigated the defect classes of the test escapes for 100% single stuck fault (SSF), transition fault, and IDDQ test sets.

1. Introduction

This paper is part of a series that reported experimental results from a test chip [1] [2] [3] [4]. The design of the experiment and architecture of the test chip were described in ITC'95 [2]. Preliminary results based on only one clocking mode were also reported in ITC'95 [3]. In ITC'96, we reported the results on timing-dependent defects and also the defect population in each defect class [4]. Based on the results in [3] and [4], we selected 309 dies for further investigation. These dies were assembled in 120-pin ceramic pin grid array packages and tested with an Advantest T6671E VLSI Test System. The Advantest T6671E VLSI Test System has a clock rate of 125MHz and a base data rate of 125/250MHz. The objectives of the final package test are as follows:

1. *Collecting accurate IDDQ measurements.*
2. *Characterizing VLV only failures.*
3. *Investigating pattern-dependent failures.*
4. *Characterizing timing-dependent failures.*
5. *Investigating repeatability of the wafer probe results.*

In this paper, we report the preliminary results from the final package test and discuss the correlation among IDDQ failures, VLV-only failures, timing-independent combinational (TIC) defects, and non-TIC defects. A die is classified as having *IDDQ failures* if its maximum IDDQ measurement exceeded a current limit. A die is classified as having *VLV-only failures* if it passed all the sampling (Boolean) tests at the nominal supply voltage but failed some sampling tests at very low voltage. The behavior of a *combinational defect* only depends on the input pattern applied and does not depend on previous patterns. The behavior of a *timing-independent defect* does not depend on the clock speed (less than or equal to the rated speed) at the nominal operating voltage. A *timing-independent combinational (TIC) defect* has both properties of a combinational defect and a timing-independent defect [4]. A defect that is either timing-dependent or pattern-dependent (non-combinational) is classified as a *non-TIC defect*. If the failure counts of a TIC defect matched those of a SSF, it is classified as a *SSF TIC defect*. Otherwise, it is a *non-SSF TIC defect*.

We also investigated the defect classes detected by 100% SSF, transition fault, and IDDQ test sets. Maxwell *et al.* have shown the relative performance of several tests [5]. Powell *et al.* have analyzed some experimental data to correlate defects to functional and IDDQ tests [6]. In ITC'96, we only showed the statistics of defect classes [4]. In this paper, we identify the defect class of each die detected by the selected tests in the example.

The test chip uses the LSI Logic LFT150K FasTest array series. The nominal supply voltage is 5V and the effective channel length is 0.7µm. It is a 25k gate CMOS gate array with 64 input pins, and 32 output pins. There are 5 circuits-under-test (CUTs) on the test chip. Two CUTs are datapath logic, MUL and SQR. The other three are control logic, STD, ELM, and ROB. The three control logic CUTs perform the same function but are implemented in different ways [1] [2]. The 5 CUTs occupy approximately 50% of the chip area. The rest of the chip is occupied by test support circuitry.

We tested the CUTs at four test speeds at the nominal supply voltage. Besides the three test speeds used in the previous probe [2], we added a test speed that is at least 3 times slower than the rated test speed. We also tested the CUTs at three different supply voltages: 5V, 2.5V, and 1.7V. When testing at 2.5V and 1.7V, two test speeds were used at each voltage. One test speed is based on the shmoo plot results. The other one is at least two times slower than the former one. For two-pattern tests, the cycle time for the first vector in each vector pair was at least 3 times slower than the rated test speed.

Several new test sets were added in the final package test. The new test sets include multiple-detect SSF test sets from University of Iowa [7], delay fault test sets from University of Southern California [8], and IDDQ test sets generated by vendors' ATPG tools. To study the possible cause for pattern-dependent defects, we added test sets that were modified from the original SSF test sets by preceding each vector with all-one, all-zero, or bitwise complemented vectors. We also added test sets that have a reverse sequence from the original SSF test sets.

This paper is organized as follows. Section 2 lists the dies selected for the final package test based on previous experiment results. Section 3 describes the experimental setup in the final package test. Section 4 describes the new test sets added in the final package test. Section 5 shows the preliminary results from the final package test. Section 6 concludes the paper.

2. Die Selection

We identified 149 "*interesting*" dies for further study based on the results from the wafer probe [3] [4]. These include 125 dies that failed at least one sampling (Boolean) tests at the nominal supply voltage, 23 dies that passed all the sampling tests at the nominal supply voltage but failed some VLV tests for either CUTs or test support circuitry, and one die that passed all the sampling tests at the nominal supply voltage and VLV tests but had IDDQ measurements more than 1mA in the wafer probe.

There were 128 failing CUTs for the sampling tests at the nominal supply voltage [4]. We define a *CUT sampling failure* as a defect in a CUT that passed the Stage 1 tests but failed at least one sampling test at the nominal supply voltage. There were three dies that had 2 CUT sampling failures. Consequently, there were 125 dies that failed at least one CUT sampling test at the nominal supply voltage. There were 12 CUT VLV-only failures and 11 test support circuitry VLV-only failures. We define a *CUT VLV-only failure* as a CUT that passed all sampling tests at nominal supply voltage, passed the Stage 1 tests at very low voltage, but failed some sampling tests at very low voltage. A *test support circuitry VLV-only failure* is a defect in a die that passed all sampling tests at nominal supply voltage but failed Stage 1 tests at very low voltage. In this paper, a VLV-only failure can be either a CUT VLV-only failure or a test support circuitry VLV-only failure. There was no die with multiple CUT VLV-only failures.

We sent 4 wafers for failure analysis (FA wafers). None of the dies on the 4 FA wafers were selected for the final package test. We have packaged 143 "interesting" dies, which include 122 dies that failed at least one CUT sampling test at nominal supply voltage, 20 dies that had VLV-only failures, and one die that passed all sampling tests at nominal supply voltage and VLV tests but had IDDQ measurements more than 1mA in the wafer probe. We also packaged 166 dies that passed all tests in the wafer probe. We used a program that can arbitrarily select dies from all dies that passed all tests in the wafer probe to select these 166 dies. Table 1 lists the summary of the packaged dies for the final package test.

Table 1 Summary of the packaged dies

defect class	total number of dies based on [3] and [4]	number of packaged dies
CUT sampling failures	125	122
VLV-only failures	23	20
IDDQ failures	NA	1
good dies	NA	166
total	NA	309

3. Experimental Setup

The test plan for the final package test is similar to the one for the wafer probe. A two-stage testing strategy was used in the final package test. Stage 1 tests consist of gross parametric tests and test support circuitry tests. Stage 2 tests consist of actual CUT tests, which include verification, exhaustive, pseudo-random, weighted-random, stuck-at, transition, path delay, gate delay, signature analysis, IDDQ, and VLV tests. We only describe the additional test sets and test conditions used in the final package test in this section. The test plan of the wafer probe can be found in [2], [3], and [4]. For Stage 1 tests, we used the tests that were used in the wafer probe. We added new test sets and test conditions in the Stage 2 tests.

3.1 Supply Voltage

In the wafer probe, all Boolean test sets were run at 5V and 1.7V. To further investigate the effect of the supply voltage on the test results, we added another supply voltage, 2.5V, in the final package test. Chang and McCluskey have studied the supply voltage for VLV testing [9] [10].

1.7V is within the proposed supply voltage, $2V_t$ to $2.5V_t$. Only one extra supply voltage was added due to the consideration of the tester time for each packaged unit.

3.2 Test Timing

The test sets were applied at three different clock speeds in the wafer probe. A very slow clock speed was added when testing at nominal supply voltage in the final package test to differentiate timing-dependent defects from timing-independent defects. Table 2 lists the clock speeds used at nominal supply voltage.

Table 2 Clock speeds used at nominal supply voltage

test timing	clock speed
r-rated timing	rated speed of each CUT
s-slow timing	2/3 rated speed of each CUT
ss-very slow timing	less than 1/3 rated speed of each CUT
f-fast timing	faster than rated speed (15% for MUL and SQR, 5% for others)

At 2.5V and 1.7V, we used two clock speeds for all Boolean tests. A very slow clock speed was used at each supply voltage to investigate if any VLV-only failure is timing dependent. Tables 3 and 4 list the clock speeds used at 2.5V and 1.7V.

Table 3 Clock speeds used at 2.5V for the final package test

test timing	clock speed
r-rated timing	1/3 rated speed at 5V
ss-very slow timing	1/6 rated speed at 5V

Table 4 Clock speeds used at 1.7V for the final package test

test timing	clock speed
r-rated timing	1/5.6 rated speed at 5V
ss-very slow timing	1/8 rated speed at 5V

3.3 IDDQ Measurements

Special care was taken during IDDQ measurements. There are four input pins with pull-up resistors. These four pins are the control pins for the embedded CrossCheck array [11]. When measuring IDDQ currents, all four of these pins were tied to the supply voltage source of the tester to eliminate the static current due to the voltage difference between V_{dd} and V_{ih}. The current limit for the measurement was set to 800µA to ensure good resolution for both high and low current states. The resolution of the current measurement is 200 nA. The wait time before each IDDQ measurement is 1ms.

Researchers have reported data on IDDQ measurements at different supply voltages [12]. In the final package test, we did IDDQ measurements at 5.25V, 2.5V, and 1.7V. V_{ih} was set to the supply voltage and V_{il} was set to 0V for all IDDQ measurements. No output pins were loaded during the IDDQ measurements.

4. Test Sets

Based on the results in [3] and [4], we added several test sets for the final package test. Some new test sets were contributed by University of Iowa and University of Southern California. We also used some updated commercial tools, such as Mentor Graphics and Sunrise's ATPG tools, to generate new test sets. To study the causes of pattern-dependent failures, we modified some of the original test sets. We describe each new test set in turn.

SSF Tests

We have multiple-detect SSF test sets with more resolution for the final package test. In the wafer probe, there were only one 5-detect and one 15-detect SSF test sets. In the final package test, we added 2-detect, 3-detect, 4-detect, 5-detect, 7-detect, 10-detect, 12-detect, and 15-detect SSF test sets. Unlike the two multiple-detect SSF test sets, which were generated by ad-hoc techniques, the new multiple-detect SSF test sets were generated by university ATPG tools that were built to generate multiple-detect SSF test sets. We also had more 100% SSF test sets that were generated by latest version commercial tools.

Delay Test Sets

These include path delay fault test sets generated by university tools and transition fault test sets generated by a commercial tool. These test sets are only available for three control logic CUTs, STD, ELM, and ROB.

IDDQ Test Sets

Two types of IDDQ test sets were added. One was generated by ATPG tools that use the pseudo stuck-at model. The vectors in the other type were selected from a set of functional vectors. The static current of each vector was measured and recorded.

Test Sets Modified from Original Test Sets

In [4], there were significant amount of CUT sampling failures that were pattern-dependent. A CUT with *pattern-dependent defects* behaved differently when the pattern preceding each vector was changed. In the wafer probe, simulated scan data source mode was used for design verification, SSF, switch-level, weighted-random, and stuck-open test sets. We modified these test sets in four different ways:

a. Insert an all-one vector in front of each vector.

b. Insert an all-zero vector in front of each vector.

c. Insert a bitwise complemented vector in front of each vector.

d. Reverse the vector sequence in the original test set.

These modified vectors were only applied through parallel load data source.

Exhaustive Test Sets

We added exhaustive test sets for the two low voltage tests. The results of these exhaustive test sets can be used as references for the results from the two low voltage tests.

5. Experimental Results

We present preliminary experimental results in this section. Most interesting dies failed the same CUT as in the wafer probe. Six dies failed the Stage 1 tests in the final package test. We exclude these 6 dies from the discussion in this paper. Three of the 6 dies had CUT sampling failures in the wafer probe. Five dies that had CUT sampling failures in the wafer probe passed all the tests in Stage 1 and 2 in the final package test. We only use the IDDQ measurements of these 5 dies for IDDQ distribution analysis but exclude them from other discussion in this paper. Because CUTs are isolated from each other, we use a CUT instead of a die as the unit for discussion.

We focus on IDDQ measurement results and VLV test results in this paper. We present these results in turn and then correlate the results with the defect class of each CUT based on the results in the wafer probe [4].

5.1 IDDQ Measurements

There are 6 IDDQ test sets used in the final package test. Table 5 lists the test length and the property of each IDDQ test set. The name of each tool is the same as the one in [1]. In this paper, we only discuss the IDDQ measurements at 5.25V. Figure 1 shows the distribution of maximum IDDQ of all CUTs. The Y axis in Fig. 1 is in logarithmic scale. There are 1515 data points measured from 303 dies in Fig. 1.

Table 5 IDDQ test set summary

Test set	Test Length					property
	MUL	SQR	STD	ELM	ROB	
IDDQ1	41	26	26	25	70	Tool 3, pseudo stuck-at
IDDQ2	43	29	25	26	66	Tool 3, selected vectors
IDDQ3	25	20	31	37	109	Tool 7, new version
IDDQ4	19	10	22	27	68	Tool 7, old version
IDDQ5	90	72	35	36	65	Tool 6
IDDQ6	64	64	64	64	128	pseudo-random

Figure 1 shows that the maximum IDDQ measurements of most CUTs were either larger than 100µA or smaller than 5µA. In fact, most low IDDQ measurements were smaller than 3µA. However, there were still many CUTs whose maximum IDDQ measurements fell between these two values.

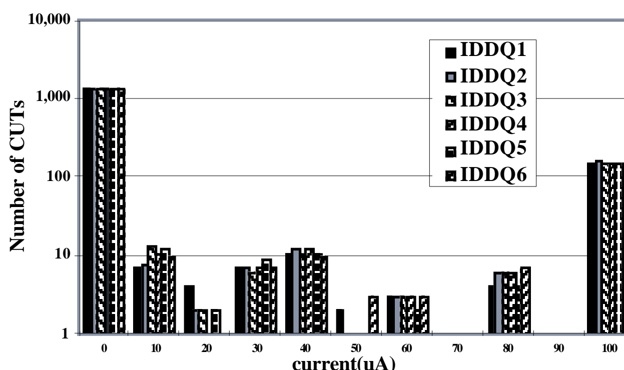

Figure 1 Max. IDDQ distribution (in logarithmic scale)

There were 161 CUTs whose maximum IDDQ measurements were larger than 100µA for at least one IDDQ test set. These 161 CUTs were on 92 dies. 72 dies had only one CUT whose maximum IDDQ measurement was larger than 100µA. The other dies had more than one CUT whose maximum IDDQ measurement was larger than 100µA. Table 6 lists the number of dies that had at least one CUT whose maximum IDDQ measurement was larger than 100µA. We only found 3 instances that a die had more than one failing CUT in the wafer probe. We explain the reason why we had more dies with more than one CUT IDDQ failure as follows. When we applied an IDDQ test set to one CUT, the inputs of the other 4 CUTs were held at zero. If the all-zero vector provoked the defect that caused high IDDQ measurements, we could get high IDDQ measurements no matter which CUT was being tested.

Table 6 The number of dies with at least one CUT whose maximum IDDQ measurement is over 100µA

number of CUTs per die over the current limit	number of dies
5	13
4	4
3	2
2	1
1	72
total	92

Table 7 shows the IDDQ measurements for CUTs with different defect classes. We only show CUTs that either were in defect classes or had IDDQ measurements larger than 3µA. The last column in Table 7 lists the number of CUTs that had IDDQ measurements within the current range but were not detected by any other tests. This number could be larger than the ones listed in the table because we only packaged 309 dies and no IDDQ

information was available for selecting dies for the final package test.

Table 7 Defect classes vs. IDDQ measurements

current range	TIC	SSF TIC	non-TIC	VLV-only	others
≥ 100μA	50	27	38	3*	1
(< 100μA) & ≥ 20μA	3	3	7	5	1
(< 20μA) & (≥ 3μA)	3	3	2	0	4
< 3μA	9	5	5	11**	NA

* 1 failed test support circuitry tests at very low voltage
** 9 failed test support circuitry tests at very low voltage

Several observations can be made based on the results in Table 7.

A. Not all non-TIC CUTs had high IDDQ measurements. Thus, timing-dependent defects may not be detected by IDDQ tests.

B. Although most defects could cause high IDDQ currents, there were some that could only slightly increase IDDQ currents.

C. Only some VLV-only CUTs had high IDDQ measurements. This indicates VLV tests and IDDQ tests may detect different defects.

5.2 VLV Tests

There were 23 VLV-only failures based on the data from the wafer probe. 11 of them failed support circuitry tests at very low voltage in the wafer probe. The other 12 failed CUT sampling tests. 10 out of the 12 CUT VLV-only failures and 10 out of the 11 test support circuitry VLV-only failures were packaged for the final package test. One of the 10 CUT VLV-only failures in the wafer probe passed all tests in the final package test. This could be due to the wrong information from the wafer map for die selection. No selected dies from this wafer repeated the results from the wafer probe in the final package test. We exclude all these dies for the discussion in this paper. Table 8 lists the test results of the 9 CUT VLV-only failures in the final package test. We used the symbols in Tables 2, 3, and 4 to indicate the different clock speeds at each supply voltage. r is "rated" timing, s is "slow" timing, ss is "very slow" timing, and f is "fast" timing. "E" means "test escape for all tests applied". "F" means "at least failed some tests".

CUT3 failed exhaustive tests using at-speed clocking mode and passed all the other test sets using nominal clock speed. The other CUT VLV-only failures had test escape for all the tests in rated, slow, and very slow clock speeds at nominal supply voltage. Most CUT VLV-only failures failed some tests for both rated and slow clock speeds at 1.7V. Only one, CUT7, failed some tests for rated clock speed but passed all tests for slow clock speed. This CUT, however, had high IDDQ measurement, 717μA. Consequently, it is a timing-dependent defect instead of a false alarm. The results also confirmed the rated speed at 1.7V, which was decided based on the shmoo plot from a good device.

Table 8 Test results of the 9 VLV-only failures

CUT	5V				2.5V		1.7V		max. IDDQ
	r	**s**	**ss**	**f**	**r**	**ss**	**r**	**ss**	
CUT1	E*	E	E	F	F	E	F	F	66.4μA
CUT2	E	E	E	F	F	E	F	F	65.6μA
CUT3	F**	E	E	F	F	F	F	F	> 800μA
CUT4	E	E	E	F	E	E	F	F	47.2μA
CUT5	E	E	E	F	E	E	F	F	51.6μA
CUT6	E	E	E	E	E	E	F	F	2μA
CUT7	E	E	E	F	E	E	F	E	717μA
CUT8	E	E	E	F	F	E	F	F	2.8μA
CUT9	E	E	E	F	F	F	F	F	81.0μA

* test escape for all tests applied
** failed some tests

The results in Table 8 also show that testing at 1.7V was more effective than testing at 2.5V. There were several test escapes when testing at 2.5V while all CUT VLV-only failures failed at 1.7V. This result supports the supply voltage proposed for VLV testing in [9] and [10]. Two CUT VLV-only failures had IDDQ measurements smaller than 3μA. This indicates that VLV tests detect some defects that are not targeted by IDDQ tests.

5.3 Defect Classes of Test Detection

We investigated the defect class of test detection for several tests. In this paper, we show the results of a 100% SSF test set, a transition fault test set, and IDDQ tests. The 100% SSF test set is test 2.2 in [3]. The transition fault test set is test 7.1 in [3]. We used all the IDDQ measurements from the 6 IDDQ test sets for this analysis. We used the test results of direct-clocking mode at the rated timing from the wafer probe for the 100% SSF test set and used the test results of the same clocking mode at the rated timing from the wafer probe for the transition fault test set. Because there were valid IDDQ measurements for 113 CUTs with sampling failures at the nominal supply voltage and rated timing, we only used these 113 CUTs for this analysis. The results shown in this section provide one data point and are valid within the scope of this experiment only. Figure 2 show the defect classes of the test detection for the 100% SSF test set, transition test set, and IDDQ tests with three different current limits, 3μA, 20μA, and 100μA.

Based on the results in Fig. 2, we make the following observations:

A. The combination of the IDDQ tests and the transition fault test detected everything.

B. All test escapes for the 100% SSF test set were non-TIC defects. All TIC defects were detected by this test set.

C. 4 out of the 5 test escapes for the transtion fault test set were non-TIC defects. The other one was non-SSF TIC defects.

D. The distribution of the test escapes for the transition fault test set was invariant to the current limits.

E. All SSF TIC defects were detected by the 100% SSF test set and transition fault test set.

F. The test escapes for the IDDQ tests include SSF TIC, non-SSF TIC, and non-TIC defects.

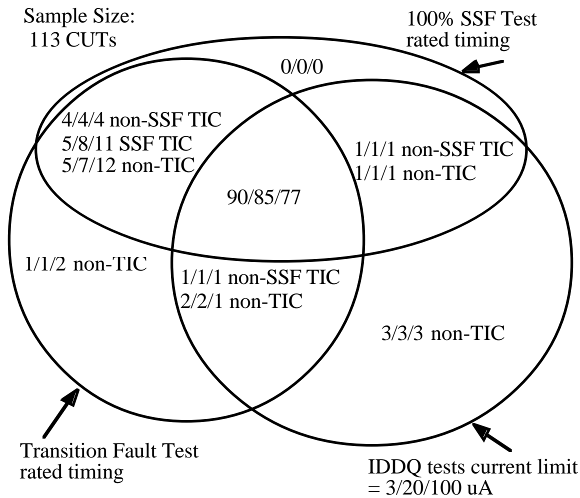

Figure 2 defect classes of test detection by different tests

6. Conclusions

The preliminary results of IDDQ tests and VLV tests for the final package test of an experimental test chip were included in this paper. We showed the distribution of maximum IDDQ measurements for 303 dies. We also showed the IDDQ measurements of CUT with different defect classes. Some TIC, non-TIC, and VLV-only defects did not cause elevated IDDQ measurements.

The supply voltage of VLV tests should be small enough to make VLV tests effective. There were many VLV-only failures which occurred only at 1.7V but did not show up at 2.5V. By using different clock speeds at very low voltage, we also showed that the test speed selected based on the shmoo plot of a good device is appropriate. Not all VLV-only failures had high IDDQ measurements. Thus, VLV tests may detect some defects that are not targeted by IDDQ tests.

We also investigated the defect classes of each test escape for 100% SSF, transition fault, and IDDQ test sets. All SSF TIC defects were detected by the 100% SSF test set. Also, most test escapes of the 100% SSF test set were non-TIC defects. Five out of the 6 test escapes for the transition fault test set were non-TIC defects. The test escapes of the IDDQ tests include both TIC and non-TIC defects. The combination of the IDDQ tests and the transition fault test detected everything except the one that failed only at the fast timing.

Acknowledgments

We would like to thank Piero Franco and Siyad Ma for their participation in the experiment. We also would like to thank Scott Keller and Michael Lynch at LSI Logic for providing the package units for bonding the dies in the experiments. We also would like to thank Hsiao-Ping Juan, Cecilia Krasuk, and Chien-Mo "James" Li for helping test the 309 dies. This work was supported in part by the National Science Foundation under Grant No. MIP-9107760, and by LSI Logic Corporation under Agreement No. 16517.

Reference

[1] Franco, P., *et al.,* "An Experimental Chip to Evaluate Test Techniques, Part 1: Description of Experiment," *Stanford University CRC Technical Report*, No. 94-5, 1994.

[2] Franco, P, *et al.*, "An Experimental Chip to Evaluate Test Techniques Chip and Experiment Design." *Proc. 1995 IT*C, Washington, D.C., pp. 653-662, Oct. 21-25, 1995.

[3] Ma, S.C., P. Franco, and E.J. McCluskey, "An Experimental Chip to Evaluate Test Techniques Experiment Results," *Proc. 1995 ITC*, Washington, D.C., pp. 663-672, Oct. 21-25, 1995.

[4] Franco, P., *et al.*, "Analysis and Detection of Timing Failures in an Experimental Test Chip," *Proc. 1996 ITC,* Washington, D.C., pp. 691-700, Oct. 20-25, 1996.

[5] Maxwell, P.C., *et al.*, "IDDQ and AC Scan: The War Against Unmodelled Defects," *Proc. 1996 ITC*, Washington, D.C., pp. 250-258, Oct. 20-25, 1996.

[6] Powell T.J., *et al.*, "Correlating Defects to Functional and IDDQ Tests," *Proc. 1996 ITC*, Washington, D.C., pp.501-510, Oct. 20-25, 1996.

[7] Pomeranz, I., and S.M. Reddy, "On n-detection Test Sequences for Synchronous Sequential Circuits," *Proc. 15th VTS*, Monterey, CA, Apr. 27-May 1, 1997.

[8] Chen, C., and S.K. Gupta, "A Satisfiability-Based test Generator for Path Delay Faults in Combinational Circuits," Proc. of 33rd DAC, Las Vegas, NV., pp. 209-214, Jun. 1996.

[9] Chang, J.T.-Y, and E.J. McCluskey, "Quantitative Analysis of Very Low-Voltage Testing," *Proc. 1996 VTS*, Princeton, N.J., pp.332-337, Apr. 28-May 1, 1996

[10] Chang, J.T.-Y. and E.J McCluskey, "Detective Delay Flaws by Very-Low-Voltage Testing," *Proc. 1996 ITC*, Washington, D.C., pp. 367-376, Oct. 20-25, 1996.

[11] Gheewala, T.R., "CrossCheck: A Cell Based VLSI Testability Solution," *Proc. 26th DAC*, Las Vegas, NV, pp. 706-709, 1989.

[12] Josephson, D., M. Storey, and D. Dixon, "Microprocessor I_{DDQ} Testing: A Case Study," IEEE Design & Test of Computers, Vol. 12, No. 2, pp. 42-52, Summer 1995.