Appendix A.

Testing for Tunneling Opens

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James C.M. Li and Edward J. McCluskey
Center for Reliable Computing
Stanford University

Abstract

A tunneling-open failure mode is proposed and carefully studied. A circuit with a tunneling open could pass at-speed Boolean tests but fail VLV testing or I_{DDQ} testing. Theoretical calculations as well as Boolean and I_{DDQ} experiments confirm the existence of tunneling opens. The Murphy experimental data show that seven out of nine VLV-only failure circuits can be explained by this failure mode. All these seven circuits survived 366 hours temperature burn-in. Finally, a cost effective screening strategy is proposed.

1. Introduction

A *tunneling open* is a very thin open that allows electrons and holes to tunnel through. Circuits with tunneling opens were first reported by [Henderson 91]. In that experiment, a large current was forced to flow through a metal wire and produced a narrow (about 100Å) opening at the input of an inverter. The logarithm of the tunneling current was found to be proportional to the voltage across the opening. The circuits only operated at very slow speeds (110KHz maximum) because the tunneling current was small.

Here we present a careful analysis of the tunneling-open failure mode. Theoretical calculations and experimental results show that a circuit with a tunneling open can pass at-speed tests at nominal voltage but slow down significantly at very low voltage. A burn-in experiment shows that the circuits with tunneling opens may not be detected by temperature burn-in. However, the existence of tunneling opens might indicate process problems. At the end of the paper, a cost effective screening strategy is proposed.

Very-low-voltage (VLV) testing is defined as Boolean testing performed at a very low supply voltage (around 2 to 2.5 times V_t) [Hao 93][Chang 96b]. VLV testing has been shown theoretically to be able to detect weak chips that contain *flaws* which do not cause functional failure at nominal operating condition but may cause intermittent or early-life failure. Table 1 compares the effectiveness of VLV, I_{DDQ} testing, temperature and voltage burn-in. Five failure modes are discussed as follows. (1) *Threshold voltage shift* is caused by hot carrier effects or process variation. This failure mode causes the circuit delay to increase significantly at very low voltage and therefore can be detected by VLV testing [Chang 96a]. This failure mode could also cause the background leakage current to increase and hence be detected by I_{DDQ} testing. Voltage burn-in is effective in accelerating the hot-carrier injection effect because the electrons are accelerated to a higher energy as the V_{DD} increases [Hnatek 95][Leblebici 93]. (2) *Gate oxide shorts* are caused by defective gate oxide. One simple model of this failure mode is a resistive short (between transistor gate and source or drain) which can cause excessive I_{DDQ} current. It has been shown that VLV testing is effective in detecting gate oxide shorts [Chang 96a]. Burn-in is also effective in screening this failure mode because high temperature and high voltage accelerate the oxide degradation. (3) *Metal shorts* are unexpected shorts between metal wires. This failure mode may cause high I_{DDQ} and it may also cause circuit delay to increase significantly at very low voltage. It has been reported that some circuits with metal shorts failed after burn-in [Righter 98].

Table 1. Effectiveness of VLV, I_{DDQ},
temperature and voltage burn-in

Failure Mode	VLV	I_{DDQ}	Temp. Burn-in	Volt. Burn-in
(1) V_t shift	Y	Y	*	Y
(2) Gate oxide shorts	Y	Y	Y	Y
(3) Metal shorts	Y	Y	Y	Y
(4) High resistance interconnect	N	N	**	**
(5) Tunneling opens	Y	***	N	?

* low temperature is effective [Hnatek 95]
** depends on the cause   ** depends on defect thickness

(4) *High resistance interconnect* can be caused by various mechanisms such as electronmigration, stress voids, or defective vias. This failure mode introduces extra RC delay which can be detected by delay testing. On the other hand, VLV testing does not detect this failure mode because RC delay does not scale when the supply voltage is reduced. Neither can I_{DDQ} detect this failure mode. Burn-in is effective in some cases (such as electronmigration) but ineffective in the others (such as silicide open [Tseng

00]). (5) In this paper, it will be shown that tunneling opens can pass at-speed tests at nominal voltage but fail VLV testing. Whether I_{DDQ} testing is effective or not depends on the defect thickness. It will be shown experimentally that temperature burn-in is not effective in screening tunneling opens. Whether voltage burn-in is effective is unknown so far.

The data shown in this paper are collected from the Murphy experiment [Franco 95] [Chang 98 ab] [McCluskey 2000]. A digital CMOS test chip was built in 0.7µ technology with gate oxide thickness = 200Å. It has five combinational *circuits under test (CUTs)* and the total gate count is 25K. In this experiment, nine chips (out of 5,500 tested) were found to have *VLV-only failures*. These chips passed millions of test patterns (including single stuck-at fault, transition fault, path or gate delay fault and exhaustive patterns) at nominal voltage (5V) but failed some tests at VLV (1.7V).

Now the question arises: can the failure modes listed in Table 1 explain all the VLV-only failures? To answer this question, I_{DDQ}(t) testing was performed on those VLV-only failure CUTs. *I_{DDQ}(t) testing* is defined as making multiple continuous I_{DDQ} measurements (for every test pattern) to observe the change in I_{DDQ} over time. Figure 1 shows the experimental results from one of the VLV-only failure CUTs. The chip was powered up and its I_{DDQ} current was allowed to settle before time "zero." At time zero, a test pattern was applied and 20 continuous I_{DDQ} measurements were taken (without changing the test pattern). For a good circuit, the I_{DDQ}(t) values should be constantly low (less than 1µA). But for this VLV-only failure CUT, some test patterns caused an *I_{DDQ}(t) drift over time* phenomenon, which is present if the I_{DDQ} values change significantly during the interval of observation. How fast the I_{DDQ} drifts down to zero is a function of supply voltage V_{DD} (section 4.2).

It has been reported that a circuit with an open defect may cause such an I_{DDQ}(t) drift over time [Maly 88] [Soden 89]. In both cases, the opens, caused by missing metal or polysilicon wires, are too large to permit tunneling. In Maly's experiment, an open defect was artificially injected in the source of a transistor. They explained this I_{DDQ}(t) drift phenomenon by the slow charging process of the reverse biased source-well junction. It took 15 seconds for the circuit to switch. In Soden's experiment, the circuit contained an open which caused the circuit to fail some tests. However, neither of these two cases mentioned above can explain the VLV-only failures in the Murphy experiment because a circuit with a large open could not pass so many thorough at-speed tests at nominal voltage. Some via or contact defects have been reported in [Needham 98] [Campbell 91] where the defects are modeled as high resistance interconnects (resistive opens). However, resistive opens cannot explain the observed $I_{DDQ}(t)$ drift over time phenomenon.

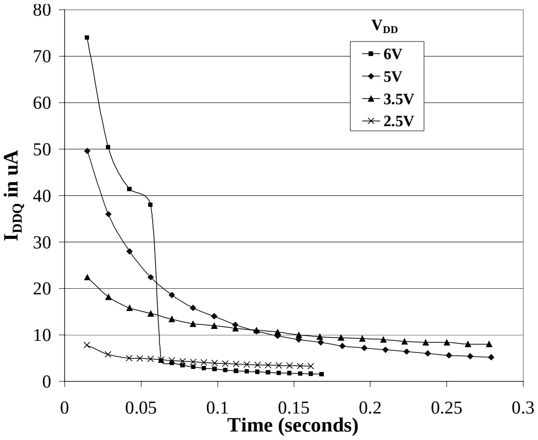

Figure 1. $I_{DDQ}(t)$ drift over time

The other explanation for the $I_{DDQ}(t)$ drift phenomenon of the Murphy chips could be a tunneling open. The tunneling open proposed here is much thinner (10-20Å) than that in Henderson's experiment. Such a narrow opening could be present at a via or a contact due to the incomplete oxide etching. The tunneling current through such a narrow opening is large enough to make the circuit operate at speed at nominal voltage. However, due to the exponential dependence of the tunneling current on the electric field across the opening, the circuit fails at very low voltage.

Table 2 shows the test results from nine VLV-only failure CUTs. They are classified into three categories according to their faulty behavior. The first two CUTs fail VLV testing (see section 4.1). These two CUTs have high and constant I_{DDQ} (section 4.2), and they failed after 6 hours of temperature burn-in (section 4.3). Their faulty behavior cannot be explained by tunneling opens. However, for the other seven CUTs, they operate at very slow speed at very low voltage. Their $I_{DDQ}(t)$ values either stay at a constant low value or drift down over time. Their behavior can be explained well by tunneling opens. All these seven CUT were unchanged after 366 hours of burn-in.

Table 2. Test results of nine VLV-only failure CUTs

category	CUT #	Speed @1.7V (sec. 4.1)	high I_{DDQ}? (sec. 4.2)	$I_{DDQ}(t)$ drift? (sec. 4.2)	fail after burn-in? (sec. 4.3)	explained by tunneling open?
I	1	hard failure	Yes	No	Yes	No
	2	hard failure	Yes	No	Yes	No
II	3	Very slow	No	No	No	Yes
	4	Very slow	No	No	No	Yes
III	5	Very slow	Yes	Yes	No	Yes
	6	Very slow	Yes	Yes	No	Yes
	7	Very slow	Yes	Yes	No	Yes
	8	Very slow	Yes	Yes	No	Yes
	9	Very slow	Yes	Yes	No	Yes

The organization of this paper is as follows. Section 2 introduces the basic physics of the tunneling effect. Section 3 first qualitatively explains the VLV-only failure by a tunneling open and then performs calculations to prove it. Section 4 provides a prediction of the behavior of the faulty circuits and then verifies with experimental results. Section 5 discusses some questions associated with tunneling opens. Finally, section 6 summarizes the paper.

2. Physics of the Tunneling Effect

When an insulator is thin enough, it is possible for electrons and holes to tunnel through it. The most commonly seen tunneling effects in CMOS technology can be classified into three categories according to their physical mechanisms. They are described in the following sections.

2.1 Trap-Assisted Tunneling

This tunneling effect is assisted by the traps which are generated by the impurities in the oxide. This effect happens even at a fairly low electric field. The magnitude of this tunneling current depends on the quality of the oxide. The typical values lie in the range of 10^{-4} to 10μA/cm^2 [Mozzami 92][Gupta 97].

2.2 Fowler-Nordheim Tunneling

If the *electric field across the oxide (E_{ox})* is strong enough, it causes band bending which makes the barrier thinner. The tunneling current therefore gets higher as the E_{ox} gets stronger. This field dependent tunneling effect is called Fowler-Nordheim tunneling and can be quantitatively modeled by the following equation [Fowler 28].

$$J_{FN} = \alpha \cdot Eox^{2} \cdot e^{(-\beta/Eox)} \tag{1}$$

In the case of a metal/oxide/silicon structure, $\alpha = 9.92\text{x}10^{-7}$ AV^{-2} and $\beta = 2.635\text{x}10^{8}$ Vcm^{-1} [Weinberg 82].

2.3 Direct Tunneling

Direct tunneling can occur in a very thin oxide at very low electric field. The direct tunneling current can be modeled by multiplying the Fowler-Nordheim tunneling current with a correction factor as in the following equation [Schuegraf 92],

$$J_{DT} = J_{FN} \cdot (1 - \sqrt{(\phi_b - V_{ox})/\phi_b}\,)^{-2} e^{\beta[(\phi b - Vox)/\phi b]^{2}/Eox} \tag{2}$$

where ϕ_b is the barrier height. Equation (2) is applicable when the *voltage drop across the oxide (V_{ox})* is less than the barrier height.

2.4 Calculations

Figure 2 shows the tunneling current density for different silicon dioxide thicknesses (i.e., the thicknesses of the tunneling open) as a function of the *voltage across oxide (V_{ox}).* The numbers were obtained from equations (1) and (2), assuming an Al/oxide/n^+-polysilicon structure. In reality, the actual numbers may vary with the material and the quality of oxide. However, the shape of the curves should be similar. This figure shows that different tunneling effects dominate different V_{ox} regions. Take the 20Å curve for example, if V_{ox} is higher than 3V, FN-tunneling dominates and the logarithm of the tunneling current increases with V_{ox}. For V_{ox} between 3V and 1V, direct tunneling current dominates over FN tunneling current. For V_{ox} lower than 1V, trap-assisted tunneling current becomes the most significant.

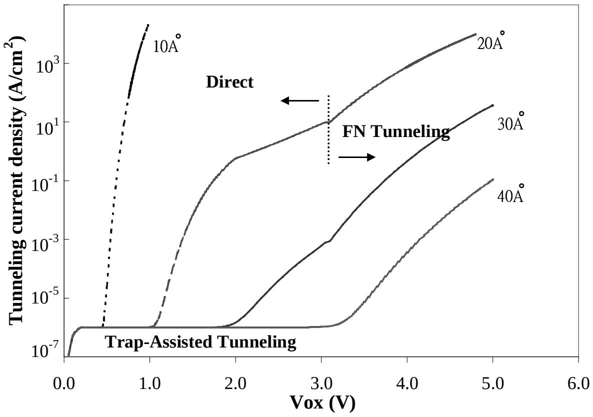

Figure 2. Tunneling current density for different oxide thickness (calculated)

3 Circuit Behavior with a Tunneling Open

3.1 Qualitative Description of a Tunneling Open

Figure 3 represents a tunneling open located at a contact hole. The metal and poly which should have been connected are separated by a very thin layer (10-20Å) of oxide. This kind of defect could be caused by incomplete etching or native (room temperature grown) oxidation after etching. Similar defects can also occur at a via where a thin air gap exists between the tungsten plug and metal wire. In the case of an air gap open, the tunneling current is smaller than the oxide case because the dielectric constant of air is about a third of that of oxide.

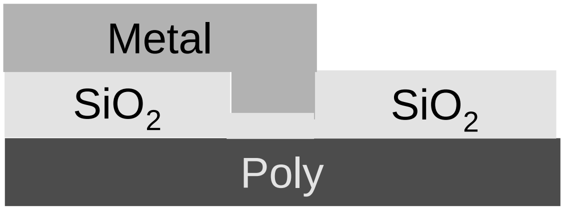

Figure 3. A tunneling open located at contact (not to scale)

Figure 4 shows an example circuit with a tunneling open located at the input of an inverter. As the voltage on the metal (V_m) ramps up, the electric field across the opening will cause the tunneling current (J_{tunnel}) to charge the gate capacitor (C_{gate}). The voltage on the poly (V_p) therefore rises. At nominal voltage, the field dependent tunneling current is large enough to switch the inverter in a very short time. However, at very low voltage, the tunneling current is so small that the inverter takes a very long time to switch. This explains why a circuit with a tunneling open can pass at-speed tests at nominal voltage but fail at very low voltage.

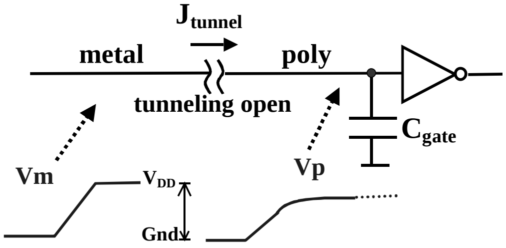

Figure 4. An example circuit with a tunneling open

When V_p stays at an intermediate voltage level, the PMOS and NMOS of the inverter are both turned on and high I_{DDQ} current is observed. As V_p continues to rise to V_{DD}, the electric field across the defect decreases and causes the tunneling current to diminish. Trap-assisted tunneling which happens at low electric field slowly charges the gate capacitor. The voltage on poly will gradually rise to V_{DD} and the I_{DDQ} will gradually drift down to zero. This slow charging process explains why a circuit with a tunneling open has very long I_{DDQ}(t) drift over time phenomenon. Note that if the tunneling open is very thin, V_p may rise so fast that high I_{DDQ} is not measurable. Therefore the observation of this phenomenon depends on the defect thickness.

Although it is not shown in the figure, the same arguments also apply to the opposite case in which V_m ramps down. However, the fall time is different from the rise time due to the polarity of the tunneling effect [Shi 98].

3.2 Theoretical Analysis

Consider the circuit of Fig. 4. Its voltage behavior and I_{DDQ}(t) drift behavior are calculated in sections 3.2.1 and 3.2.2 separately.

3.2.1 Voltage Behavior

Assume that the tunneling open has area A and thickness d. The *capacitance across the tunneling open C_{defect}* is ε_{ox}A/d. The *total capacitance of the gate capacitance* is *C_{gate}*. If there is no tunneling effect, the total charge on the poly is conserved. The voltage on the poly due to the coupling effect can be expressed as:

$$V_{p\_no\_tunneling}(t) = V_m(t) \cdot \frac{C_{defect}}{C_{defect} + C_{gate}} \qquad (3)$$

However, if the tunneling effect is taken into account, the total charge on the poly increases as the tunneling current flows through the open to charge the gate capacitors. In this case, the voltage on the poly can be expressed as:

$$V_{p\_tunneling}(t) = \left[V_m(t) + \frac{A\int J_{tunnel}(t)dt}{C_{defect}} \right] \cdot \frac{C_{defect}}{C_{defect} + C_{gate}} \qquad (4)$$

Compared with equation (3), equation (4) has one more term which corresponds to the total charge that tunnels through the open. The following calculations will demonstrate that this term cannot be ignored if the tunneling effect is significant.

Figure 5 illustrates the calculated waveforms for the voltage on poly (solid lines) given a ramp input voltage on the metal (dotted line) at nominal voltage. Based on the process technology of the Murphy experiment [LSI 93], the following numbers are assumed: nominal supply voltage $V_{DD} = 5V$, gate capacitance $C_{gate} = 40fF$, defect area $A = 1\mu m^2$ and defect thickness d = 12Å. If no tunneling effect is considered (equation 3), the $V_{p\_no\_tunneling}$ (thin solid line) eventually settles at 2V and the inverter is not switched (assuming logic threshold = $V_{DD}/2$ = 2.5V). However, if the tunneling effect is considered (equation 4), the $V_{p\_tunneling}$ (thick solid line) eventually goes higher than 2.5V and the inverter is switched. This calculation shows that the tunneling effect cannot be ignored when the open is as thin as 12Å.

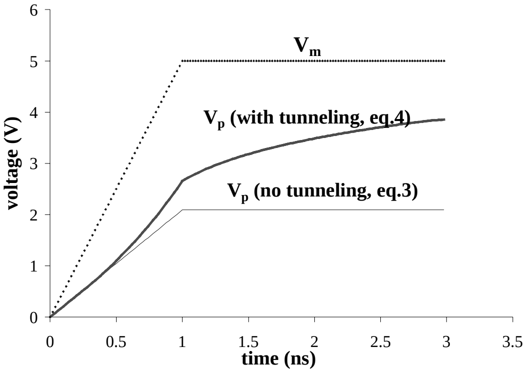

Figure 5. Voltage waveforms in circuit of Fig. 4 (V_{DD}=5)

Figure 5 illustrates two issues in testing tunneling opens. One is that tunneling and coupling effects take place so fast that no significant delay can be observed (only 0.5 ns delay from V_m = 2.5V to V_p = 2.5V). It is therefore very difficult to detect the tunneling open by transition or path/gate delay tests at nominal voltage. The other thing is that the V_p may not stay below (V_{DD}-Vt) for a long time. It depends on the thickness of the defect. Therefore it is not guaranteed that I_{DDQ} testing can detect a tunneling open.

In the Murphy experiment, the supply voltage of VLV testing is two times the transistor threshold voltage ($2V_t$ = 1.7V) [Chang 96b][Chang 98b]. Figure 6 shows the calculated waveforms at 1.7V given the same circuit as in Fig. 4. In this case, the voltages on poly calculated from eq.3 and 4 are almost the same (thin and thick lines overlap). The tunneling effect fails to boost the V_p above the logic threshold ($V_{DD}/2$ = 1.7V/2 = 0.85V) because the tunneling (FN or direct) current is small at low voltage. Although the circuit fails to operate at-speed, it eventually can operate correctly with the help of the small trap-assisted tunneling current given a very long wait time.

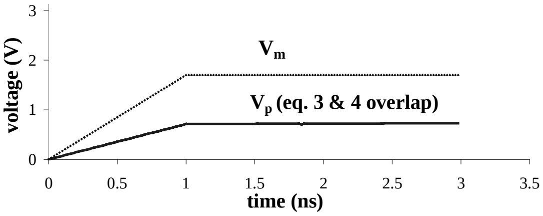

Figure 6. Voltage waveforms in circuit of Fig. 4 (V_{DD}=1.7)

3.2.2 I_{DDQ}(t) Drift Behavior

Consider the same circuit as shown in Fig. 4. Two assumptions are made: 1) the I_{DDQ}(t) drift over time phenomenon is dominated by the trap-assisted tunneling current (J_{TA}), and 2) the trap-assisted tunneling current remains constant. These assumptions, though not accurate, give a reasonably accurate approximation of J_{TA} as shown in the following equation,

$$J_{TA} = \frac{C_{gate} \cdot \varDelta V_p}{A \cdot T_{drift}} \tag{5}$$

where T_{drift} is defined as the time interval from the moment when trap-assisted tunneling current dominates to the moment when I_{DDQ}(t) drifts down to zero. $\varDelta V_p$ is the voltage change of V_p during the time interval T_{drift}.

In the nominal voltage simulation (Fig. 5), V_p rises slowly after reaching 4V which represents the end of FN (direct) tunneling effect and the beginning of trap-assisted tunneling effect. Before V_p reaches (V_{DD}-Vt), both PMOS and NMOS are turned on. Consequently, high I_{DDQ} is observed at the inverter. As the Vp rises from 4V to (V_{DD}-Vt), the I_{DDQ} gets smaller and finally drifts down to zero. Assuming that V_t is 0.8V, the voltage change of V_p before the I_{DDQ}(t) drifts down to zero is therefore (V_{DD} - V_t) - 4.0V = 0.2V which is ΔV_p. According to the experimental data, T_{drift} is in the range of 0.1 and 1 second. Using the same values of C_{gate} and A as in the last section, the estimated J_{TA} from eq. 5 would be around 8 to 0.8 μA/cm^2 which falls in the range of the typical values of trap-assisted tunneling current. This calculation shows that a tunneling open can explain the $I_{DDQ}(t)$ drift over time phenomena of the VLV-only failure CUTs.

4 Predictions and Experimental Results

This section first makes predictions for the faulty behavior of the circuits with tunneling opens. Experimental results collected from the Murphy chips are then shown to verify the predictions. Boolean and I_{DDQ} test results are shown in sections 4.1 and 4.2 respectively. Section 4.3 shows the burn-in results. Section 4.4 quotes some failure analysis results from the Sematech project [Nigh 97].

4.1 Boolean Tests

4.1.1 Predictions

Table 3 compares the speed ratio of four non-tunneling failure modes at nominal voltage and very low voltage [Chang 96a]. The *speed ratio* is defined as the speed of a defective-free circuit divided by the speed of a defective circuit. These numbers are obtained from simulations by injecting representative defects. This table shows that the difference between good and defective circuits becomes significant at very low voltage. A circuit with any of these non-tunneling failure modes could pass at-speed Boolean tests at nominal voltage but slow down 3 to 42 times at very low voltage. In some cases, the defective circuit cannot operate at all (*hard failure*).

Table 3. Speed ratio of non-tunneling failure modes

Failure mode	Speed ratio	
	NV	VLV
Transmission gate open	3.3	Hard failure
V_t shift	1.3	3.0
Diminished drive gate	1.9	3.2
Degraded signal	1.7	42.0

Figure 7 compares the expected speeds of three circuits: a good circuit, a circuit with a tunneling-open failure and a circuit with a non-tunneling failure. At nominal voltage (NV), all three circuits have similar speeds. At very low voltage (VLV), the circuit with a non-tunneling failure mode (thin solid line) slows down 3 to 42 times (or fails) while the circuit with a tunneling open slows down much more than 42 times. Note that the curve of a tunneling open has a knee. Above the knee, the FN or direct tunneling effect is large enough to make the circuit operate at speed. Below this knee, the small trap-assisted tunneling current makes the speed slow down significantly. It may take as long as milliseconds for the small tunneling current to charge the gate capacitors. Also note that the circuit with a tunneling open can operate at the same lowest V_{DD} ($V_{DD,min}$) at which a good circuit can function. On the contrary, the circuit with a non-tunneling failure may fail completely above $V_{DD,min}$.

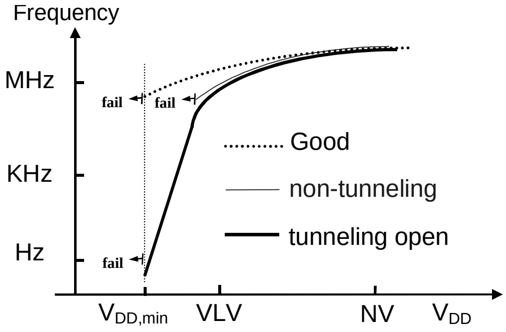

Figure 7. Predicted speeds of three circuits

4.1.2 Experimental Results

A speed measurement was performed to verify the predictions. The maximum speeds of the circuits were measured at different supply voltages. Table 4 lists the results of a good CUT and the nine VLV-only failure CUTs. The first row shows the speed of a good circuit. Its speed ranges from 37MHz to 4.17MHz as the supply voltage drops from 5V to 1.4V which is the lowest supply voltage ($V_{DD,min}$) at which a good circuit can function. At nominal voltage (5V), all CUTs have similar speeds. At very low voltage (1.7V), CUTs #1 and #2 failed to function (the slowest speed tested was 0.06Hz). CUT #3 operated 58 times slower than a good circuit. The other six CUTs were 20K times slower than a good circuit.

Table 4. Experimental circuit speeds (Hz)

CUT	5.0V	2.5V	1.7V	1.4V
good	37.0M	18.2M	7.69M	4.17M
1	35.7M	hard failure	hard failure	hard failure
2	33.3M	hard failure	hard failure	hard failure
3	37.0M	10.2M	132K	41.7K
4	35.7M	8.33M	1.75K	143
5	37.0M	3.33M	500	30.3
6	37.0M	6.25M	769	12.8
7	35.7M	5.88M	1.04K	16.1
8	35.7M	10.5M	3.57K	62.5
9	37.0M	12.7M	2.77K	50.0

Figure 8 shows the experimental circuit speeds of the good and the nine VLV-only failure CUTs based on the numbers in Table 4. The first two CUTs fail below V_{DD} = 4V and 3.5V respectively (their curves overlapped with the others). They do not match the expected behavior of tunneling opens. The last seven CUTs match the expected behavior of tunneling opens. The knee happens at 2.5V. They all operate at the same $V_{DD,min}$ as a good circuit.

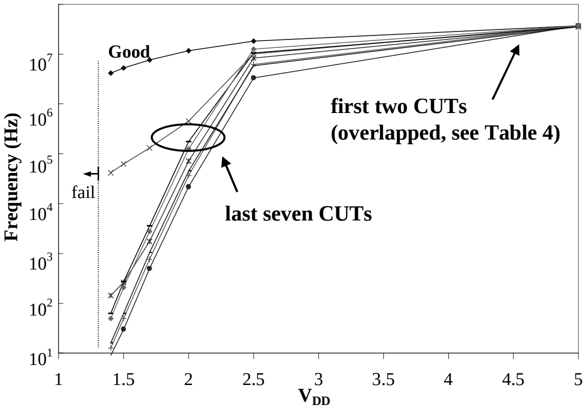

Figure 8. Experimental circuit speeds (see Table 4)

4.2 I_{DDQ} Tests

4.2.1 Predictions

Table 5 shows the predicted I_{DDQ} behavior of different failure modes that might cause VLV-only failure or $I_{DDQ}(t)$ drift over time. The first four failure modes have been discussed in connection with Table 1. The fifth failure mode, *defective PN junction*, could happen in the following cases: 1. PMOS gate to source(drain) shorts, 2. NMOS gate to substrate shorts, and 3. source(drain) - substrate(well) junction leakage. These defective PN junctions have very small reverse bias current which may cause long I_{DDQ}(t) drift as reported in [Maly 88].

Table 5. Predicted I_{DDQ}(t) of different failure modes

failure mode	High I_{DDQ}?	time constant of drift, τ	V_{DD} dependency of τ
(1) High resistance interconnect	No	No drift	No drift
(2) V_t shift (3) Gate oxide shorts (4) Metal shorts	Yes	No drift	No drift
(5) Defective PN junction	Yes	> ms	V_{DD} decrease, τ decrease
(6) Tunneling opens	Y/N*	> ms	V_{DD} decrease, τ increase

*depends on defect thickness

The first column shows whether the failure modes cause high I_{DDQ} or not. Depending on the defect thickness, a tunneling open may or may not cause high I_{DDQ}. The second column shows the *time constant* τ *of the* I_{DDQ}*(t) drift* which is defined in eq. 6. The I_{DDQ}(t) drift (see Fig. 1) is modeled by the following equation,

$$\boldsymbol{I_{DDQ}(t) = I_{drift} \cdot e^{-t/\tau} + I_{final}} \tag{6}$$

where I_{drift} is the amplitude of the I_{DDQ}(t) drift and the I_{final} is the final I_{DDQ} value. τ is referred to as the *time constant of* I_{DDQ}*(t) drift*. For the first four failure modes, I_{DDQ} should not change with time. For a defective PN junction and a tunneling open, the time constant may be as long as milliseconds or seconds.

The third column indicates whether the time constant is a function of supply voltage. For the case of a defective PN junction, since the current through a reverse biased PN junction is independent of the voltage, the time constant of I_{DDQ}(t) drift should go down linearly as the supply voltage goes down. On the contrary, for a tunneling open, the time constant should go up as the supply voltage goes down. Because FN and direct tunneling become insignificant at low voltage, the defective node stays at an intermediate voltage for a longer time.

4.2.2 Experimental Results

An I_{DDQ}(t) testing experiment was performed to verify the previous predictions. In this experiment, twenty continuous I_{DDQ} measurements were taken after applying each pattern. Each I_{DDQ} measurement took about 7-21 milliseconds. Table 6 lists the results collected from a good CUT as well as the nine VLV-only failure CUTs. The first row shows that the good circuit did not have I_{DDQ} higher than 1μA. The first two VLV-only failure CUTs had high and constant I_{DDQ} over time. The third and fourth CUT had low and constant I_{DDQ} over time. They can be explained with very thin tunneling opens (see section 3.1). The last five CUTs had I_{DDQ}(t) drift over time. None of the last five VLV-only failure CUTs has a time constant that decreases as the supply voltage drops. These results show that the last seven CUTs match the expected behavior of a tunneling open.

Table 6. I_{DDQ}(t) experimental results

CUT	first I_{DDQ} (μA)	I_{DDQ} drift?	I_{drift} (μA)	$\tau(V_{DD})$ in ms		
				6V	5V	3.5V
good	0.9	No	-	-	-	-
1	1800	No	-	-	-	-
2	328	No	-	-	-	-
3	0.8	No	-	-	-	-
4	0.7	No	-	-	-	-
5	65	Yes	24	14	28	84
6	45	Yes	40	28	55	180
7	50	Yes	50	28	44	70
8	35	Yes	35	28	63	91
9	40	Yes	40	28	63	140

Based on both experimental results shown in sections 4.1.2 and 4.2.2, the behavior of the first two CUTs can be explained by non-tunneling failure modes. The behavior of the last seven CUTs can be explained well by the tunneling-open failure mode.

4.3 Burn-in Experiment

4.3.1 Predictions

If the tunneling open is so thin, will it break down easily? It has been shown that for a carrier tunneling through the oxide, the minimum distance between collisions is about 8-15Å [Fischetti 85]. It means that in a very thin oxide, it is very possible for the carriers to undergo direct tunneling (ballistic transport) without damaging the oxide. Quantitatively, the charge to breakdown (Q_{BD}) is $1\sim10^4$ Coul/cm^2 for a 30Å oxide and $10^3\sim10^7$ Coul/cm^2 for a 25Å oxide [Schuegraf 94].

To estimate the lifetime of a 12Å thin oxide (as in the case of section 3.2.1), the following assumptions were made. The Q_{BD} is 10^7 Coul/cm^2. The charge going through the tunneling open is $V_{DD}/2$ x C_{gate} (= 2.5V x 40fF = 100fCoul) per switch. Calculation shows that a 12Å thin oxide can survive 10^{12} switches before it breaks down. This number is very large compared with the number of test patterns (in the order of millions, 10^6). So the tunneling opens may survive a long period of usage without breaking down.

After the tunneling open breaks down, the defective contact (or via) may become a resistive open. This does not mean the chip is "healed". Suppose the defective oxide thickness in Fig. 3 is not uniform. Only a very small area (A) is thinner so that most current flows through this small area. In this case, electron-migration could be serious due to localized high current density. Then the device may have reliability problems. Based on the above discussion, whether tunneling opens cause reliability problems is not known yet.

4.3.2 Experimental Results

Since high temperature is effective in speeding up the oxide degradation process [Schuegraf 94], a 366 hours temperature burn-in experiment was performed. Characterization tests (including speed measurement and I_{DDQ} testing) were performed before, during and after the burn-in process. The burn-in temperature was 130 degree C. The burn-in voltage was 5V, which is the highest available power supply voltage for the burn-in equipment used. Exhaustive test patterns were applied during burn-in (i.e., dynamic burn-in).

Table 7 shows the experimental results for good CUTs and the nine VLV-only failure CUTs. The changes of max I_{DDQ} values as well as the speeds at nominal voltage (5V) and very low voltage (1.7V) during the burn-in are listed. The first row shows the average values of a reference group of good CUTs. The first two VLV-only failure CUTs which are not suspected to have tunneling opens failed after the first six hours of burn-in. The other seven VLV-only failure CUTs which are suspected to have tunneling opens survived the 366 hours burn-in and their circuit behavior remained almost unchanged (except that CUT #7's I_{DDQ} increased after 6 hours of burn-in). Although all suspect CUTs survived the temperature burn-in, voltage burn-in will be performed in the future to further verify whether tunneling opens cause early-life failure or not.

4.4 Failure Analysis

Although failure analysis has not yet been done on these nine VLV-only failure CUTs, data from other experiments also support the existence of a tunneling open. In Sematech's experiment [Nigh 98], four out of seven "low voltage sensitive" dies which passed tests at nominal voltage but failed at low voltage were sent to failure analysis. Two of them were found to have gate-substrate or drain-substrate shorts. Nothing was found on the other two dies. This implies that some of the VLV-only defects are difficult to observe in failure analysis. A tunneling defect can be the culprit.

5 Discussion

5.1 Indication of Process Problems

Since the circuits with tunneling opens can operate at-speed at nominal voltage and they do not fail after burn-in, why do we want to test for tunneling opens? The answer is that the tunneling open can be an indication of process problems.

5.2 Screening Strategy

What is the best strategy to screen out the chips with tunneling opens? Traditionally, people use I_{DDQ} testing (single measurement per pattern, single pass/fail limit) to screen out weak chips. However, it has been shown in the previous sections that some tunneling opens may not fail traditional I_{DDQ} tests. Figure 9 shows a proposed screening strategy for tunneling opens. It should be performed after regular nominal voltage tests. This is a two-stage screening strategy which combines VLV and $I_{DDQ}(t)$ testing. Only if a circuit fails at VLV does it go to $I_{DDQ}(t)$ testing. If its $I_{DDQ}(t)$ values remain at a high and constant value (do not drift over time), the circuit is not a tunneling open. The circuit can cause early-life failure and must be rejected. If its $I_{DDQ}(t)$ values remain at a constant low level or its $I_{DDQ}(t)$ values drift over time, then the circuit might have a tunneling open. Compared with traditional I_{DDQ} testing, the proposed screening strategy is less costly because VLV testing requires shorter test time.

Table 7. Burn-in results (I_{DDQ} in μA, speed in Hz)

CUT #	before burn-in			after 6 hours burn-in			after 150 hrs. burn-in			after 366 hrs. burn-in		
	max	speed (Hz)		max	speed (Hz)		max	speed (Hz)		max	speed (Hz)	
	I_{DDQ}	5V	1.7V	I_{DDQ}	5V	1.7V	I_{DDQ}	5V	1.7V	I_{DDQ}	5V	1.7V
good	0.9	37M	7.7M	0.9	37M	7.7M	0.9	37M	7.7M	0.9	37M	7.7M
1	1080	35M	HF	1200	HF	HF	1K	HF	HF	1K	HF	HF
2	1480	33M	HF	2300	HF	HF	1K	HF	HF	1K	HF	HF
3	0.8	37M	132K	0.8	37M	125K	0.8	37M	133K	1.1	37M	145K
4	0.7	35M	1.7K	0.8	35M	1.51K	0.8	35M	1.58K	0.8	35M	1.54K
5	63.4	37M	500	63.8	37M	384	61.8	37M	370	62.8	37M	357
6	45.4	37M	769	45.8	37M	625	44.6	37M	714	45.2	37M	625
7	50	35M	1.0K	2980	35M	1.00K	3K	35M	0.91K	3K	35M	0.83K
8	32.4	35M	3.5K	32.4	35M	2.94K	32.4	35M	2.94K	32.4	35M	2.78K
9	36.0	37M	2.7K	36.4	37M	2.4K	35.8	37M	2.5K	30.8	37M	2.38K

HF: hard failure

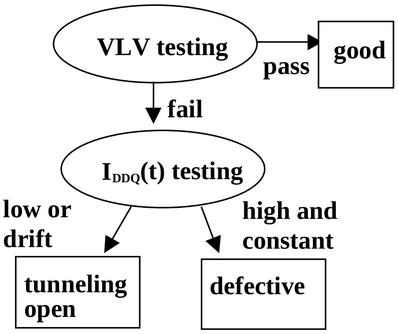

Figure 9. Proposed screening strategy for tunneling opens

The most effective test voltage to detect tunneling opens is the lowest possible supply voltage. As far as the test pattern is concerned, single-detect single stuck-at test patterns may not be effective because the tunneling effect has polarity dependence. Both the rise and fall transitions of a node have to be tested. Test patterns that have higher transition fault coverage such as transition fault test patterns or multiple-detect single stuck-at test patterns are more effective in detecting tunneling opens.

To verify the previous discussion, an experiment was performed [Chang 98a]. To change the number of transitions in a test pattern, the test pattern was modified into five different versions:

1. reordering the sequence of the vectors
2. padding an all-one vector before every vector

3. padding an all-zero vector before every vector
4. padding a bit-wise complemented vector before every vector
5. padding a one-bit-shifted vector before every vector

The testing was done at very low voltage (1.7V) and the test speed was the rated speed of a good circuit at 1.7V. The numbers of total failures were recorded. The first two non-tunneling open CUTs in Table 2 showed the same test results for the modified and original versions of test patterns. The last seven tunneling open CUTs showed different test results for some modified versions than for the original version. The experimental results support the previous arguments that the tunneling opens do not behave like stuck-at faults. The test results change with the number of transitions.

For $I_{DDQ}(t)$ testing, test patterns that have high coverage of node transition are effective because the $I_{DDQ}(t)$ drift over time can only be observed after the defective node has transition. To save test time, two I_{DDQ} measurements for each test pattern might be enough. According to this experiment, the wait time between two measurements can be tens or hundreds of milliseconds. If the second measurement is less than a certain percent (e.g., 80%) of the first measurement, then the circuit is suspected of having a tunneling open.

5.3 Defect Coverage

What is the defect coverage of VLV testing for tunneling defects? Will it still be valid in more advanced technology than 0.7μ? As is shown in the calculation example in section 3.2.1, the defect thickness (d) which is detectable by VLV testing is a function of gate capacitance (C_{gate}) and defect area (A). Therefore the detectable defect thickness of the VLV testing varies with locations in the same circuit. Table 8 lists the calculated minimum detectable defect thickness (d_{min}) that VLV testing can detect. Some typical numbers were estimated. The calculation is done in the same way as described in section 3.2.1. Note that in this calculation, it is assumed that no charge leaks through the gate oxide at the moment of gate switching. This is a valid assumption because the charges that tunnel through the tunneling open (dominated by direct or FN tunneling) is orders of magnitude more than the charges that leak through the gate oxide (dominated by trap-assisted tunneling).

Table 8 shows that VLV testing is capable of detecting tunneling opens with defect thickness d_{min} as thin as 7Å. A question that might arise in connection with Table 8 is that since the nominal supply voltage is already lower in the advanced technology, why is VLV testing still effective? The answer is that the defect area (A) and gate capacitance (C_{gate}) are also scaled down. Therefore the calculation shows that VLV testing is still needed to screen out tunneling opens in advanced technologies.

Table 8. Minimum detectable defect thickness

feature size	NV (V)	VLV (V)	A (μm^2)	C_{gate} (fF)	d_{min} (Å)
0.7μm	5	1.7	1*	40*	12
.35μm	3.3	1.2*	0.3*	10*	8
.18μm	1.8	0.9*	0.07*	3*	7

* estimated numbers

6 Summary

Nine VLV-only failure CUTs were found in the Murphy experiment. A tunneling open is proposed to explain seven of these VLV-only failures. A tunneling open can occur at a contact or a via where a very thin layer of oxide allows tunneling current to flow through it. Theoretical calculations show that field-dependent tunneling current allows the circuit to pass at-speed tests at nominal voltage but causes it to operate at very slow speed at very low voltage. It is also shown that the trap-assisted tunneling current can cause $I_{DDQ}(t)$ to drift over an interval of hundreds of milliseconds.

The results of various experiments verified the theory. Table 2 summarizes the experimental results. These nine CUTs can be divided into three categories according to their faulty behavior. The first category failed at very low voltage. This category does not match the expected behavior of a tunneling open. This category could be caused by some non-tunneling failure mode, such as gate oxide shorts. The second category has very long delay at VLV but does not have high I_{DDQ}. The third category has very long delay at VLV and $I_{DDQ}(t)$ drift over time. The last two categories (seven CUTs) can be explained as tunneling-opens.

Although the tunneling open circuits have survived the 366 hours temperature burn-in, the existence of tunneling opens might indicate process problems. VLV testing followed by $I_{DDQ}(t)$ testing is proposed as a cost effective screening strategy.

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Appendix B.

Diagnosis of Tunneling Opens

Diagnosis of Tunneling Opens

James C.-M. Li and E. J. McCluskey

Center for Reliable Computing, Stanford University

cmli,ejm@crc.Stanford.edu

Abstract

This paper resolves two issues regarding diagnosis of tunneling opens: efficient screening and accurate localization. In the first part, a test pattern selection and sorting algorithm is presented. It is shown that the presented algorithm saves $I_{DDQ}(t)$ test time without impacting on its effectiveness. The second part of this paper presents a locating algorithm which combines both VLV and $I_{DDQ}(t)$ test results. This technique is shown to be able to accurately locate the tunneling opens with higher resolution than a commercial single stuck-at fault diagnosis tool.

1. Introduction

A tunneling open is a very thin layer of oxide located in a via or a contact. The tunneling open is so thin that it allows electrons or holes to tunnel through it [Li 00]. Diagnosis of tunneling opens is important to improve the process problems and hence increase the yield. (In this paper, the term “diagnosis” includes both identifying the defective chips as well as locating the defects within the chips.) However, chips with tunneling opens are difficult to identify because they pass thorough at-speed tests at nominal voltage. Furthermore, once we identify a tunneling open suspect chip, it is also difficult to perform failure analysis because the tunneling open is small and hidden. This paper provides solutions for these diagnosis issues: 1. how to efficiently identify chips with tunneling opens and 2. how to accurately locate tunneling opens within chips.

Figure 1 illustrates the diagnosis flow of tunneling opens. Those chips that failed Very-low-voltage (VLV) testing are further tested by *$I_{DDQ}(t)$ testing* which is defined as taking multiple continuous I_{DDQ} measurements in a single pause. *$I_{DDQ}(t)$ drift over time* is defined as the $I_{DDQ}(t)$ values decrease significantly during the duration of measurement. Those chips that have $I_{DDQ}(t)$ drift over time are possible tunneling open suspects [Li 00].

They go on to the next stage, locating the failures. Finally, a culprit list is obtained. A *culprit list* is a collection of circuit gates that can cause the observed faulty behavior.

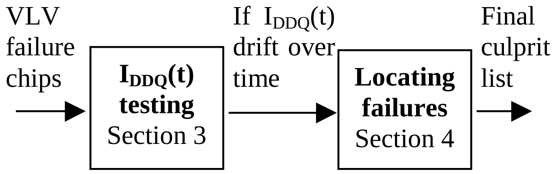

Figure 1. Diagnosis flow of tunneling opens

The first portion of this paper aims at efficient screening for tunneling opens. Since I_{DDQ}(t) testing is a time consuming test, short test patterns that detect the tunneling opens as soon as possible are needed. Instead of building an ATPG tool to generate test patterns, a simple but efficient test pattern selection and sorting algorithm is presented. Just as an I_{DDQ} pattern selector selects test pattern for I_{DDQ} testing [Mao 92], the presented I_{DDQ}(t) pattern selector selects (and sorts) test pattern for I_{DDQ}(t) testing. This selector takes any available test patterns generated by the designers or by ATPG tools. It adopts a "greedy" algorithm which sorts test patterns to maximize the probability of detecting tunneling opens as early as possible. The presented I_{DDQ}(t) pattern selector is economic both in terms of test pattern selection process as well as test time.

After identifying the tunneling open suspects, the second issue is to locate the tunneling opens. (In this paper, we assume that tunneling opens are caused by random defects. They do not occur in every via or contact.) Traditionally, people use single stuck-at fault (SSF) diagnosis tools to locate failures. For tunneling opens, the existing single stuck-at fault diagnosis tools may not be accurate enough because a circuit node with a tunneling open not necessarily stuck at a logic zero or one. On the other hand, I_{DDQ} diagnosis algorithms which have been previously presented are based on bridging fault or transistor leakage fault model [Aitken 91] [Chakravarity 92] [Nigh 97] [Thibeault 97]. These fault models are not accurate for tunneling opens. So far, there is no diagnosis algorithm that is suitable for locating a tunneling open.

In this paper, a two-step algorithm is presented for locating the tunneling opens with high resolution. The first step uses VLV test results to generate a small initial culprit list. The second step further reduces the number of culprits by utilizing the I_{DDQ}(t) drift over time information. It will be shown that the presented algorithm gives correct results with higher resolution than a commercial single stuck-at fault diagnosis tool. A diagnosis is *correct* if the actual defect location is included in the reported culprit list. A diagnosis has *high resolution* if the number of the reported culprits is small.

This paper is organized as follows. The second section shows two example circuits and defines the terminology. The third section describes the test pattern selection and sorting algorithm. The fourth section describes the locating algorithm. In both Sections 3 and 4, simulation and experimental results are shown to validate the presented algorithm. Then the fifth section summarizes this paper.

2. Examples and Definitions

2.1. An Inverter Example

Figure 2(a) shows an example inverter with a tunneling open located at its input. Suppose the metal voltage (V_m) rises, the Fowler-Nordheim tunneling current (J_{tunnel}) charges the gate capacitor (C_{gate}). The voltage on the poly (V_p) therefore follows. While the V_p is at an intermediate value, high I_{DDQ} is observed. As trap assisted tunneling current continues to charge C_{gate}, V_p rises at a slow speed. $I_{DDQ}(t)$ therefore decreases gradually with time. Figure 2(b) shows an example $I_{DDQ}(t)$ drift over time which is measured from one of the Murphy test chips [Li 00][McCluskey 00]. Similar things happen when the input signal has a fall transition. The conclusion is that $I_{DDQ}(t)$ drift over time is observed when the input of inverter has high-to-low or low-to-high transition.

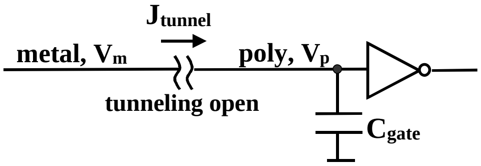

Figure 2(a) Inverter with tunneling open

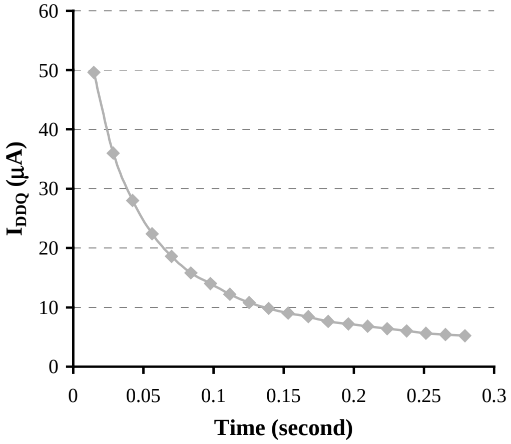

Figure 2(b) I_{DDQ}(t) drift over time

2.2. Definitions

Some terms are defined here to facilitate further discussions. *Pseudo transition fault test patterns* are defined as test patterns that detect transition faults (slow-to-rise or slow-to-fall). The fault effect, in analogy to pseudo stuck-at fault test patterns, does not have to propagate to the primary outputs to be observed. The fault effect, however, can be observed by I_{DDQ}(t) testing. A *pseudo transition fault test pattern pair,* denoted as {p1, p2}, is made up of two patterns. The first pattern, p1, initializes the state and the second pattern, p2, launches a transition. *Pseudo transition fault coverage* is defined as the number of transition faults which are detected by a set of pseudo transition fault test patterns over the number of total transition faults. A *pseudo transition fault dictionary* is a lookup table which specifies the pseudo transition fault test patterns and the transition faults they detect.

2.3. An NAND Gate Example

Figure 3 shows a NAND gate T that is part of a larger circuit. Two of the primary inputs (P.I.), A and B, are connected to gate T. The output of gate T (node Z) is connected to some other gates. Figure 4 shows the schematic of the NAND gate T implemented in static CMOS. All the fourteen via or contact locations where a tunneling open can occur are marked with d#.

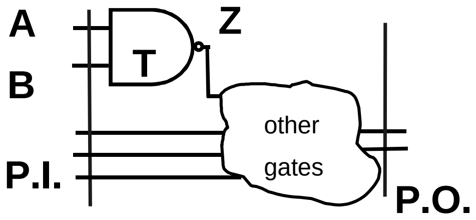

Figure 3. Example circuit with NAND gate T

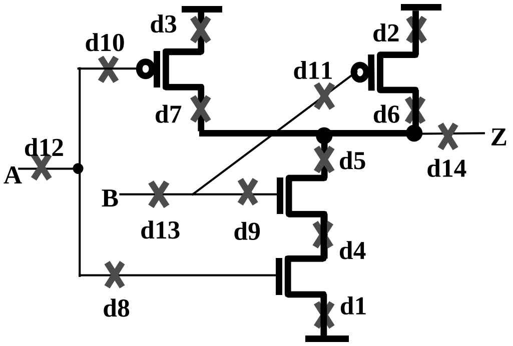

Figure 4. Fourteen defect locations in gate T

Table 1 shows a pseudo transition fault dictionary for the circuit in Figure 3. Every row represents a test pattern pair. For example, the first test pattern pair launches a falling transition at input A. Whether or not this transition fault propagates to the primary outputs, this test pattern is a valid pseudo transition fault test pattern. This pattern pair detects A slow-to-fall and Z slow-to-rise faults. These two columns, test patterns and their detected faults, constitute the pseudo transition fault dictionary.

Table 1. Pseudo transition fault dictionary

Test pattern			Detected Faults*	Detected Defects
A	B	Z		
Fall	1	Rise	Af,Zr	d3,d7,d10,d12,d14
Rise	1	Fall	Ar,Zf	d1,d4,d5,d8, d10,d12,d14
1	Fall	Rise	Bf,Zr	d2,d6,d11,d13,d14
1	Rise	Fall	Br,Zf	d1,d4,d5,d9, d11,d13,d14

[*] Af = A-slow-to-fall fault

There is an additional column showing the tunneling open defects that can be detected. For example, the first test pattern pair can detect five defects: d3,d7,d10,d12 and d14. It can be observed that, these four pseudo transition fault test patterns detect all transition faults in a NAND gate, they also detect all the tunneling opens. That is, 100%

pseudo transition fault coverage of a NAND gate guarantees to detect all tunneling opens in it.

3. Test Pattern Selection and Sorting

In I_{DDQ}(t) testing, the test time is proportional to the number of pauses needed (each pause consists of multiple continuous I_{DDQ} measurements). The *test length* of an I_{DDQ}(t) testing is defined as the number of pauses needed. In this section, a test pattern selection algorithm is presented. Section 3.1 describes the algorithm. Section 3.2 and 3.3 shows simulation and experimental results respectively.

3.1. Algorithm

An initial fault list **F** is set to be all the transition faults in the circuit. The initial pattern list **P** is the collection of pattern pairs of every two neighboring test patterns. For example, if the original test pattern sequence is $\{p_1,p_2,p_3...p_n\}$, then $\{p_1,p_2\}$ is the first pattern pair and $\{p_2,p_3\}$ is the second pattern pair, *etc*.

The first step is to run a customized fault simulation to build a pseudo transition fault dictionary for every pattern pair in **P**. Based on this dictionary, the second step selects a pattern pair that detects the most transition faults. The third step updates the fault list **F** by deleting the detected faults. The pattern list **P** is also updated by deleting those pattern pairs that do not detect any undetected faults in **F**. If both **F** and **P** are not empty, the algorithm goes back to the second step. Otherwise it stops and the selected pattern pairs are reported (in the selection order). This algorithm maximizes the possibility to detect transition faults and hence maximizes the possibility to detect tunneling opens. Because the selected patterns have the same pseudo transition fault coverage as the original patterns, the selected patterns have the same effectiveness as the original ones.

In the case of combinational circuits, the selected test patterns can be applied in the sorted order. In the case of sequential circuits, the test patterns (assumed to be sequential patterns, not scan patterns) have to be applied in the original order. However, I_{DDQ}(t) measurements are necessary only for those selected patterns.

3.2. Simulation Results

To prove the effectiveness of the pattern selection and sorting algorithm, a computer simulation is performed. Table 2 shows two circuits used in this simulation. They are also used in the Murphy chips. The first circuit is a six-bit squarer. It has 313 test patterns which are originally generated by an academic ATPG tool which detects every single stuck-at fault 15 times. If no pattern selection is performed, it would require pauses at all 313 patterns to make $I_{DDQ}(t)$ measurements. After selection, only 51 test patterns were selected. The test length is reduced by 83.7% while the same pseudo transition fault coverage is preserved. For the other circuit (m12, a multiplier), the algorithm also reduced the test length by 82.8%.

Table 2. Test length (original vs. selected)

Circuit	Original	Selected	Reduction
6sq	313	51	83.7%
m12	466	80	82.8%

Figure 5 compares the pseudo transition fault coverage of the original test patterns with the selected (and sorted) patterns. The Y-axis is the pseudo transition fault coverage and the X-axis is the test pattern length. This figure is plotted using the data from 6sq. It can be seen that the curve of the sorted test patterns (thick dots) grows faster than the curve of the original test patterns (thin line). This figure shows that the sorted patterns have higher probability of detecting a tunneling open earlier than the original test patterns. Both curves have the same final values of almost 100% fault coverage. This shows that the selected and sorted test patterns have the same effectiveness as the original ones. The other circuit, m12, shows similar trend and is therefore not plotted.

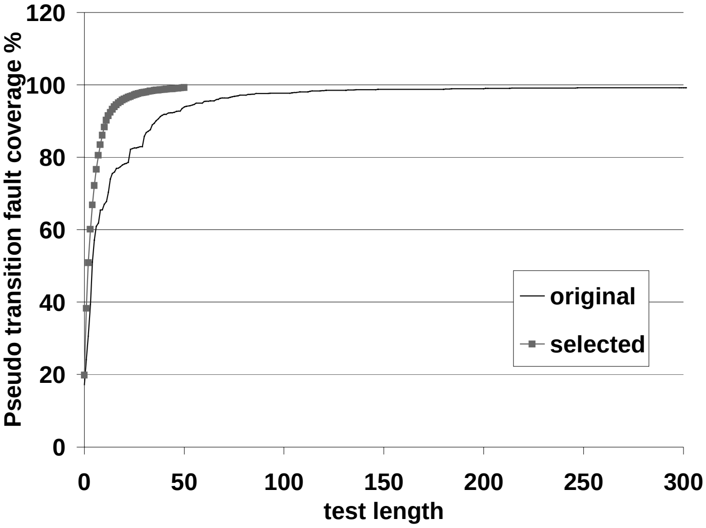

Figure 5. Growth of fault coverage (original vs. sorted)

3.3. Experimental Results

I_{DDQ}(t) testing is performed on five of the Murphy *CUTs* (circuits under test) that are suspected to have tunneling opens. They are either 6sq or m12. In the I_{DDQ}(t) experiment, after applying a specified test pattern, the tester paused and 20 continuous I_{DDQ} measurements are taken. Every single measurement takes between 7 and 21ms. Every I_{DDQ} measurement is recorded without setting any pass/fail threshold. If the last I_{DDQ} measurement is smaller than the first I_{DDQ} measurement by al least 10% and the difference is greater than 3μA, this test pattern is claimed to have I_{DDQ}(t) drift over time. (The I_{DDQ}(t) values of a good CUT remain low and constant below 3μA).

Both the original and sorted test patterns are applied in this experiment. Table 3 shows the first pattern that detects I_{DDQ}(t) drift over time. Assuming the I_{DDQ}(t) testing stops as soon as the first I_{DDQ}(t) drift over time is detected, then these numbers represent the test time needed. Take the first CUT for example, if all the 313 original test patterns are applied, the thirty-second pattern is the first one to detect I_{DDQ}(t) drift over time. If only the sorted 51 test patterns are applied, the I_{DDQ}(t) drift over time can be detected as early as in the nineteenth pattern. The test time saved is 41%. Only in one case, CUT #4, the sorted version requires more patterns than the original version. For all these five CUTs, 55% of the test time is saved on the average. None of these five cases escapes the selected (and sorted) test patterns. The experimental results show that the test pattern selection and sorting algorithm saves I_{DDQ}(t) test time without loosing effectiveness.

Table 3. First pattern to observe $I_{DDQ}(t)$ drift

CUT ID	Original	Sorted	Test time saved
1	32	19	41%
2	2	2	0%
3	5	1	80%
4	4	7	-
5	52	14	73%
Average	19	8.6	55%

4. Locating the Tunneling Open

The second portion of this paper addresses locating tunneling opens within the circuits. Section 4.1 first describes the algorithm. Section 4.2 and 4.3 show simulation and experimental results.

Notice that this localization technique is based on gates, not faults. From Table 1, it is observed that some defects can be modeled as more than one transition faults (e.g., d14 can be modeled as Zf and Zr). Therefore, this technique reports results in terms of gates instead of faults.

4.1. Two-step Localization Algorithm

Step 1 – Culprit List Generation

The first step utilizes the Boolean test results collected from the VLV testing. Traditionally, SSF diagnosis tools are used to diagnose Boolean failures. However, circuits with opens have sequential faulty behavior [Soden 89] which can confuse the SSF diagnosis tool and produce results containing a large number of innocent gates.

To understand the effect of the above problem, a computer simulation is performed. Table 4 shows the simulation results. The same Murphy circuits as section 3.2 are used again. The first circuit, 6sq, has 651 gates. The second circuit, m12, has 1677 gates. The test patterns applied are the same as that is used in section 3.

Six representative tunneling opens are injected by simulation. The first three rows show three different tunneling opens injected in a NOR gate in the 6sq circuit. These three tunneling opens locate in the same gate but their defect locations are different (similar to Fig. 4, there are also 14 different defect locations in a two-input NOR gate). The second three rows show three tunneling opens injected in a two-input AND gate in the m12 circuit. A fault simulation is performed to produce the faulty behavior of these faulty circuits.

The first column of Table 4 shows the numbers of culprit gates reported by a commercial SSF diagnosis tool. A *culprit gate* is the gate that contains the diagnosed fault. Although SSF diagnosis tool is correct in all six cases, the numbers of culprit gates are large (i.e. low resolution). The second column will be used in section 4.2 later.

Step 2 – Culprit List Reduction

To solve the above resolution problem, $I_{DDQ}(t)$ drift over time information is used to reduce the number of culprits. From Table 1, we know that $I_{DDQ}(t)$ is observed when the defective NAND gate is tested by pseudo transition test patterns. However, we do not know which pair it is because we do not know the defect location. The conclusion is that the necessary condition for $I_{DDQ}(t)$ drift to occur is that the defective gate is tested by one pair of the pseudo transition test patterns.

Before we go into the details of the algorithm, three example cases are discussed in Table 5. Suppose five test patterns (P_1 – P_5) are applied in sequence and $I_{DDQ}(t)$ are measured after every pattern. Assume that $I_{DDQ}(t)$ drift over time is observed after applying patterns P_2 , P_4 and P_5. For patterns P_1 and P_3, their $I_{DDQ}(t)$ values remain low and constant (i.e., no drift). Every row represents a gate G. Letter D in column P_n row G denotes that at least one fault of gate G is detected by a pseudo transition fault test pattern pair $\{P_{n-1}, P_n\}$. Letter ND denotes that none of the faults in gate G is detected by the pseudo transition fault test pattern pair $\{P_{n-1}, P_n\}$. A dash means don’t care (either D or ND).

In the first case, the culprit gate 1 is among one of the initial culprits reported by the step 1. Gate 1 was detected by three pattern pairs and they match the observed $I_{DDQ}(t)$ drifts. Gate 1 is called a *single culprit gate (SCG)* which is defined as a single gate that can explain all the $I_{DDQ}(t)$ drifts. In the second case, gate 2 and 3 are both reported by step 1. Although gate 2 or 3 alone does not match the $I_{DDQ}(t)$ drifts, the combination of them does. Therefore, gate 2 and 3 are called a pair of *multiple culprit gates (MCG)*. In case 3, suppose gate 4 and gate 5 are the only two gates reported by step 1. However, they can not explain all $I_{DDQ}(t)$ drifts. In this case, gate 4 and gate5 are only a portion of multiple culprit gates. Some warning message will be given saying that there should be some other undiagnosed faulty gates in additional to gates 4 and 5. The detailed algorithm of step 2 is as follows,

1. Construct a table similar to Table 5 with every column represents a test pattern with $I_{DDQ}(t)$ drift and every row represents a initial culprit gate obtained from step 1.
2. Check for single culprit gate (SCG)
3. If no SCG, check for multiple culprit gates (MCG)
4. If no MCG, check for incomplete multiple culprit gates (IMCG). Give warning messages.

4.2. Simulation Results

To compare with the commercial SSF diagnosis tool, the presented two-step algorithm is performed on the same six faulty circuits as in section 4.1. The $I_{DDQ}(t)$ test results are produced by computer simulations. The second column shows the numbers of culprit gates. The numbers are much smaller than the commercial SSF diagnosis tool gives. In all six cases, the presented algorithm gives single culprit gate (SCG) results and the injected faulty gate are located correctly. This shows that the presented algorithm successfully enhance the diagnosis resolutions without loosing correctness. On the average, the presented algorithm reports 3.7 culprit gates. Compared with the commercial SSF diagnosis tool, the presented algorithm reduces 94% of the culprits.

Table 4. Number of culprit gates (simulation)

Circuit	SSF	Presented	Reduction
6sq Total gate:651 Test length:313	21	4 (SCG)	81%
	12	4 (SCG)	67%
	4	4 (SCG)	0%
M12 Total gate: 1677 Test length: 466	226	5 (SCG)	98%
	81	3 (SCG)	96%
	3	2 (SCG)	33%
Average	57.8	3.7	94%

Table 5. Three cases of step 2

Case #	Initial culprits	P_1 no drift	P_2 drift	P_3 no drift	P_4 drift	P_5 drift	Results
Case 1	Gate1	-	**D**	-	**D**	**D**	Single culprit gate (SCG)
Case 2	Gate 2	-	ND	-	ND	**D**	Multiple culprit gates (MCG)
	Gate 3	-	**D**	-	**D**	ND	
Case 3	Gate 4	-	ND	-	**D**	ND	Incomplete Multiple culprit gates (IMCG)
	Gate 5	-	**D**	-	ND	ND	

D = detected by $\{P_{n-1}$ to $P_n\}$, ND = not detected, - = don't care

4.3. Experimental Results

To prove the effectiveness of presented two-step algorithm, experimental data are collected from the same five Murphy CUTs. For the VLV testing, all CUTs are tested at 1.7V which is about two times the transistor's threshold voltage. The waiting time between applying the primary input and strobing the primary output is 1μs. The testing continues until the end without aborting on failures. Every failing output is recorded. For $I_{DDQ}(t)$ testing, experiment is performed in the same way as described in Section 3.3 except that $I_{DDQ}(t)$ data are measured for every test pattern to maximize the amount of information (i.e. no selection).

Table 6 compares the numbers of culprit gates obtained from the commercial SSF diagnosis tool with our presented algorithm. In the first two cases, the presented algorithm shows incomplete multiple culprit gates. This indicates that there are still some culprit gates undiagnosed by step 1. In the other cases, single culprit gates are reported. The presented algorithm reduces the number of culprits by 67% on the average.

Table 6. Number of culprit gates (experiment)

CUT ID	SSF	Presented	Reduction
1	1	1 (IMCG)	0%
2	3	3 (IMCG)	0%
3	10	7 (SCG)	30%
4	6	1 (SCG)	83%
5	25	3 (SCG)	88%
Average	9	3	67%

5. Summary

This paper provides solutions to two diagnosis issues of tunneling opens. In the first part of this paper, a test pattern selection and sorting algorithm is presented. This algorithm selects (and sorts) pseudo transition fault test patterns to efficiently identify tunneling open chips. Table 2 shows that the selected patterns are approximately 80% shorter than the original ones. The experimental results are summarized in the left portion of Table 7.

In the second part of this paper, a two-step algorithm is presented to locate the tunneling opens. The first step uses VLV testing results to generates a small initial culprit list. The second step further reduces the number of culprits by using $I_{DDQ}(t)$ drifts over time information. Experimental results show that the presented algorithm gives only one third as many culprit gates as a commercial SSF diagnosis tool. The results are summarized in right part of Table 7.

Table 7. Summary of the experimental results

CUT ID	Test pattern selection and sorting			Localization		
	Before sorting	After sorting	Time saved	SSF	Presented	Culprit reduction
1	32	19	41%	1	1	0%
2	2	2	0%	3	3	0%
3	5	1	80%	10	7	30%
4	4	7	-	6	1	83%
5	52	14	73%	25	3	88%
Average	19	8.6	55%	9	3	67%

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Appendix C.

Testing for Resistive and Stuck Opens

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Testing for Resistive Opens and Stuck Opens

James C.-M. Li, Chao-Wen Tseng, and E.J. McCluskey
Center for Reliable Computing
Stanford University
http://crc.stanford.edu

Abstract

This paper studies the behavior of stuck and resistive open defects. The effects on test results of three test conditions (supply voltage, speed, temperature) as well as test patterns applied are evaluated. Diagnosis schemes for stuck and resistive opens are also presented. Five Murphy chips are diagnosed as having stuck open defects and one chip is diagnosed as having a resistive open defect. Their experimental data match our expectations for stuck opens and resistive opens.

1. Introduction

This paper studies two major types of open defects: resistive opens and stuck opens. A *resistive open defect* is defined as a defect resistor between two circuit nodes that should be connected. A *stuck-open defect* is a special case of a resistive open in which the resistance value is very large. (Please distinguish a stuck-open defect from a stuck-open fault.) Other open defects, such as tunneling opens and silicide opens, are discussed in [Li 00] and [Tseng 00] respectively.

The effects on test results of three test conditions (speed, supply voltage, temperature) as well as the test patterns applied are evaluated. Theoretical analysis, simulation and Murphy experimental test chip data [McCluskey 00] are used for this evaluation. Table 1 summarizes the results of this evaluation.

The test results for stuck-open defects do not depend on V_{DD}. Nominal V_{DD} testing is effective and changing the power supply voltage during tests is not necessary. Resistive open defects, on the other hand, are *voltage dependent*, which means the test results are different for different values of V_{DD}. It has been suggested that testing at supply voltage lower than nominal V_{DD} is effective for testing bad vias [Baker 99]. In this paper, it will be shown that the optimal test voltage depends on the defect location.

Our evaluation shows that testing at a supply voltage higher than nominal V_{DD} is effective for detecting resistive open defects located in the *wire delay significant paths* in which the wire delay is greater than 30%. On the contrary, *very-low-voltage (VLV) testing* in which V_{DD} is reduced to as low as 2 to 2.5 times the transistor threshold voltage [Chang 96] is effective for detecting resistive open defects located in the *gate delay significant paths* in which the gate delay is much larger than the wire delay (see Section 2.1).

Stuck-open defects can be detected by tests applied at slower than rated speed. For resistive open defects, it is known that resistive opens can cause extra signal delay [Needham 98][Baker 99]. Resistive opens cause *timing dependent* defect behavior, which means the test results may depend on the test timing. In this paper, we are going to define a metric, *delay ratio*, which is the delay of a defective circuit over that of a good circuit. Delay ratio represents the signal to noise ratio in distinguishing bad chips from good ones. Based on this metric, simulations show that *at-speed testing* in which the test is applied at the maximum speed of the circuit is effective for detecting resistive open defects (see Section 2.1).

Table 1. Three conditions and test patterns for detecting opens

Conditions	Stuck-open defect	Resistive open defect
V_{DD} (Section 2.1)	Test results not voltage dependent Nominal V_{DD} testing effective	Test results voltage dependent Optimal V_{DD} may depend on defect location
Speed (Section 2.1)	Test results not timing dependent Both at-speed and slow speed effective	Test results timing dependent At-speed testing effective
Temperature (Section 2.2)	Test results not temperature dependent Both hot and cold effective	Test results temperature dependent Optimal temperature may depend on defect material
Pattern (Section 2.3)	Test results sequence dependent Transition fault test patterns effective	Test results timing dependent Transition fault test patterns effective

In this paper, it is assume that the size of a stuck open defect is sufficiently large so that coupling effect does not change the test results. The *coupling effect* is defined as the transitions of signals of the other nodes affect the logic value of the faulty nodes through coupling capacitance. So far we have not yet identified any defective chip for which the test results are affected by the coupling effect in the Murphy experiment.

Resistive open defects are *temperature dependent*, which means the test results depend on the test temperature. Baker states that temperature does not make much difference in testing resistive opens, but no data are shown [Baker 99]. In this paper, the resistive open materials are assumed to be metal, for which the temperature coefficient of resistance is positive [Landolt 96]. Our simulation results suggest that testing at a temperature higher than room temperature is better than room temperature testing. However, in some other cases, resistive open defects of negative temperature coefficient materials (such as silicide opens) can be detected by testing at a temperature lower than room temperature [Tseng 00]. The overall conclusion is that the optimal test temperature may depend on the resistive open material (see Section 2.2).

Stuck-open defects exhibit a memory effect and defective circuits with stuck opens have sequential behavior [Wadasck 78] [Soden 89]. The Murphy experiment shows that some defective chip behavior is *sequence dependent* which means the test results depend on the test patterns' ordering even at very slow test speed [Chang 98a]. Stuck-open fault test patterns were developed to detect stuck-open defects [Elziq 82] [Chandramouli 83]. Cox showed that stuck-open faults in a CMOS network can be represented by transition faults (slow-to-rise and slow-to-fall) in equivalent gate level circuits [Cox 88]. In this paper, we will show that transition fault test patterns, which are supported by most ATPG tools are effective for detecting both stuck-open and resistive open defects (see Section 2.3).

I_{DDQ} testing is not guaranteed to be effective for all stuck-open and resistive open defects. This conclusion is consistent with previous research [Maly 88] [Hawkins 94] [Singh 95].

A diagnosis scheme for stuck opens and resistive opens is presented. From the 116 defective Murphy chips, five stuck-open suspect chips and one resistive open suspect chip are identified. Their experimental data (from VLV, I_{DDQ}, and shmoo testing) match our theoretical analysis for stuck opens and resistive opens.

The organization of this paper is as follows. Section 2 presents theoretical analysis for three test conditions as well as the test patterns for detecting stuck and resistive open defects. Simulation results are presented to confirm the theoretical analysis. In Section 3, five chips are identified as having stuck-open defects and one chip is identified as having a resistive open defect. Finally, Section 4 summarizes the paper.

2. Theoretical Analysis and Simulation Results

2.1. Test Speed and Test Voltage

An Inverter Chain Example

Consider the three-stage inverter chain in Fig. 1. The delay of the inverter in the middle can be estimated by the following equation,

$$Delay \cong [R_{tr}(V_{DD}) + R_{def}] \cdot C \tag{1}$$

where R_{tr} is the turn-on resistance of the transistor, which is a function of V_{DD}. R_{def} is the value of defect resistance, which is assumed to be insensitive to V_{DD} (assuming R_{def} is metal). C is the total load capacitance (including the gate capacitance and the wire capacitance). Compared with R_{tr}, C is relatively insensitive to V_{DD} and hence is assumed to be constant.

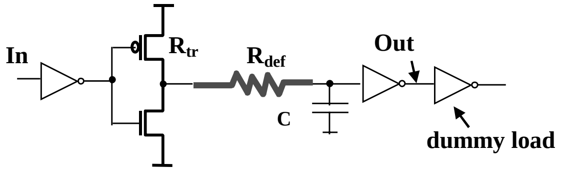

Figure 1. An example Inverter Chain

To facilitate our further discussion, two terms are defined. *Delay delta* is defined as the difference of delay between a good circuit and a defective circuit. *Delay ratio* is defined as the delay of a defective circuit over that of a good circuit. From the test point of view, a larger delay ratio means a larger signal to noise ratio. In this paper, we are using delay ratio as the metric to compare the effectiveness of test techniques.

Equation (1) shows that, given a defective circuit with a resistive open defect, the delay delta and delay ratio can be expressed by the following equations,

$$Delay\ delta = R_{def} \cdot C \tag{2}$$

$$Delay\ ratio = \frac{R_{tr}(V_{DD}) \cdot C + R_{def} \cdot C}{R_{tr}(V_{DD}) \cdot C} = 1 + \frac{R_{def}}{R_{tr}(V_{DD})} \tag{3}$$

The delay delta is constant for different values of V_{DD}. The delay ratio, on the contrary, is a function of V_{DD}. At higher voltage, the R_{tr} C term becomes smaller and the delay ratio is larger. Theoretical analysis shows that testing at a voltage higher than nominal V_{DD} is more effective than testing at nominal V_{DD}.

SPICE simulations were performed using the example inverter chain in Fig. 1. The SPICE simulations parameters are downloaded from a TSMC 0.18μm technology file [MOSIS website]. The reason for choosing this technology is that this is the most popular copper technology that is currently in use. It was shown that the duo damascene process used in the copper technology introduces open defects more frequently than old processes used in the aluminum technologies [Stamper 98].

The simulation results are shown in Table 2. Table 2(a) lists the absolute values of delay (from In to Out in Fig. 1) in ns. Every row represents a value of V_{DD}. The highest V_{DD} is 3.0V, which is 67% higher than nominal V_{DD} (1.8V). This value of high voltage is chosen so that the gate oxide electric field does not exceed the maximum non-destructive value of a good oxide [Chang 97]. The lowest V_{DD} is 1.0V, which is about twice the transistor threshold voltage (V_t=0.5V). This voltage is shown to be effective in very-low voltage (VLV) testing [Chang 96].

Every column represents a value of R_{def}. The first column lists the absolute delay values of a good inverter chain. Columns 2 to 7 list the absolute delay values of the defective inverter chain for different defect resistances. In the last column, the defect resistance is infinity. In this case, the defects become stuck opens. The inverter chain with a stuck-open defect failed in the simulations at any voltage.

Table 2(b) lists the delay delta values. As equation (2) predicts, the delay deltas don't change much with V_{DD}. Table 2(c) lists the delay ratios. As equation (3) predicts, the delay ratios increase with V_{DD}. Two things can be learned from Table 2(c). One is that delay ratio increases as V_{DD} gets higher. This means testing at voltage higher than nominal V_{DD} is more effective than testing at voltage lower than nominal voltage. The other thing is that, for stuck-open defects, the circuit fails for all voltages.

Three Inverter Chain Example

In a real circuit, there are many different paths. Figure 2 shows an example circuit with three similar inverter chains. The gray rectangles represent metal wires with wire resistance R_w. The wire capacitance is denoted as C_w. These three paths are essentially the same except for the numbers of inverters and the lengths of the metal wires. Path 1 has the longest metal wire of length 2mm, which is typically used for inter-connection between circuit blocks. Path 3 has the shortest wire of length 20μm, which is typically used for local connection. All wires are of width 0.5μm. Their corresponding resistance (R_W) and capacitance (C_W) values are calculated using parameters for metal 6 in the TSMS 0.18μm technology [MOSIS website].

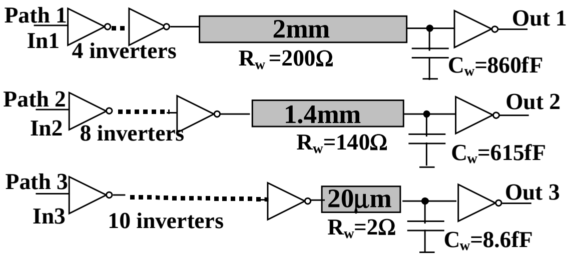

Figure 2. Three Inverter Chains

Table 2(a) Absolute delay (ns) of inverter chain (Fig. 1)

V_{DD}	Defect-free	0.5KΩ	2KΩ	8KΩ	32KΩ	128KΩ	Infinity
3.00V	0.12	0.13	0.16	0.26	0.66	2.21	Fail
2.50V	0.13	0.14	0.17	0.27	0.66	2.20	Fail
1.8V(Nominal)	0.17	0.18	0.20	0.30	0.69	2.19	Fail
1.50V (3V_t)	0.20	0.21	0.23	0.33	0.72	2.22	Fail
1.00V (2V_t)	0.38	0.38	0.40	0.49	0.92	2.48	Fail

Table 2(b). Delay delta in ns (delay with defect - delay without defect)

V_{DD}	Defect-free	0.5KΩ	2KΩ	8KΩ	32KΩ	128KΩ	Infinity
3.00V	0.00	0.01	0.04	0.14	0.54	2.09	Fail
2.50V	0.00	0.01	0.04	0.14	0.53	2.07	Fail
1.8V(Nominal)	0.00	0.01	0.03	0.13	0.52	2.02	Fail
1.50V (3V_t)	0.00	0.01	0.03	0.13	0.52	2.02	Fail
1.00V (2V_t)	0.00	0.00	0.02	0.11	0.54	2.10	Fail

Table 2(c). Delay ratio (delay with defect / delay without defect)

V_{DD}	Defect-free	0.5KΩ	2KΩ	8KΩ	32KΩ	128KΩ	Infinity
3.00V	1.0	1.1	1.3	2.2	5.5	18.4	Fail
2.50V	1.0	1.1	1.3	2.1	5.1	16.9	Fail
1.8V(Nominal)	1.0	1.1	1.1	1.8	4.1	12.9	Fail
1.50V (3V_t)	1.0	1.1	1.2	1.7	3.6	11.1	Fail
1.00V (2V_t)	1.0	1.0	1.1	1.3	2.4	6.5	Fail

Table 3 lists the SPICE simulated path delay values of these three paths (same parameters are used as last section). Their path delay is measured from their IN terminals to the OUT terminals. The path delay is the sum of gate delay and wire delay.

$$Path\ delay = Gate\ delay\ (V_{DD}) + Wire\ delay \qquad (4)$$

where the gate delay is measured from the IN to the OUT terminal of each path without the presence of wires (*i.e.*, set C_w=0, R_w=0). Gate delay is caused by transistors and therefore is a function of V_{DD}. The wire delay is obtained by subtracting the gate delay from the path delay. Wire delay can be also estimated by the product of R_w and $C_{w,}$ which are both insensitive to V_{DD}.

Table 3. Path delay of three paths in Fig. 2.

Path #	Path delay	Gate delay	Wire delay
Path1	0.47ns	0.33ns (70%)	0.14ns (30%)
Path 2	0.52ns	0.43ns (83%)	0.09ns (17%)
Path 3	0.47ns	0.47ns (100%)	0.00ns (0%)

In Table 3, path 1 has fewer inverters and a longer wire. Its wire delay accounts for 30% of the path delay. This is a *wire delay significant path,* which has wire delay than the reference path (path 2). On the contrary, path 3 has more inverters and a shorter wire. This is a *gate delay significant path,* which has larger gate delay than wire delay.

Equation (4) shows that gate delay significant paths are more sensitive to V_{DD} than wire delay significant paths. As V_{DD} drops, the path delay of a gate delay significant path increases more significantly than that of a wire delay significant path. This has an interesting implication for testing. That is, a defect located in a gate delay significant path can be more easily detected at low V_{DD} than at high V_{DD}.

Table 4 shows the path delay values obtained from SPICE simulations of the circuit of Fig. 2. Every row represents a value of power supply voltage V_{DD}. Three cases are shown. In the first case, all three paths are defect free. Path 2 is the *critical path,* which has the largest delay in the good circuit at any V_{DD}. We assume that, in the following cases, at-speed testing is performed at the maximum speed of the critical path, i.e. path 2.

In the second case, an 8KΩ resistive open is injected in path 1, the wire delay significant path, at the output of the leftmost inverter. The other two paths are defect free. The injected resistive open can be *detected* if the path delay of a defective path is larger than that of the other defect-free paths. The detected opens are indicated by boldface numbers in Table 4. The defect in path 1 can be detected at a supply voltage equal to or higher than nominal V_{DD}. However, at a supply voltage lower than nominal V_{DD}, the path delay of a defective path 1 is shorter than that of a defect-free path 2. The defect in path 1 is therefore “masked” by path 2. It is because path 1 is a wire delay significant path, which does not slow down significantly as V_{DD} drops.

In the third case, another 8KΩ resistive open is injected in path 3, the gate delay significant path, at the output of the leftmost inverter. This defect can be detected at a supply voltage lower than V_{DD} and cannot be detected at a supply voltage equal to or higher than nominal V_{DD}.

To sum up, testing at a voltage higher than nominal V_{DD} voltage is effective for resistive opens located in wire delay significant paths. Testing at a voltage lower than nominal V_{DD} is effective for resistive opens located in gate delay significant paths.

Table 4. Path delay (ns) of three cases (Fig. 2)

V_{DD}	Case 1 (good circuit)			Case 2 (defective path 1)			Case 3 (defective path 3)		
	Good Path 1 (WD*)	Good Path 2	Good Path 3 (GD*)	Defect in path 1 (WD)	Good Path 2	Good Path 3 (GD)	Good Path 1 (WD)	Good Path 2	Defect in path 3 (GD)
3.0V	0.37	0.39	0.33	**0.45**[**]	0.39	0.33	0.37	0.39	0.39
2.5V	0.39	0.42	0.36	**0.47**	0.42	0.36	0.39	0.42	0.42
1.8V (Nominal)	0.47	0.52	0.47	**0.54**	0.52	0.47	0.47	0.52	0.52
1.5V ($3V_t$)	0.55	0.63	0.58	0.62	0.63	0.58	0.55	0.63	**0.64**
1.0V ($2V_t$)	1.02	1.24	1.21	1.09	1.24	1.21	1.02	1.24	**1.27**

*WD = Wire Delay significant, GD = Gate Delay significant
**Boldface indicates the corresponding defect can be detected

2.2. Test Temperature

Transistor turn-on resistance (R_{tr}) decreases as temperature (T) gets lower. Assuming that defect resistance remains unchanged with temperature, equation (3) suggests that the delay ratio increases as temperature decreases. SPICE simulations (same setup as in Fig. 1) were performed at three different temperatures, 0, 25, and 100°C with nominal V_{DD}. These temperatures are used in the package tests in industry [Tseng 00]. Table 5(a) shows the delay ratio at different temperatures. The resistive open is assumed to be an ideal resistor, which does not change its resistance with temperature. The simulation results show delay ratio is slightly greater at 0°C.

Table 5(a). Delay ratio at different temperatures (R_{def} unchanged with T)

Temperature	Defect-free	0.5KΩ	2KΩ	8KΩ	32KΩ	128KΩ	Infinity
100°C	1.0	1.1	1.2	1.7	3.9	12.4	Fail
25°C	1.0	1.1	1.1	1.8	4.1	12.9	Fail
0°C	1.0	1.1	1.2	1.8	4.3	13.6	Fail

Table 5(b). Delay ratio at different temperatures (R_{def} changes with T)

Temperature	Defect-free	0.5KΩ	2KΩ	8KΩ	32KΩ	128KΩ	Infinity
100°C	1.0	1.1	1.2	1.9	4.8	15.8	Fail
25°C	1.0	1.1	1.2	1.8	4.1	12.9	Fail
0°C	1.0	1.1	1.1	1.8	3.9	12.3	Fail

However, if we assume that the resistive open material is metal rather than an ideal resistor, then the temperature coefficient must be taken into account. To study this effect, another SPICE simulation was performed. This simulation is similar to the last one but the resistive open material is assumed to be copper, which has a positive temperature coefficient of resistance 0.004 K^{-1} [Landolt 96]. Table 5(b) shows the delay ratio at three different temperatures. The resistance values shown are their values at 25°C. The simulation results show that the delay ratio of resistive opens increases as the temperature increases. For stuck-open defects, they could not produce correct outputs at 0, 25, or 100°C.

On the other hand, for resistive open defects consisting of negative temperature coefficient materials (such as silicide opens), cold temperature testing is better [Tseng 00]. The overall conclusion is that whether hot testing or cold testing is more effective depends on the resistive open material.

2.3. Test Patterns

Figure 3 shows the schematic of a NAND gate. There are 14 possible open defects in this NAND gate. They can be either stuck opens or resistive opens. They are marked as dx. D1 to d11 are intra-gate opens and d12 to d14 are inter-gate open. Transistors are marked as T1 to T4.

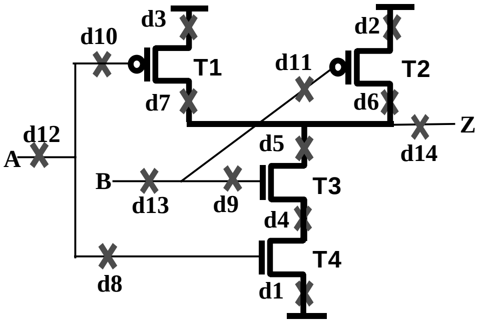

Figure 3. Fourteen open defects in a NAND gate

Table 6 shows all the effective test patterns for detecting opens in this NAND gate. There are five pattern pairs in this table and they detect all fourteen opens in the

NAND gate. There is an additional column showing the detected transition faults. The combination of test pattern pairs {1,2,3,4} or {1,3,5} detect all six transition faults in this NAND gate. They also detect all opens in this NAND gate.

Table 6. Effective test patterns and detect opens in NAND (detected transition faults also shown)

Pattern pair #	In/out [*]			Detected open defects	Detected transition. faults[**]
	A	B	Z		
1	F	S1	R	d3,d7,d10, d12,d14	Af, Zr
2	R	S1	F	d1,d4,d5,d8, d12,d14	Ar, Zf
3	S1	F	R	d2,d6,d11, d13,d14	Bf, Zr
4	S1	R	F	d1,d4,d5,d9, d13,d14	Br, Zf
5	R	R	F	d1,d4,d5,d8,d9 d12,d13,d14	Ar, Br, Zf

[*] F = Fall, R = Rise, S1=Static 1

[**] Af = A slow-to-fall fault, Ar = A slow-to-rise fault

Table 6 is applicable to both stuck-open and resistive open defects. The difference between these two defects is that circuits with resistive open defects may pass the tests at slow speed. Circuits with stuck-open defects do not pass tests even at slow speed.

Sequence Dependence of Stuck-open Defects

One interesting behavior of stuck-open defects is that they can have sequence dependent test results. A faulty circuit is said to be *sequence dependent* if the test results depend on the test patterns' ordering. For example, suppose there is a stuck-open defect in location d3 in Fig.3. This open makes one pull-up branch fail but the other pull-up branch can still work. For test pattern sequence AB = {00,11, 01} is effective to defect d3 (assuming the output Z is observed after applying the underlined pattern). However, AB = {00,01,11} is not effective because the first test pattern (00) already pulls up output Z to V_{DD}. The charges stored in the output node Z invalidate the test. This example shows a defective circuit with stuck-open defects can be sequence dependent although the good circuit is combinational.

Timing Dependence of Resistive Open Defects

It is shown in Section 2.1 that resistive opens cause signal delay. The faulty effect is transient. Chips with resistive open defects could pass the test if the test speed is very slow. Therefore, resistive open defects cause *timing dependent* defect behavior, which means the test results depend on the test timing. Transition fault test patterns are effective for resistive opens. However, the test results depend on the test speed.

Timing Dependent and Sequence Dependent

In the Murphy experiment, 25 out of 116 defective chips were found to be both *timing dependent and sequence dependent*, which means their test results are different at different test timing and their test results are also different when different reordered versions of test patterns are applied. One possible explanation for this population of chips is that a real defect can cause a combination of both stuck opens and resistive opens.

2.4. I_{DDQ} Testing

Whether stuck-open defects cause high I_{DDQ} depends on many factors, such as: (1) residual charges on the floating gate [Johnson 94]. (2) parasitic capacitors associated with the floating gate [Maly 88][Johnson 94]. (3) P/N junction reverse bias leakage current [Maly 88]. (4) floating gate topology and process technology [Champac 94]. (5) defect size [Henderson 91][Li 00]. (6) transistor pair on/off status [Hawkins 94]. Because there are so many factors, whether stuck-open defects cause high I_{DDQ} depends on individual case.

For resistive open defects, I_{DDQ} testing is not effective because the extra delay caused by defects is in the order of nanoseconds. This extra delay is too short to cause any quiescent I_{DDQ} current. The overall conclusion is that, I_{DDQ} testing is not guaranteed to be effective for stuck-open defects and hardly effective for resistive opens. [Hawkins 94] had similar conclusions.

I_{DDT} testing (measuring the transient current of the chip as a function of time) was shown to be more effective than I_{DDQ} testing in detecting resistive open defects in simulation [Kruseman 00]. In their simulation, a single NAND gate with resistive open was shown to have elevated I_{DDT} current, which is different from the I_{DDT} current of a good NAND gate. Practically, in a large circuit, a large number of gates are switching simultaneously which makes it difficult to distinguish the effect of a defect. Research in applying I_{DDT} testing for detecting resistive open defects is being carried out.

3. Experimental Results

Various experiments were performed on the 116 defective Murphy chips. Section 3.1 identifies five stuck-open suspect chips and Section 3.2 identifies one resistive open suspect chip.

3.1. Stuck Opens

In the Murphy experiment, some test patterns were applied in the following five different orders [Chang 98a]. (1) pad an all-zero pattern between every original pattern. (2) pad an all-one pattern between every original pattern. (3) reverse the original test pattern sequence (i.e. last pattern applied first). (4) pad a bit-wise complement pattern before every original pattern. (5) pad a one-bit shifted pattern before every original pattern.

The outputs were only observed at the original patterns. The experimental results show that 11 out of 116 defective chips are sequence dependent but not timing dependent. Their test results depend on the order of the patterns but not on the application speed (as long as the speed does not exceed the specified speed). These 11 sequence dependent chips are potential candidates to have stuck-open defects.

3.1.0. Boolean diagnosis

We use the stuck-open fault model to diagnose these sequence dependent chips. This diagnosis scheme is applicable for the intra-gate stuck-open defects because they can be modeled by stuck-open faults. Table 7 lists the 11 intra-gate stuck-open defects in the NAND (d1 to d11 in Fig. 3) and their corresponding stuck-open faults (in transistors T1 to T4). For inter-gate open defects (d12 to d14), which are not modeled by stuck-open faults, they have to be diagnosed by a more sophisticated technique like [Venkataraman 00].

Table 7. Intra-gate opens and their stuck-open faults

Defects	Stuck-open fault
d3,d7,d10	T1
d2,d6,d11	T2
d1,d4,d5,d8,d9	T3, T4

The following steps explain the diagnosis technique. We use the NAND gate with a stuck-open defect d3 in Fig.3 as an example. D3 can be modeled by a stuck-open fault in transistor T1.

STEP 1. SSF diagnosis. The *observed output failures* from the tester contain two pieces of information: *failing pattern addresses* and *failing pins*. All the test patterns are numbered in the order they are applied. These sequence numbers are called *pattern addresses*. The failing pattern addresses are the addresses of the test patterns at which the chip failed. The failing pins of a failing pattern are the pins that give erroneous logic values. For the NAND gate example, suppose the tester observes erroneous output values on Z twice. One failure occurs when the Lth test pattern is applied and the other failure occurs when the Nth test pattern is applied. Then the observed output failures from the tester would look like Table 8.

Table 8. Observed output failures from tester (NAND)

Failure #	Failing pattern address	Failing pin
1	L	Z
2	N	Z

After testing the chip on the tester, the observed output failures are given to a commercial SSF diagnosis tool and a list of diagnosed SSF faults are produced. The *faulty gates* are defined as the gates that contain diagnosed faults at the input or output pins. For the same NAND gate example, if the SSF diagnosis tool reports A stuck-at 1 as the diagnosed fault, then the NAND gate is the faulty gate.

STEP 2. SSF fault simulation. All the single stuck-at faults associated with the faulty gates obtained from STEP 1 are fault simulated and a single stuck-at *fault dictionary* is produced. A fault dictionary contains a list of faults and their corresponding failing pattern addresses and failing pins. Continuing from the same NAND gate example, suppose that an A stuck-at one fault is reported by STEP1, Table 9 shows the entry for the A stuck-at 1 fault in the SSF dictionary. Three failures are expected to occur when the Lth, Mth, and Nth patterns are applied if A stuck-at 1 is injected.

Table 9. A stuck-at 1 fault entry in SSF dictionary

Failure #	Failing pattern address	Failing pin
1	L	Z
2	M	Z
3	N	Z

STEP 3. Post processing. A logic simulation is performed on a good circuit for every test pattern. Logic values of all pins in every gate of the good circuit are stored in a table. For the same NAND gate example, Table 10 shows the table of logic values of all input and output pins for this NAND gate. Every row represents a test pattern applied. The whole table starts from the first pattern and ends at the last pattern. Only the test patterns of concern are shown in Table 10. From Table 6, we know that defect d3 (modeled by stuck-open fault T1) is detected by a pair of test patterns in which A falls and B remains at 1. This means that the necessary condition to detect the stuck-open fault T1 is to detect the A stuck-at 1 fault. This implies that we can construct the entry for T1 stuck-open fault in the stuck-open fault dictionary from the entry for A stuck-at 1 fault in the SSF dictionary. For every row in Table 9, we look up Table 10 and check if the stuck-open fault is detected. If so, that row is copied into the corresponding entry in the stuck-open fault dictionary. If not, that row is discarded. For the first row in Table 9, Table 10 shows that test pattern pair {L-1, L} detects the fault T1. The first row of Table 9 is therefore copied to the stuck-open fault dictionary. For the second row in Table 9, Table 10 shows that test pattern pair {M-1, M} does not detect the fault T1. The second row of Table 9 (failing pattern M) is therefore not copied to the stuck-open fault dictionary.

Table 10. Logic values of all I/O pins for NAND

Pattern address	A	B	Z
L-1	1	1	0
L	0	1	1
…	…	…	…
M-1	0	0	1
M	0	1	1
…	…	…	…
N-2	1	1	0
N-1	0	1	1
N	0	1	1

For the third row in Table 9, Table 10 shows that patterns N-1 and N are identical. (In a real diagnosis case, identical test patterns for a gate can happen because the whole circuit has more then one gate.) In this case, we go back one more cycle and check pattern N-2. Pattern pair {N-2, N-1} detects fault T1,the third row of Table 9 (failing pattern N) is copied into the stuck-open fault dictionary. The reason for doing this is that we assume the test results for stuck opens are not timing dependent. Table 11 shows the constructed entry for fault T1 in the stuck-open fault dictionary.

Table 11. T1 stuck-open fault entry in dictionary

Failure #	Failing pattern address	Failing pin
1	L	Z
2	N	Z

STEP 4. Matching test results. Now that we have the stuck-open fault dictionary and the observed output failures from the tester, we compare them and see if there is a *match* (*i.e.* an entry in the stuck-open fault dictionary is identical to the observed output failures, both failing pattern addresses and failing pins are the same). In this example, Table 8 and Table 11 match. The stuck-open fault T1 is diagnosed.

In this diagnosis experiment for Murphy chips, a 15-detect single stuck-at fault (SSF) test set, which detects every single stuck-at fault at least 15 times was applied. This test was one of the most effective test sets in the Murphy experiment. (Other test sets were applied and the diagnosis results are similar.) All its 5 reordered versions were applied at nominal voltage and at characterized speed. Five out of the 11 sequence dependent chips are diagnosed as having single stuck-open faults. Table 12 summarizes the diagnosis results. The first column shows the number of faults diagnosed by a commercial SSF diagnosis tool. The SSF diagnosis results are not perfect for these chips because their test results are sequence dependent and cannot be modeled well by single stuck-at fault model. The second column shows the number of faults diagnosed by our stuck-open fault diagnosis. The faulty gates that contain the faults are also shown. These five chips are called stuck-open suspect chips in the following text.

Table 12. Diagnosis results (stuck-open suspect chips)

Chip ID	SSF diagnosis	Stuck-open fault diagnosis	
	# of faults	# of faults	Faulty gate
1	3	1	NOR
2	1	1	NOR
3	1	1	AND+NOR
4	4	1	OR
5	4	1	AND+NOR

Regarding the other sequence dependent chips, we could not find a single entry in the stuck-open fault dictionary that match their observed output failures from the tester. However, we did find that a union of multiple entries in the fault dictionary matches the observed output failures. One possible explanation is that the defects caused multiple stuck-open faults on the other sequence dependent chips.

3.1.1. Test voltage

These five stuck-open suspect chips were further tested at several voltages: 6V (20% higher than nominal V_{DD}), 5V (nominal V_{DD}), 2.5V ($3V_t$) and 1.7V ($2V_t$). The experiment was performed at scaled speeds (vary with V_{DD}) and at room temperature. The scaled speeds were determined by shmoo experiment with 30% margin added. The test pattern set applied was the same 15-detect SSF test set (no reordering). All the test patterns were applied without aborting. At the end of testing, the total numbers of failures were counted.

The experimental results show that the numbers of failures of these five stuck-open suspect chips did not change with V_{DD}. This shows that the test results of these five stuck-open suspect chips are not voltage dependent.

3.1.2. Test speed

The five stuck-open suspect chips were tested at four different speeds: characterized speed, 1.5X slower, 3X slower and 30X slower than the characterized speed. This experiment was performed at nominal V_{DD} and at room temperature. The same 15 detect SSF test patterns were applied.

The experimental results show that the number of failures of these five chips did not change for different test speeds. This shows that the test results of the five stuck-open suspect chips are not timing dependent.

3.1.3. Test patterns

The original and reordered versions of the 15-detect SSF test patterns were applied to the five stuck-open suspect chips at characterized speed, nominal voltage and room temperature. One chip (ID#4) escaped the pad-one version (transition fault coverage 49.7%). Three chips (ID#1,2,5) escaped the pad-zero version (transition fault coverage also 49.7%). None of the five chips escaped the original and reversed versions (both have high transition fault coverages of 99.4%). The experimental results show that the transition fault test patterns are effective for detecting stuck-opens.

3.1.4. I_{DDQ} Testing

Table 13 shows the maximum I_{DDQ} values of these stuck-open suspects. For this technology, the I_{DDQ} current of a good circuit is very low. Three μA was used as the threshold in [Chang 98b]. Two out of the five stuck-open suspect chips have I_{DDQ} higher than 3μA while the rest three have I_{DDQ} current lower than 3μA. These numbers show that I_{DDQ} testing cannot effectively detect all circuits with stuck-open defects.

Table 13. Max I_{DDQ} values of stuck-open suspect chips

Chip ID	Max I_{DDQ} (μA)
1	**139.0**[*]
2	1.9
3	**19.0**
4	1.9
5	2.2

[*] boldface indicates I_{DDQ} larger than 3μA

3.2. Resistive Opens

The Murphy experimental results show that 39 out of 116 defective chips are timing dependent. These chips are potential candidates to have resistive opens.

3.2.0. Boolean diagnosis

We constructed a resistive open fault dictionary in similar way to the stuck-open fault dictionary. The only difference is that, in STEP 3 we do not go back more than one cycle if the preceding pattern (N-1) is the same as pattern N. This is because we assume that circuits with resistive open defects can pass the test pattern if we wait for more than one cycle. Although this assumption is not generally true for all resistive open defects, it is valid for our diagnosis experiment (will be verified in Section 3.2.1). For the same NAND gate example with a resistive open defect in d3, failing patterns L and M are treated in the same way. The only difference is that the failing pattern N is not copied into the resistive open fault dictionary. The constructed fault dictionary contains only the first row in Table 11.

For the diagnosis experiment, all the timing dependent chips were tested at nominal V_{DD}, room temperature, and characterized speed. We identified one chip whose observed output failures match the union of two entries (pull-up and pull-down of an inverter) in the resistive open fault dictionary. The resistive open defect could be located at the input or output pin of the faulty inverter. This chip is called resistive open suspect chip in the following text.

The matching is not perfect. There are a few failing patterns (and failing pins) in the fault dictionary that are not observed on the tester. This could be because the delay delta is so small that the fault can only be observed from the primary outputs through long paths but not short paths [Tseng 01].

3.2.1. Test speed and voltage

A shmoo experiment was performed on this resistive open suspect chip. The shmoo plots of a good chip and the resistive open suspect chip are both shown in Fig. 4. The X-axis is the V_{DD} and the Y-axis is the minimum clock cycle time, which is the reciprocal of the circuit speed. From this figure, it can be seen that the defective circuit is about 10ns slower than a good circuit. This delay delta value remains approximately unchanged from 6V to 2V. This chip escaped very-low-voltage (VLV) testing at 1.7V. It also escaped slow speed tests at nominal voltage. It was only detected by at-speed tests at nominal voltage.

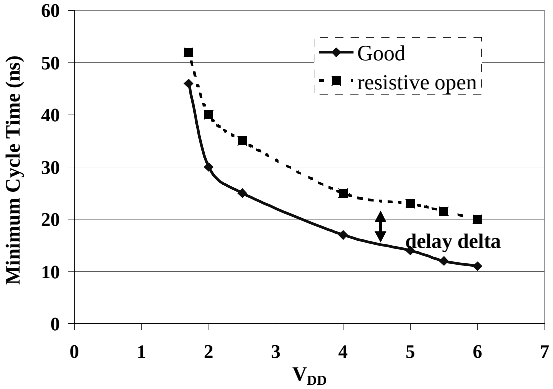

Figure 4. Shmoo plot (good vs. resistive open)

This shmoo plot also confirms our previous assumption in Section 3.2.0 that circuits with resistive open defects can pass the test if we wait for more than 1 cycle. Figure 4 shows that the good circuit has a minimum cycle time of 12 ns at nominal V_{DD} (5V) and the defective chip has a minimum cycle time of 22ns. If the chip is tested at a clock period of 12ns, the detective chip fails the test (12ns < 22ns). If we double the test clock cycle time from 12ns to 24ns, the defective chip can pass the test (24ns > 22ns).

Table 14 lists the delay ratio of this resistive open suspect chip. The numbers are calculated from the shmoo plot in Fig. 4. This table shows that the delay ratio of the resistive open suspect chip decreases as V_{DD} decreases. This is consistent with our SPICE simulation for the resistive opens (see Table 2(c)). It was shown that, for the other defects (such as gate oxide shorts, metal shorts, weakly driven gate, threshold voltage shift), the delay ratio increases as V_{DD} drops [Chang 96]. Table 14 shows that the experimental result of this resistive open suspect chip matches simulation results of a resistive open defect rather than other that of other defects in [Chang 96].

Table 14. Delay ratio of resistive open suspect chip

V_{DD}	Delay ratio
1.2x Nom. (6V)	1.8
1.1x Nom. (5.5V)	1.8
Nominal (5V)	1.8
$3V_t$ (2.5V)	1.4
$2V_t$ (1.7V)	1.1

Notice that in Fig. 4, the delay delta is smaller than 10ns at 1.7V. One possible reason is that, for a good chip, the critical path changes from 5V to 1.7V. To prove this argument, one special shmoo experiment was performed on the good circuit. In this shmoo, the test speed keeps increasing until the first failure occurs. The experimental result shows that the failing pattern addresses and failing pins at 1.7V are different from that at 5V. This shows that the critical path of a good circuit at 1.7V is different from that at 5V.

3.2.2. Test Pattern

This resistive suspect chip was detected by all reordered versions of the 15-detect SSF test sets at characterized speed. This chip escaped all tests at one third of the characterized speed. The experimental results show that this resistive open suspect chip is timing dependent.

3.2.3. I_{DDQ} Testing

This circuit has a maximum I_{DDQ} value of only 1.8μA, which is below the 3μA threshold. This result shows that, as expected, I_{DDQ} testing is not effective in detecting this resistive open suspect chip.

4. Summary

The effect on test results of three test conditions (supply voltage, speed, and temperature) for detecting stuck-open and resistive open defects are evaluated. The conclusions are: transition fault test patterns are effective for both defects. At-speed tests are effective for resistive open defects. Changing other test conditions, such as test temperature and supply voltage, could be effective for resistive open defects but some knowledge about the material and location of opens has to be known in advance.

Diagnosis schemes for stuck-opens and resistive opens are presented. Five stuck-open suspect chips and one resistive open suspect chip are identified. Table 15 summarizes their experimental results. The first five chips are sequence dependent, but neither timing dependent nor voltage dependent. Some of them have high I_{DDQ} current while others don't. Their behaviors match the expectation of stuck-open defects. The last chip is timing dependent and voltage dependent. It has low I_{DDQ}. Its behavior matches the expectation of a resistive open defect.

Table 15. Summary of stuck and resistive open chips

Chip ID	TD?*	VD?*	High I_{DDQ}?	Suspect defect
1	N	N	Y	Stuck open
2	N	N	N	Stuck open
3	N	N	Y	Stuck open
4	N	N	N	Stuck open
5	N	N	N	Stuck open
6	Y	Y	N	Resistive open

*TD = Timing Dependent, VD=Voltage Dependent

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Appendix D.

Diagnosis of Sequence Dependent Chips

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Diagnosis of Sequence-dependent Chips

James C.-M. Li and E.J. McCluskey
Center for Reliable Computing, Stanford University
cmli,ejm@crc.Stanford.edu

Abstract

A technique capable of diagnosing single and multiple stuck-open and stuck-at faults is presented. Eleven sequence-dependent chips (test results depend on the order of test patterns) are diagnosed. Seven of them are diagnosed as having single stuck-open faults. Two of them are diagnosed as having multiple stuck-at and stuck-open faults.

1. Introduction

In the Murphy experiment [McCluskey 00], eleven out of 116 defective chips are found to be *sequence-dependent* but not *timing dependent*. Their test results depend on the order of the patterns but not on the application speed (as long as the speed does not exceed the specified speed). The purpose of this paper is to diagnose these 11 sequence-dependent chips. This is the first paper that shows experimental diagnosis results based on the stuck-open fault model. This is also the first paper that experimentally shows how *timing skew* affects the test effectiveness of stuck-open faults. Timing skew is the uncertainty of relative timing of two changing signals [McCluskey 62].

A stuck-open (SOP) fault in a CMOS gate G is defined as a permanent failure that leaves one transistor in G in a non-conducting state. Figure 1 shows a NAND gate and its four stuck-open faults. Wadsack showed that circuits with stuck-open faults have sequential test results [Wadsack 78]. The following example illustrates how a defective NAND gate with stuck-open faults can be sequence-dependent. Suppose that a stuck-open fault T1 occurs in the NAND gate. This fault makes one pull-up branch fail but the other pull-up branch can still work. Test pattern sequence AB = {00,11, $\underline{01}$} can detect T1 (faulty output sequence = {1,0,$\underline{0}$}, fault detected at the underlined pattern). However, AB = {00,$\underline{01}$,11} is not effective (faulty output sequence = {1,$\underline{1}$,0}, same as correct output sequence). Because the first test pattern (00) already pulls up output Z to V_{DD}, the charge stored in the output node Z invalidates the test. (For detecting stuck opens with transition fault test set, please see [Li 01] [Cox 88])

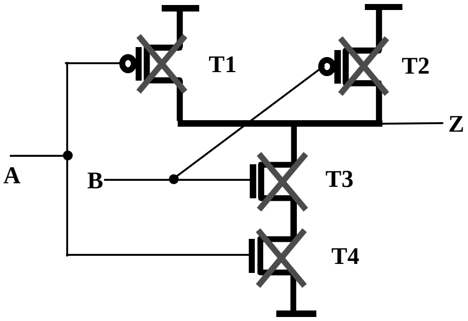

Figure 1. Four stuck-open faults in NAND gate

Stuck-open fault simulation techniques were presented in [Konuk 96] and [Barzilai 86]. No experimental results were shown. Other diagnosis techniques for opens can be found in [Venkataraman 00][Hora 01]. Hora and Venkataraman's work were based on single stuck-at fault simulations and did not take sequence dependence into account.

A stuck-open diagnosis technique based on the stuck-open fault model was presented in [Li 01]. This technique is capable of diagnosing faulty combinational circuits that have sequence-dependent test results. In this paper, the diagnosis technique is improved to diagnose both single and multiple faults. The fault model can be either stuck-open fault or stuck-at fault. This technique is applied to eleven sequence-dependent Murphy chips.

The Murphy chips were fabricated in 0.7μm technology [McCluskey 00]. The total gate count is 25K. There are five types of designs on it. Two of them are datapath circuits, the others are control logic. All five designs are combinational circuits. The total number of inputs of these five designs is 108 and total number of outputs is 54.

Our diagnosis technique is a logic-level diagnosis scheme. We simulate the behavior of stuck-open faults based on the schematic information provided by the manufacture's data book [LSI 93]. As long as the Murphy chips are actually implemented in the way that is specified in the book, our logic-level modeling of the stuck-open fault is correct and the diagnosis results are valid. Also notice that stuck-open faults can be caused by various physical defects such as missing contacts or bad transistors. Our diagnosis technique reports faults based on their faulty behavior. The actual defects cannot be known unless a physical failure analysis is performed.

The organization of this paper is as follows. Section 2 shows the diagnosis flow. Section 3 shows the diagnosis results. Section 4 concludes the paper.

2. Diagnosis Flow

Figure 2 shows the overall diagnosis flow. Each step in this figure will be described in detail in the following subsections. To facilitate our discussion, we use a combinational circuit (Fig. 3) that has a stuck-open fault T1 in a NAND as an example. In this figure, PI stands for primary inputs and PO stands for primary outputs. CL stands for combinational logic.

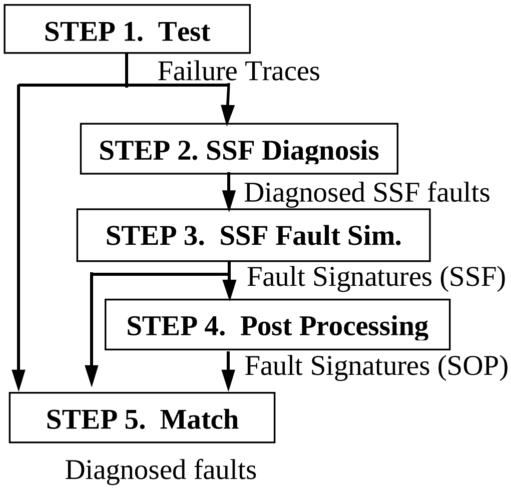

Figure 2. Diagnosis Flow

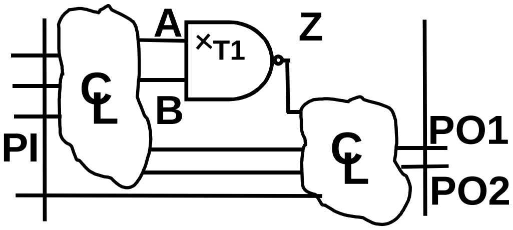

Figure 3. Example circuit

STEP 1. Test

Defective chips are tested on the tester and their *failure traces* are recorded. The failure traces (FT) from the tester contain two pieces of information: *failing patterns* and *failing pins*. The failing patterns are the PI patterns at which the chip failed. The failing pins of a failing pattern are the primary output pins that give erroneous logic values. For the faulty NAND example, suppose the tester observes erroneous output values twice: one failure occurs when the test pattern L is applied and the other failure occurs when the test pattern N is applied. The failures occur at primary output pins PO1 and PO2 respectively. The failure traces from the tester would look like Table 1.

Table 1. Failure traces from tester

Failing pattern	Failing pin
L	PO1
N	PO2

STEP 2. SSF diagnosis.

After testing the chip on the tester, the failure traces are given to a commercial SSF diagnosis tool and a list of diagnosed SSF faults are produced. The *faulty gates* are defined as the gates that contain diagnosed faults at the input or output pins. For the same example, if the SSF diagnosis tool reports that the input A of the NAND gate has a stuck-at 1 fault, then the NAND gate is the faulty gate.

STEP 3. SSF fault simulation.

All the single stuck-at faults associated with the faulty gates obtained from STEP 2 are fault simulated (with the test patterns applied on the tester) and their *fault signatures* (FS) are produced. Fault signatures of a fault are the failing patterns and the failing pins obtained from fault simulation with the fault injected. Continuing with the same NAND gate example, Table 2 shows the fault signatures of the A stuck-at 1 fault. Three failures are predicted to occur when test patterns L, M, and N are applied if a stuck-at one fault is present on lead A.

Table 2. Fault signatures for A stuck-at 1 fault

Failing pattern	Failing pin
L	PO1
M	PO2
N	PO2

STEP 4. Post processing.

In this step, we want to obtain the fault signature for SOP faults from the fault signature for stuck-at faults. Before that, we need two tables: the *Excitation Condition*

(EC) table and *Gate Input Sequence* (GIS) table. They will be described in detail as follows.

Table 3 shows the excitation condition for a T1 stuck-open fault. The first input is an *initialization pattern* that sets up the NAND gate for exciting the fault. The second input is a *strobe pattern* after which the output is observed.

Table 3. Excitation condition for SOP fault T1

A	B	Comment
1	1	Z=0, initialize pattern
0	1	Z=1, strobe pattern

For every type of gate, we make an *Excitation Condition* (EC) table. The EC table for a certain gate contains the gate input pair to excite the stuck-open faults in the gate. Table 4 shows an EC table for NAND gates. Every row shows a gate input pair and the excited stuck-open fault. For example, the first row of this table means that the gate input pair "A falls and B remains static one" excites stuck-open fault T1. The EC table is made based on the schematic information provided by the manufacture [LSI 93]. For a gate with three or more inputs, the EC table is created in the similar way.

Table 4. EC table for NAND

A*	B	Excited faults
F	S1	T1
S1	F	T2
R	S1	T3,T4
S1	R	T3,T4

* F = Fall, R = Rise, S1=Static 1

A fault-free logic simulation is performed on a good circuit to obtain a *Gate Input Sequence* (GIS) table, which lists the input values of the faulty gates (diagnosed from step 2) for every test pattern that is applied on the tester. For the same NAND gate example, Table 5 shows the GIS table for this particular NAND gate. Every row represents a test pattern applied. The gate output Z is also shown for reference. Only the test patterns L, M and N are shown here for illustration purpose. (In our implementation, the GIS table is stored statically in memory. There is no insufficient memory problem for our circuits. For bigger circuits, this implementation could cause memory problems. We might need to generate the GIS table dynamically to save memory.)

Table 5. GIS table for NAND in Fig. 3

Pattern	A	B	Z
(starting from 1)			
…			
L-1	1	1	0
L	0	1	1
…	…	…	…
M-1	0	0	1
M	0	1	1
…	…	…	…
N-2	1	1	0
N-1	0	1	1
N	0	1	1
…			

Now that we have the EC table and GIS table, we can convert the SSF fault signatures (SSF-FS) to the SOP fault signatures (SOP-FS). For every failing pattern in SSF-FS, we check its previous pattern and see if any stuck-open fault is excited. If so, the failing pattern and failing pin is copied into the corresponding SOP-FS. If not, the failing pattern and failing pin is discarded.

For example, pattern L is the first failing pattern of SSF-FS in Table 2. The GIS table shows the input A has a falling transition and input B keeps static one. According to the first row of the EC table (Table 4), stuck-open fault T1 is excited by pattern pair {L-1, L}. The propagation of the faulty effect is guaranteed by the SSF fault simulation (STEP 3). The T1 stuck-open fault is therefore detected by pattern pair {L-1, L} and the first row of Table 2 is copied to the SOP-FS for T1 (see Table 6). For the second row in Table 2, the EC table (Table 4) shows that pattern pair {M-1, M} does not excite any SOP fault. The second row of Table 2 is therefore not copied to any SOP-FS.

For the third row in Table 2, the GIS table (Table 5) shows that, for pattern N-1 and N, the gate inputs to NAND are identical. (The fault is not detected by pattern N-1 because the fault effect was not propagated to the PO in pattern N-1). In this case, we go back one more pattern and check gate inputs of pattern pair {N-1, N-2}. For pattern pair {N-2, N-1}, the gate inputs excite fault T1 so the third row of Table 2 is copied to the SOP-FS for T1. This is because we assume the charge stored at NAND gate output Z hold for two continuous cycles. This assumption is valid as soon as we do not test the chip with an extremely slow speed. (In this experiment, the test pattern is applied at a speed of 1MHz.) Table 6 shows the constructed SOP-FS for fault T1.

Table 6. Fault signatures for stuck-open fault T1

Failing pattern	Failing pin
L	PO1
N	PO2

STEP 5. Match.

Figure 4 shows the relation between the fault signatures (FS) of a certain fault and the failure traces (FT) from tester. A *failing element* is a failing pattern and a failing pin. Those failing elements that are in the fault signatures and in the failure traces from the tester belong to the category of *intersection*. The number of failing elements in intersection is denoted as I. Those failing elements that are found only in fault signatures but not in the failure traces belong to the category of *Simulation Only*. Those failing elements that are found only in the failure traces but not in the fault signatures belong to the category of *Tester Only*. The numbers of failing elements belonging to these two groups are denoted as SO and TO respectively.

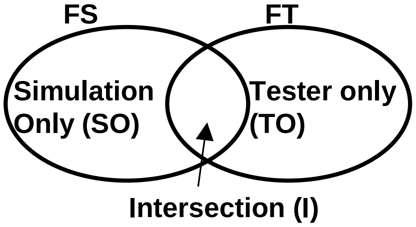

Figure 4. Relationship between FS and FT

In this matching step, we are using two scores to represent how well the fault signatures (of a certain fault) match the failure traces, the *prediction score* and *matching score* [Hora 01]. The prediction score (P) is defined as the number of failing elements in the intersection (|I|) over the number of failing elements in the fault signatures(|FS|). *i.e.*,

$$Prediction\ Score\ (P) = \frac{|I|}{|FS|} \times 100 \tag{1}$$

The matching score (M) is defined as the number of failures in the intersection (|I|) over the number of failing elements in the failing traces (|FT|), *i.e.*,

$$Matching\ Score\ (M) = \frac{|I|}{|FT|} \times 100 \tag{2}$$

A *perfect match* happens if the fault signatures (FS) of a particular fault and the failure traces (FT) are identical. The matching score is 100 and the prediction score is also 100.

Another possible match outcome is P score = 100 but M score less than 100. All the fault signatures are observed on the tester but there remain some failure traces that are not predicted. A possible explanation is that the fault under diagnosis is one of multiple stuck-at or stuck-open faults. (see Chips 6,7 for the discussions of other possible explanations) To account for this case, the following matching steps are implemented.

Step 5-1. The fault signatures of every SSF and SOP fault are matched with the failure traces. An M score and a P score are assigned to every fault. We pick a fault with the highest P score. (If two faults are tied with equal P scores, we pick the one with the highest M score.) If the fault has both P and M scores equal to 100, then the matching process is finished. In the NAND gate example, Table 1 and Table 6 are identical. We have a perfect match for the T1 stuck-open fault.

Step 5-2. If there is no perfect match, pick another fault from the rest of the fault list which has the highest P score (If two faults are tied with equal P scores, we pick the one with the highest M score). Add the FS of that chosen fault to the FS of the previous fault to form a new FS. (The adding process removes the overlapped failing pin and failing patterns in case two faults have the same failing pins in the same failing patterns.) The P and M scores of this new FS are then calculated by equation (1) and (2) respectively.

Step 5-3. Match the new FS with the FT and see if the M score increases. Repeat steps 5-2 and 5-3 until we have a perfect match or there are no more faults that can improve the score.

3. Experiment Results

In the Murphy experiment, some test patterns were applied in the following five different orders [Chang 98]. (1) insert an all-zero pattern between every original pattern. (2) insert an all-one pattern between every original pattern. (3) reverse the original test pattern sequence (i.e. last pattern applied first). (4) insert a bit-wise complement pattern before every original pattern. (5) insert a one-bit shifted pattern before every original pattern.

The outputs were only observed at the original patterns. The experimental results show that 11 out of 116 defective chips are sequence-dependent but not timing dependent. Their test results depend on the order of the patterns but not on the application speed (as long as the speed does not exceed the specified speed). These 11 sequence-dependent chips are potential candidates to have stuck-open faults.

In this diagnosis experiment for Murphy chips, a 15-detect single stuck-at fault (SSF) test set, which detects every single stuck-at fault at least 15 times was applied. This test was one of the most effective test sets in the Murphy experiment. (We also applied other test sets. See section 3.5 for discussions)

3.1. Chips 1 to 5

Five out of the 11 sequence-dependent chips were diagnosed as having single stuck-open faults. Table 7 summarizes the diagnosis results. The first column shows the number of faults diagnosed by a commercial SSF diagnosis tool. The SSF diagnosis does not match perfectly because their test results are sequence-dependent. The second column shows the number of faults diagnosed by our stuck-open fault diagnosis. They all match completely. The faulty gate types that contain the stuck-open faults are also listed.

Table 7. Diagnosis results (Chips 1 to 5)

Chip ID	SSF diagnosis	Stuck-open fault diagnosis		
	# of faults (uncollapsed)	# of faults	Score M/P	Faulty gate
1	3	1	100/100	NOR
2	1	1	100/100	NOR
3	1	1	100/100	AOI
4	4	1	100/100	OR
5	4	1	100/100	AOI

3.2. Chips 6 and 7

In chip 6, a stuck-open fault in T1 in a NAND gate had the highest scores. Its P scores were 100 but M scores were not 100. This means there existed some tester-only failure traces. After examining the failure traces of chip 6, it was found that tester-only failure traces occurred when gate input pair AB is {10,01}. This could be explained by a *static hazard* caused by timing skew of gate inputs A and B. A static hazard is present if it is possible for a temporary change of output to occur in response to an input change that does not cause the steady state output to change [McCluskey 86].

Figure 5 shows how timing skew affects the excitation of stuck-open faults. Assume that we have a stuck-open fault in T1 in the NAND gate in Figure 1 and we have a gate input pair AB = {10,01}. In case (i), the A input falls first and then B input rises later. The output Z can be kept at logic one due to the parasitic capacitor holding the charges at the faulty gate output. In this case, the stuck-open fault cannot be detected. In case (ii), input B rises first and output A falls later. For a good NAND gate, the output Z is pulled down momentarily and then pulled back up again (*i.e.*, static-one hazard). For a defective NAND gate, the output Z is pulled down but cannot be pulled back to one due to the stuck-open fault T1. In this case, the stuck-open fault could be detected (as long as the faulty effect is propagated properly). This could explain why chip 6 failed the gate input pair AB = {10,01}.

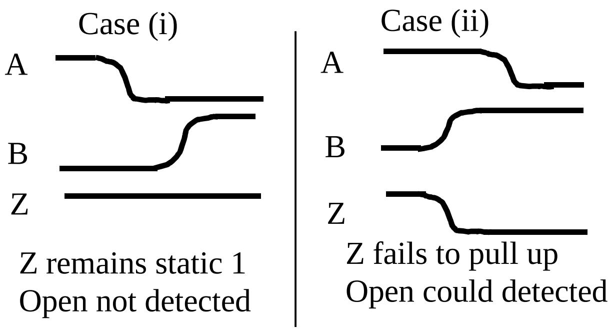

Figure 5. Two cases of timing skew

[Reddy 83] described how timing skew effects the detection of stuck-open faults but no experimental data were shown. In our experiment, it is observed that the opposite gate input sequence, AB ={01,10}, did not excite the stuck-open fault. This experiment shows that timing skew does affect the test effectiveness for stuck-open faults.

To take this timing skew problem into account, we added one entry, AB = {10,01}, to the EC table for NAND gate as an additional gate input pair for exciting the stuck-open fault in T1. After making this modification, the fault signatures of the stuck-open fault in the NAND gate perfectly match the failure traces of chip 6. The diagnosis result of chip 6 is shown in Table 8. The SSF diagnosis gave 40 faults but our stuck-open fault diagnosis gave only one fault.

For chip 7, we found a similar timing skew problem for an OAI gate. After making the similar modification to the EC table, the stuck-open fault diagnosis gives perfect match results (compared with SSF diagnosis which gave 10 faults).

Table 8. Diagnosis results (Chip 6 &7)

Chip ID	SSF diagnosis	Stuck-open fault diagnosis (modified EC table)		
	# of faults (uncollapsed)	# of faults	Score M/P	Faulty gate
6	40	1	100/100	NAND
7	10	1	100/100	OAI

3.3. Chips 8 and 9

For chip 8, multiple faults were diagnosed. One of them is a single stuck-at fault in a NAND gate. The other fault is a stuck-open fault in an OR gate. These two faults are present at the same time. The P and M score of the combination of the fault signatures of these two faults are 100 (see step 5-2). The diagnosis result for chip 8 is shown in Table 9. Compared with the SSF diagnosis which gives 37 faults, our diagnosis gives a perfect match result with the combination of two faults.

Table 9. Diagnosis results (Chip 8 & 9)

Chip ID	SSF diagnosis	Stuck-open fault diagnosis		
	# of faults (uncollapsed)	# of faults	Score M/P	Faulty gate
8	37	2	100/100	NAND (SSF) OR (SOP)
9	20	3	63/100	NAND (SSF) OAI (SSF) OAI (SOP)

For chip 9, one single stuck-open fault was identified. The faulty gate is an OAI gate and the matching score was 53. Besides this SOP fault, there are two single stuck-at faults identified. Each one of them had matching score of 5. These three faults are supposed to present at the same time. The union of these three faults gave a matching score of 63 and prediction score of 100. Although the matching was not perfect, this is the highest score we have so far.

The multiple faults presented in chips 8 and 9 are in different logic cones. Their failing pins and failing patterns are all different. So we do not have to consider the multiple fault cancellation effects.

3.4. Chips 10 and 11

For chips 10 and 11, we could not find any stuck-open fault or stuck-at fault that has a P score or M score of 100. Our diagnosis was not successful.

One possible reason for this unsuccessful diagnosis is that the defects are not well modeled by stuck-at or stuck-open fault models. This could be because the defects are large in area or the defects are clustered [Koren 94].

Other possible explanation can be non-inverting feedback bridging faults (NFBF). Mei showed criterion for test patterns to detect NFBF [Mei 74]. However, so far we cannot find a good match between the experimental data with Mei's theorem. Feedback bridging faults can also be detected by I_{DDQ} testing [Rajsuman 94] [Gulati 93]. The max I_{DDQ} of chip 9 is 2,620 μA and the max I_{DDQ} of chip 10 is 2,740 μA. But we could not find the same I_{DDQ} behavior as in the simulations of Rajsuman. Gulati's showed failure analysis results without presenting any diagnosis technique.

A third possibility could be that some of the library cells were not implemented exactly in the same way as is shown in the databook. In this case, our simulated fault signatures could be invalid and therefore fail to find a good match with real data.

3.5 Other test sets

We did the same experiment using a SSF test set with 98% fault coverage. This imperfect fault coverage is chosen on purpose to evaluate our diagnosis technique in a real life situation. The diagnosis results are the same except for chip 2. This chip escaped the 98% SSF test set so no failure traces were observed.

4. Conclusions

A technique for diagnosing single and multiple stuck-at and stuck-open faults is presented. Seven out of the eleven sequence-dependent Murphy chips are diagnosed to have single stuck-open faults. Two chips are identified to have multiple stuck-open and stuck-at faults. The other two chips are not successfully diagnosed and the possible reasons are discussed.

Our experimental data also show that timing skew does effect the detection of stuck open faults. We achieve a perfect diagnosis match by taking this timing skew into account.

Several attempts have been made to perform failure analysis on these Murphy chips. Unfortunately, these efforts failed due to insufficient layout information. However, the same technique is being applied to our next generation of test chips

(ELF35) [Li 99]. Hopefully we can perform failure analysis on the ELF35 chips in the future.

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