Comparisons of Various Scan Delay Test Techniques

Center for Reliable Computing
Stanford University
December 2005
Task ID: 1175.001
Donghwi Lee and Edward J. McCluskey

Abstract

Chips that produce correct results under operating conditions are called *good chips*. Some good chips may fail structural tests applied via scan chains (also called *overkill chips*). A reduction in supply voltage (also called *supply voltage droop*) due to the resistance of power-ground network is called *IR-drop*. IR-drop is investigated as a potential cause of overkill. IR-drop may slow down the speed of a chip unnecessarily, which could result in failing the structural test even though the chip could operate correctly in normal operation (i.e., overkill). In order to reduce the switching activity, test patterns can be generated such that don't-care bits are filled with the last significant bit (also called *repeat-fill test patterns*). Our experiments show that repeat-fill test patterns reduce the occurrence of overkill by 58%, but increase the number of test escapes by 50%.

A new technique to reduce potential overkill due to IR-drop is presented. Compared to the normal transition delay test set, the proposed technique was able to reduce the occurrence of overkill by 25% without increasing test escapes. The proposed test set has the same number of patterns as the normal transition delay test set while the repeat-fill test set has 2.3 times larger in test set length compared to the normal transition delay test set. Test time of proposed technique is 1.3 times longer than test time of the normal transition delay

test set. In the repeat-fill test set, test time is 2.3 times longer than test time of the normal transition delay test set.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1 Introduction

1.1 Sources of overkill

Chips that produce correct results under operating conditions (also called *good chips*) may fail structural tests applied via scan chains (also called *overkill*). There are three main sources of overkill: (1) multi-cycle paths, (2) long false paths, and (3) excessive switching activities.

1. *A multi-cycle path* is a path that requires two or more clock cycles to propagate a response and to capture it at the scan flip-flops [Saxena 02]. During normal operation, it is guaranteed by design that the contents of the destination flip-flops of multi-cycle paths are sampled only at appropriate times. However, in test mode, the destination flip-flops of multi-cycle paths may be sampled at incorrect times. Therefore, the multi-cycle paths may cause overkill. Figure 1 illustrates the multi-cycle path example.

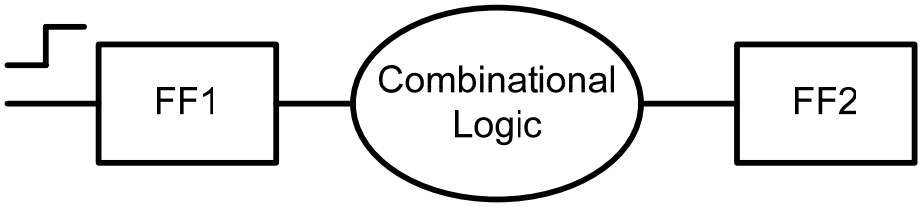


Figure 1 Multi-cycle path - example

Let's suppose a path given in Figure 1 is a 2-cycle path. The 2-cycle path requires 2 cycles for a signal to propagate from FF1 to FF2. In transition delay testing, a transition at the starting flip-flop (FF1) is made at cycle *n*, and the response of the circuit is captured at the destination flip-flop (FF2) at cycle *n+1*. However, a transition does not necessarily propagate to FF2 at cycle *n+1* because this path is 2-cycle path. If the correct output is captured at FF2 at cycle *n+2* but not at *n+1*, transition delay test causes overkill.

2. *A false path* is a path that cannot be sensitized during normal operation. A path that can be sensitized during normal operation is called a *valid path*. A false path whose delay is greater than the system clock period is called a *long false path*. In scan-based transition delay testing, some test patterns could sensitize the long false paths.

In this case, transitions propagated along the long false paths may not have the expected logic values because the test is applied with the system clock, whose period is smaller than the delay of long false paths [Kim 03]. Therefore, long false paths may cause overkill.

Overkill could be a chip with a defect. For example, a chip with a defect on a false path could still operate correctly in a system because this defect is not sensitized in a system. However, this chip could fail a scan-based transition delay test if it sensitizes and tests a false path. Figure 2 exemplifies a portion of a chip that contains three paths crossing at a node P.

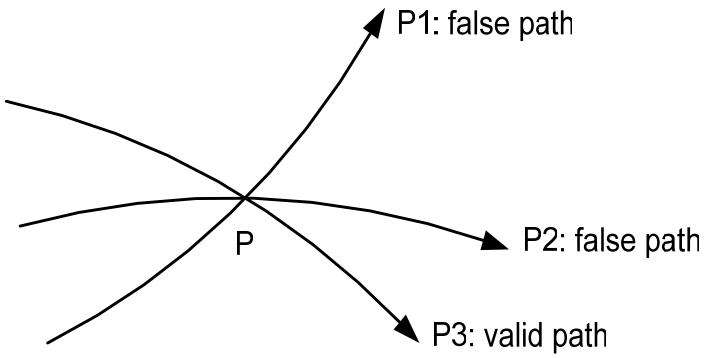


Figure 2 Long false path - example

Let's assume P1 and P2 are false paths and P3 is a valid path. We will also assume that this circuit operates at a 10ns clock period. We will first consider how overkill could occur with the presence of defects at a node P. Delays of three paths are given in Table 1.

Table 1 Delay of paths a defect

Path	Delay (ns)	
	Defect-free circuit	2ns of delay defect at node P
P1	9	11
P2	6	8
P3	7	9

Structural delay test pattern could test a delay defect at node P through P1, which is a false path. It would cause overkill because delay through this false path is greater

than 10ns (Note that P1 is a long false path because its delay is greater that the system clock period). However, the delay defect tested through P2 will not cause overkill because delay through this false path is smaller than 10ns. Hence, false path sensitization does not always result in overkill. If a node P is stuck at 0 or 1, overkill would not occur even if node P is tested through a long false path because node P would also cause a valid path (P3) to fail the test. The node P stuck at 0 or 1 would cause overkill if there is no valid path crossing the node P. However, it is difficult to guarantee that paths containing a defective node are all false paths and no valid paths go through that defective node.

Overkill could also occur without the presence of defect. Let's consider paths in Figure 2 again. Delays of paths are given in Table 2. In this example, delays at nominal Vdd will be considered.

Table 2 Delay of paths without a defect

Path	Delay (ns) at nominal Vdd	Delay (ns) at 75% of nominal Vdd due to voltage droop
P1	11	14
P2	12	15
P3	7	11

We will assume that the system clock period is 10ns. P1 and P2 are long false paths, whose delay is greater than system clock period. If P1 or P2 is tested by a structural delay test, this chip will fail the test. However, this is good chip because the delay of the valid path P3 is smaller than system clock period. Therefore, overkill could happen.

3. Excessive switching activity of test patterns may also cause overkill. Supply voltage droop due to the resistance of power-ground network is called *IR-drop* [Saxena 03]. This happens when large current flows in a chip. When scanning in test vectors, large amount of nodes toggle at the same time. This may result in current spikes which are usually higher than the currents during functional operation. As a result of current spikes, power supply voltage could drop below the normal operation range. This fluctuation of power supply voltage degrades the speed of a CUT. Therefore, a good chip could fail the structural test depending on the amount of

switching activity of test patterns [Saxena 03]. Let's consider delays of paths given in Table 2 again. The last column presents the elongated delays of paths due to supply voltage droop. If the structural test set contains excessive switching activity such that the paths given in Figure 2 suffer from IR-drop, this test set would test the delays presented at the last column. In this case, testing valid path P3 could cause overkill because the delay of P3 under the voltage droop is greater than the system clock period. Note that excessive switching activity of test patterns may cause overkill although test patterns test only valid paths. Hence, the optimum switching activity of structural test patterns should be determined to minimize overkill.

1.2 Outline

This report is organized as follows.

Section 2 presents the NVIDIA test chips used for this project.

Section 3 presents two test flows used for this project. Various structural test conditions are also presented in detail.

Section 4 presents the classification of our test samples. Based on various structural tests we applied, we classified the test chips into four categories: (1) structural test escapes, (2) weak suspects, (3) rated-speed failures, and (4) slow-speed failures. All categories are further classified into overkill candidates and defective chips except structural test escape. This section provides criteria for the classification in detail.

Section 5 presents the experimental results on transition delay test sets with various switching activities. Two possible physical mechanisms of how excessive switching activity of test patterns could cause overkill are discussed with the SPICE simulation results. Flowchart of implementing the proposed transition fault delay test sets are discussed in detail. Experiments were applied to overkill candidates to support the proposed method. Experiments were also applied to defective chips in order to investigate the impact on the test quality degradation. Correlation between the switching activity and delay size is also presented.

This report concludes with Section 6.

2 Test Chip

This section presents the test chip used in the experiments. Table 3 presents the characteristics of the test chips.

Table 3 Characteristics of test chips

Test chip	Feature size of the Technology	Number of logic gates	Number of Flip-Flops	Number of Clock Domains	Number of I/Os
ELF13	0.13μm	7.2 million	NA	>10	>100

ELF13 is a NVIDIA's graphics processor using 0.13μm technology. It has 7.2 million logic gates and more than 10 clock domains. The nominal supply voltage is 1.355V. The design has several hundred I/Os.

3 Test flows

The test flow to collect the ELF13 samples and perform experiments is split into two flows: (1) the production test flow and (2) the experiment test flow. The production test flow is used to collect the test chip samples. After collecting the samples, we applied various tests according to the experiment test flow in order to categorize the test chip samples.

3.1 Production test flow

Figure 3 presents the production test flow.

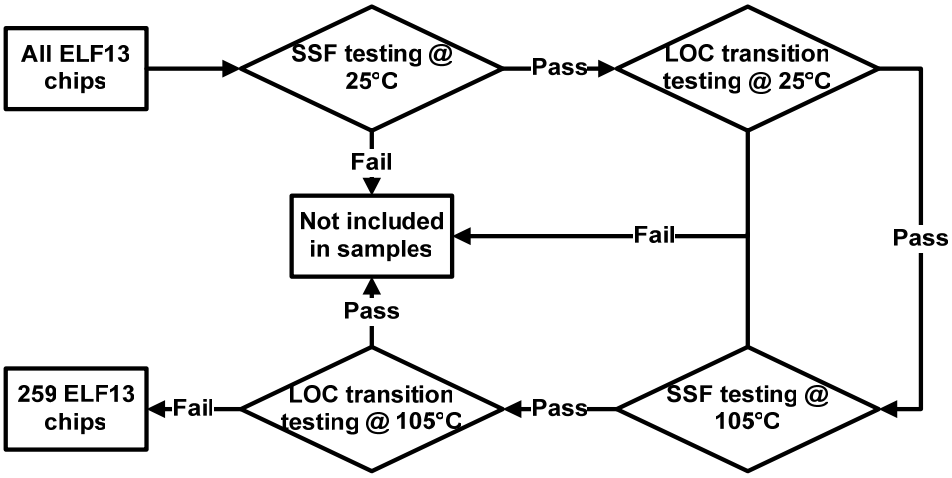


Figure 3 Production test flow

NVIDIA selected 259 ELF13 chips using the production test flow. Chips that failed structural tests at room temperature were not included in our samples because NVIDIA assumes that they would only contain small number of potential overkill chips.

3.2 Experiment test flow

More structural test sets were applied to those 259 chips using our experiment test flow in order to characterize them. Figure 4 presents the experiment test flow.

All the structural tests were applied at room (25°C) and hot (105°C) temperatures while SLT and functional test were only applied at room (25°C) temperature. Table 4 presents the test conditions applied in the experiment test flow in detail.

2-detect test patterns were applied at three different supply voltages to investigate the voltage dependent defects: low *Vdd (0.9V)*, nominal *Vdd (1.355V)*, and high *Vdd (1.6V)*.

Low voltage value was selected under the following criteria: (1) this value should not cause good chips to fail and (2) this value should not cause chips to fail during scan data loading.

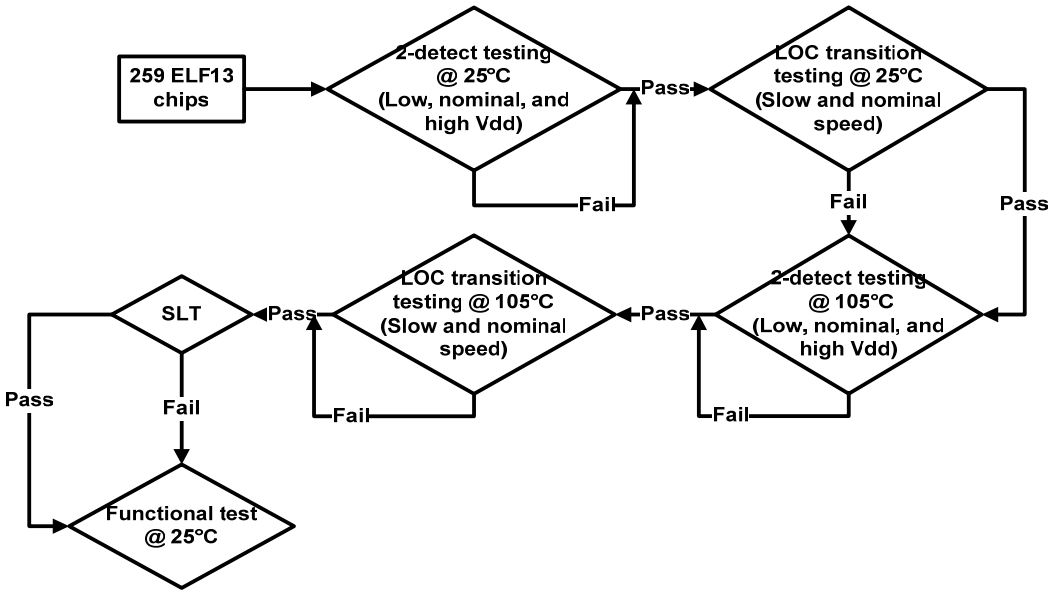


Figure 4 Experiment test flow

Table 4 Test conditions

Test	Test conditions			
	Test set	Speed (MHz)	Voltage (V)	Temperature (°C)
Test 1	LOC	Nominal	1.355	25
Test 2	LOC	10	1.355	25
Test 3	2-detect	<10	0.9	25
Test 4	2-detect	<10	1.355	25
Test 5	2-detect	<10	1.6	25
Test 6	LOC	Nominal	1.355	105
Test 7	LOC	10	1.355	105
Test 8	2-detect	<10	0.9	105
Test 9	2-detect	<10	1.355	105
Test 10	2-detect	<10	1.6	105

Table 5 presents the summary of the test length and the fault coverage of the test sets used in the experiment test flow.

Table 5 Structural test sets for the experiment test flow

Test set	Test set length	Fault coverage (%)
LOC	25,909	89.8%
2-detect	11,777	94.3%

4 Definitions, Test chip categories, and Results

In this section, we will categorize the test chips based on the experiments presented in the previous sections.

4.1 Definitions

4.1.1 Test escape

Various structural test sets, system level test, and functional test are applied to our test chips. A chip that passes all the structural tests but fail system level test or functional test is called a *structural test escape*.

4.1.2 Rated-speed failure

A chip that passes slow speed test but fails nominal speed LOC transition delay test is called a *rated-speed failure*. Slow speed LOC transition delay test and 2-detect test with nominal and high Vdd are slow speed tests.

4.1.3 Slow-speed failure

A chip that fails at least one slow speed test is called a *slow-speed failure*.

4.1.4 Weak suspect

Weak ICs contain *flaws*, which are defects in a chip that do not cause failures under normal operating conditions but result in degradation in chip performance or noise immunity. Weak chips due to certain flaws can be easily detected at certain lower-than-normal power supply voltage [Hao 93]. A chip that fails 2-detect test with low Vdd but passes all other structural tests is categorized as a weak suspect.

4.1.5 Overkill candidate

A chip that passes the System Level Test, functional test, but fails structural tests is called an *overkill candidate*.

4.1.6 Defective chip

A chip that that fails the SLT or functional test, and fails at least one structural test is called a *defective chip*.

4.2 Results of test chip classification

Table 6 presents the test results of ELF13 classification. Note that our samples pass the LOC transition delay test at room temperature but we observe some rated-speed failures. This is because the LOC transition delay test set applied at the experiment test flow has higher fault coverage than the LOC transition delay test set applied at the production test flow.

Table 6 ELF13 test chip classification

Temperature	Category	SLT or functional test		Total
		Pass	Fail	
Hot temperature only	Structural test escape (TE)	NA	0	2
	Rated-speed failure	89	20	109
	Slow-speed failure	22	7	29
	Weak suspect (WS)	15	3	18
	Overkill candidate	126	0	126
Room temperature only	Structural test escape (TE)	NA	26	26
	Rated-speed failure	1	0	1
	Slow-speed failure	10	2	12
	Weak suspect (WS)	19	2	22
	Overkill candidate	30	0	30
Hot and room temperature	Structural test escape (TE)	NA	9	9
	Rated-speed failure	20	21	41
	Slow-speed failure	7	7	14
	Weak suspect (WS)	12	5	17
	Overkill candidate	40	0	40

5 Switching activity of test patterns

5.1 Switching activity of scan-based test patterns

Several researches have been conducted on reducing the power dissipation of test patterns. [Saxena 03] presented the technique to generate “quiet patterns” which contain less switching activity. Test scheduling [Chou 97] provides a way to generate patterns that satisfy the power budget. Another methods to reduce test power are static compaction [Sankaralingam 00], test vector reordering [Dabholka 98], and gating of scan elements [Gerstendorfer 99]. However, those power reduction techniques do not correlate power consumption to overkill. In this report, we will provide the relationship between power consumption and the occurrence of overkill and test escapes.

Power consumption in a CMOS circuit can be divided into static and dynamic [Hodges 03]. Static power consumption is due to the leakage current. When a node toggles its value, dynamic power consumption occurs, which is proportional to the number of toggled nodes. When scanning in test vectors, all the scan flip-flops and combinational logics that are fed by the scan flip-flops are exercised. Due to the lack of the lower correlation between consecutive vectors, a larger number of nodes will be toggled during scanning in and scanning out the vectors [Wang 98]. Therefore, switching activity of scan-based test patterns could result in high power consumption and large currents during test mode. Heat and current spikes generated from power consumption during test mode may exacerbate the delay of a CUT (Circuit Under Test) in the following manner.

1. Heat build-up can increase the delay of a CUT. Propagation delay of CMOS inverters can be expressed from equation 1 [LIM 84].

$$t_{pd} = 0.9 C_L V_{DD} [\frac{1}{I_{Dn(Sat)}} + \frac{1}{I_{Dp(Sat)}}] \quad (1)$$

where $I_{Dn(Sat)}$ and $I_{Dp(Sat)}$ are saturation current of NMOS and PMOS, respectively. This equation implies that the propagation delay of an inverter is inversely proportional to the saturation currents of NMOS and PMOS. However, saturation current in a CMOS circuit decreases as temperature increases. Therefore, heat accumulated due to the switching activity of test patterns could slow down the

operation of a CUT. Figure 5 presents the SPICE simulations on the relationship between delays and temperature in a four-stage inverter chain. In this simulation, 0.13μm technology file is used.

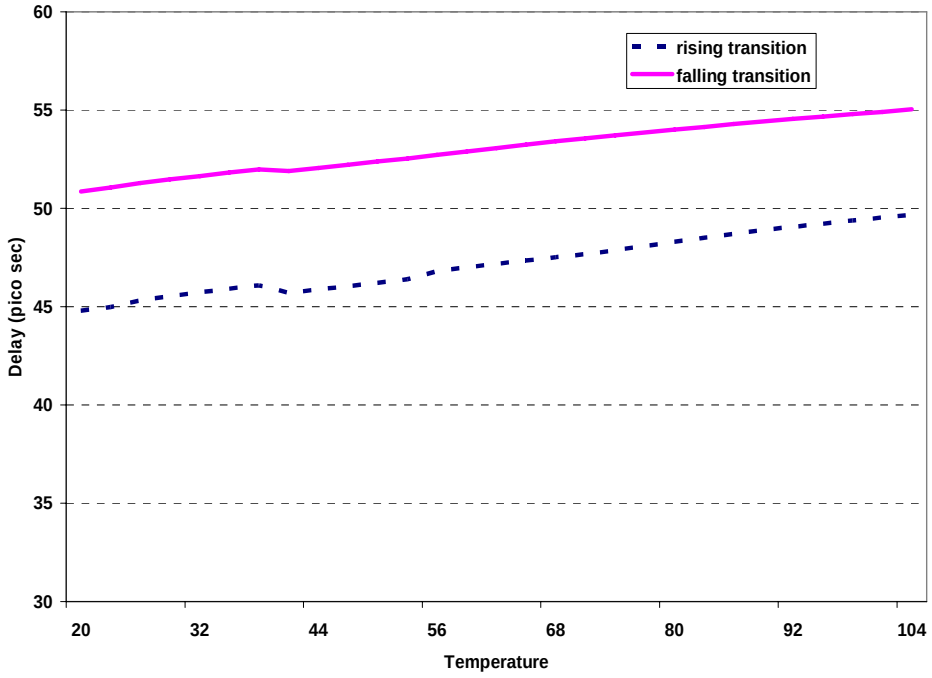


Figure 5 SPICE simulations – Delay vs. temperature

2. Current spikes can increase the delay of a CUT. A reduction in supply voltage (also called *supply voltage droop*) due to the resistance of power-ground network is called *IR-drop*. This happens when large current flows in a chip. When scanning in test vectors, large amount of nodes are toggled at the same time. This may result in current spikes which are usually higher than the currents during functional operation. As a result of current spikes, power supply voltage could drop below the normal operation range. This fluctuation of power supply voltage degrades the speed of a CUT. Relationship between the supply voltage and propagation delay is given by the following equation [Jonathan 96].

$$t_{pd} = \frac{C_L V_{DD}}{\mu C_{ox}(W/L)(V_{DD} - V_t)^2} = K\frac{V_{DD}}{(V_{DD} - V_t)^2} \qquad (2)$$

Propagation delay of a CMOS circuit increases as a supply voltage decreases. Therefore, a good chip may be slower than the system speed when it is tested using scan-based transition test patterns and suffers from IR-drop due to switching activity of test patterns. Figure 6 presents the SPICE simulations on the delays and supply voltage change in a four-stage inverter. Simulation is done at 25°C using 0.13μm technology file.

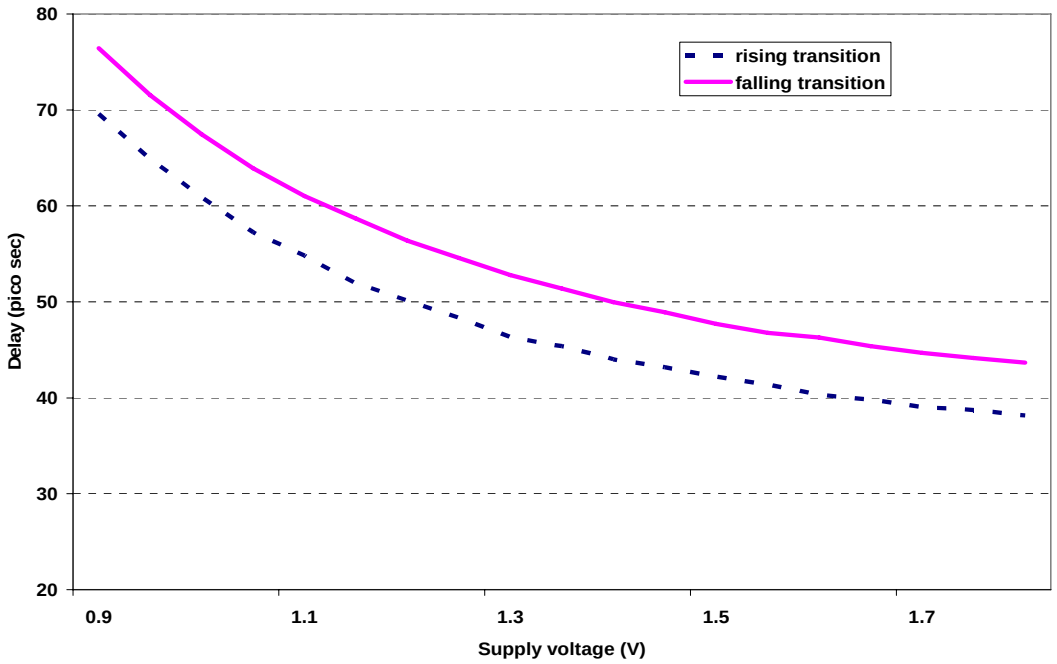


Figure 6 SPICE simulations – Delay vs. supply voltage

5.2 Transition delay test set

In this section, we will explain various transition delay test sets.

5.2.1 Launch-on-capture and launch-on-shift transition delay test set

The *transition fault* models a delay of a transition at the inputs and outputs of logic gates [Waicukauski 88]. In order to detect transition faults, we need to make a transition on a node and propagate a transition to the observable outputs. Therefore, two vectors (V_1, V_2) are needed in transition delay testing, where V_1 initialize the value of the node, V_2 makes a transition on the node and sensitizes the transition to the observable outputs. Most

commercial ATPG tools support two kinds of transition delay test sets: *Launch-On-Shift (LOS)* and *Launch-On-Capture (LOC)* [Saxena 02]. Figure 7 presents the timing diagram of LOS and LOC test patterns.

In LOS test patterns, scan data is loaded through scan chains. Nodes in a CUT are initialized at the last shift clock. In order to make transitions and capture the response of a CUT, scan enable signal must go from 1 to 0, and capture clock is applied subsequently. Because scan enable signal changes between launch and capture clock, which is applied at system speed, scan enable signal should be designed to operate at system speed. Due to this design restriction, LOC test patterns are more frequently used.

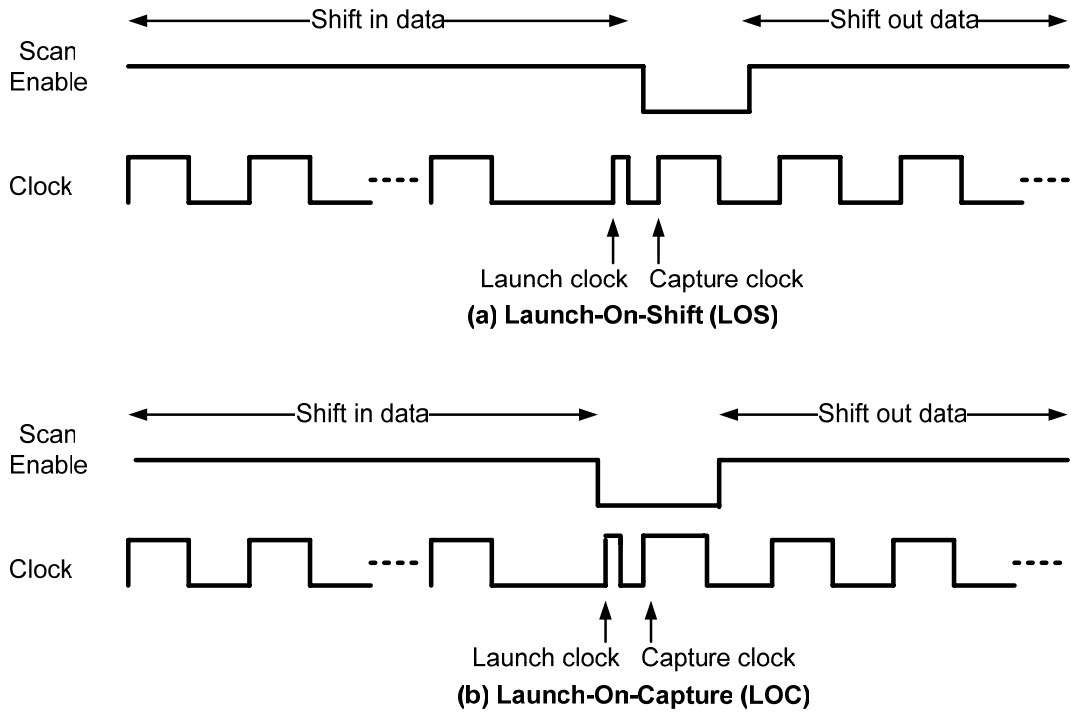


Figure 7 Timing diagrams of transition delay test patterns

In LOC test patterns, scan enable signal does not need to operate at system speed. Once scan data is loaded through scan chains, scan enable signal transitions to 0. Subsequently, launch and capture clock are applied. Launch vector should be calculated from the response of a CUT at the capture clock because launch and capture clock are applied while scan enable is low. Due to this restriction, LOC test set suffers from large test set size and low

fault coverage compared to LOS test set. In addition, it requires more ATPG computation and restrictions than LOS test set whose launch vector is simply shifted in.

5.2.2 Launch-on-capture test set with idle cycles

Excessive switching activity could cause good chips to fail structural tests. Underlying physical mechanisms on the failures may vary [Saxena 03]. However, we will focus on the heat dissipation and IR-drop during scanning in data as the physical mechanisms of the cause of overkill. Heat dissipation or IR-drop due to the excessive switching activity could increase the delays of a CUT such that it fails transition delay test but operates correctly in a system. During scanning in data, most of the scan flip-flops and the logic gates that are fed by the outputs of scan flip-flops will be toggled at the same time. *Launch-On-Capture with idle cycles (LOC-IC)* test set is the LOC test set with idle cycles inserted between the last shift and launch clock per pattern. A *base LOC test set* is the LOC test set before idle cycles are inserted. A base LOC test set is directly generated from a commercial ATPG tool. Figure 8 presents the timing diagram of LOC-IC.

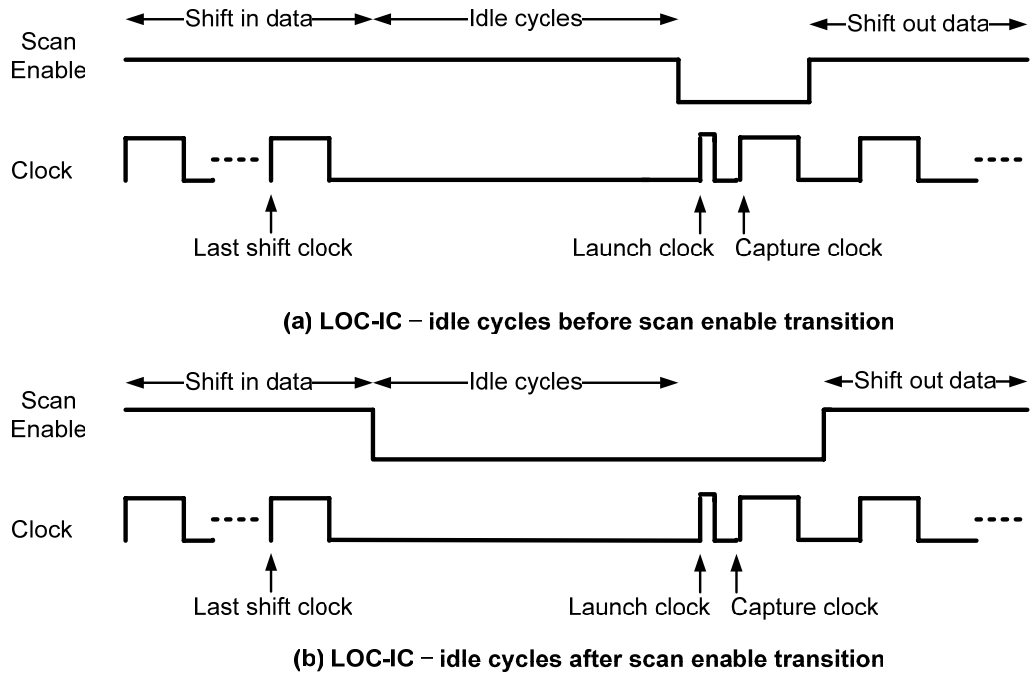
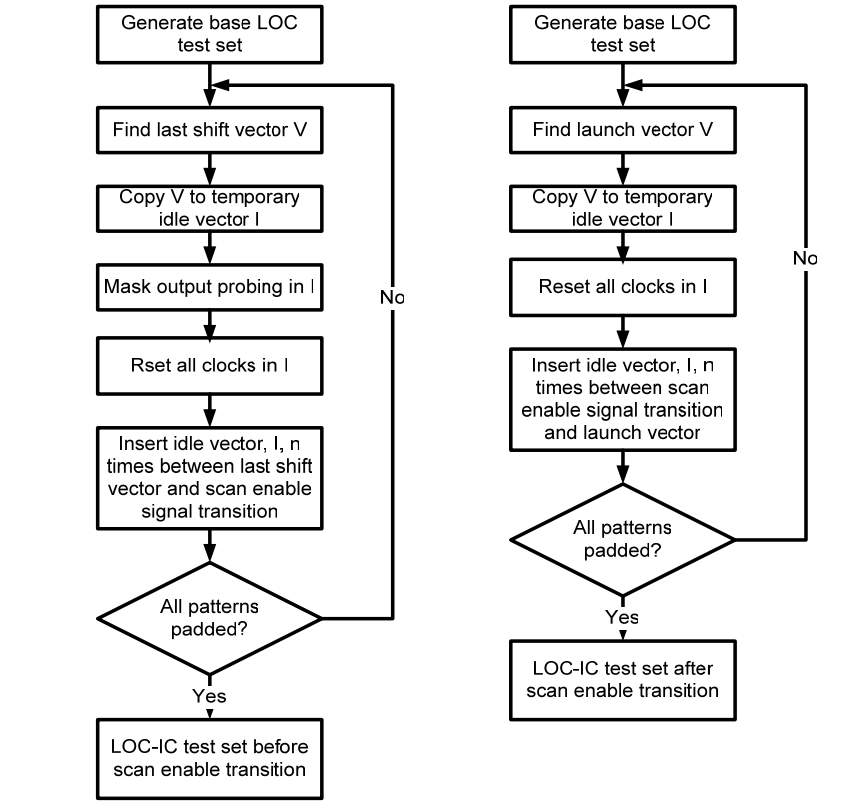


Figure 8 Timing diagram of LOC-IC transition delay test pattern

As can be seen from Figure 8, LOC-IC transition delay test set can be implemented in two ways: (1) idle cycles are inserted before scan enable signal transition, and (2) idle cycles are inserted after scan enable signal transition.

Idle cycles provide a CUT with relaxation time to recover its original supply voltage or dissipate heat due to scanning in data. Idle cycle insertion should not change the expected values of the base LOC transition delay test set. Therefore, no clocks pulse and no outputs are compared during idle cycles. In addition, primary input values should not be changed. The LOC-IC transition delay test set has the same fault coverage as the base LOC transition delay test set and it initializes and propagates faults to the observable outputs same as the base LOC transition delay test set does. In implementing the LOC-IC test set, no additional ATPG time is required because the expected outputs do not change. Figure 9 presents the flowchart of generating two kinds of LOC-IC test set.



(a) LOC-IC test set before scan enable transition (b) LOC-IC test set after scna enable transition

Figure 9 Flowchart of LOC-IC test set generation

5.3 Delay size

Failing LOC transition delay test patterns are used to obtain shmoo plots. From shmoo plots, maximum operating frequencies at nominal supply voltage were collected. Based on the maximum operating frequencies, we calculated the amount of added delay due to defects using the following equation.

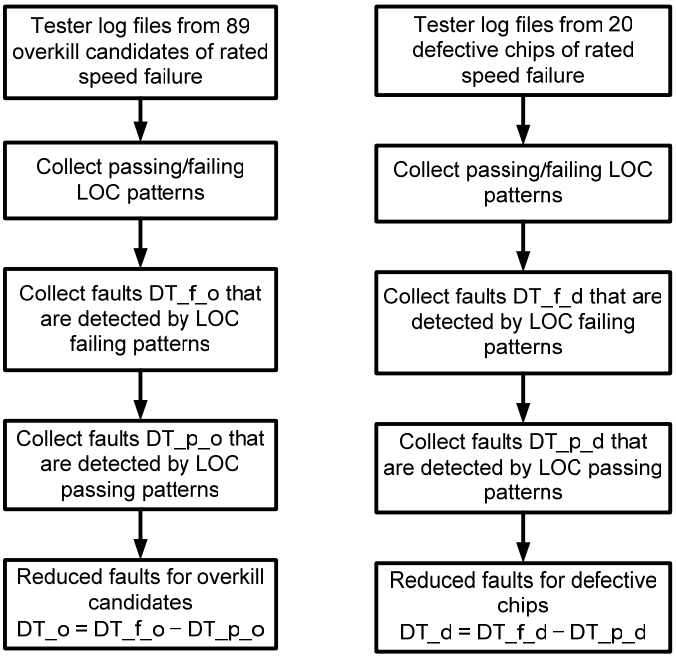
$$\text{Added delay} = \frac{1}{\text{maximum operating frequency}} - \frac{1}{\text{system frequency}} \quad (3)$$

5.4 Test setup

In this section, we will explain how various transition delay test sets are generated and applied to test chips. In the following test experiments, we used 119 ELF13 rated-speed failures at hot temperature only. Among 119 rated-speed failures, 89 chips are overkill candidates and 20 chips are defective.

5.4.1 Repeat-fill LOC test set generation

Test patterns whose don't-care bits are filled with the last significant bit are called *repeat-fill test patterns*. Test patterns whose don't-care bits are filled randomly are called *random-fill test patterns*. Compared to the random-fill test patterns, repeat-fill test patterns have lower switching activity. However, the test set size increases with repeat-fill scheme compared to random-fill scheme because compaction algorithm cannot fully take advantage of don't-care bits in pattern compaction. In ELF13 design, test set length of repeat-fill test set targeting the entire faults is prohibitively large. Note that random-fill LOC test set has 25,909 patterns. Therefore, targeting faults should be reduced. From the experiment test flow given in Figure 4, we logged the failure cycles from LOC test at 105ºC. From the tester log files, failing and passing LOC transition test patterns were collected. Reduced fault list contains the faults that are detected by failing LOC transition test patterns but not detected by passing LOC transition test patterns. Reduced fault lists were generated for overkill candidates and defective chips. Figure 10 presents the flowchart for collecting the reduced fault list.



(a) Reduced faults for overkill candidates (b) Reduced faults for defective chips

Figure 10 Flowchart of reduced faults collection

For overkill candidates, the number of reduced faults is 2.3% of the entire faults. For defective chips, it is 0.17%. After collecting reduced fault lists, repeat-fill and random-fill LOC test sets are generated targeting reduced faults in Figure 10.

5.4.2 LOC-IC test set generation

Random-fill LOC test sets explained in section 5.4.1 are used as the base test sets in generating LOC-IC test sets. Using those base test sets, LOC-IC test sets are generated according to the flowchart given in Figure 9. The number of idle cycles is varied from 3% to 30% of the shift cycles. Idle cycles are inserted before or after the scan enable signal transition.

5.4.3 Test flow

All LOC transition delay test sets explained in the 5.4.1 and 5.4.2 are summarized in Table 7. We name a LOC-IC test set as follows. First number refers to the number of idle cycles per pattern expressed as a percentage of the maximum number of shift cycle. Letter A/B followed by the number indicates the position of idle cycles. A means that idle cycles

are inserted after scan enable signal transition. B means that idle cycles are inserted before scan enable signal transition. For example, if the number of shift cycles is 1000, every pattern in 10A LOC-IC test set has 100 idle cycles which are inserted between scan enable transition and the launch cycle.

Table 7 Summary of LOC test sets

Chips	Test set	Fault coverage (%)		Test set length
		Over entire faults	Over reduced faults	
Overkill candidates	Base LOC	85.08	99.03	8,961
	Repeat-fill LOC	71.42	94.38	20,640
	3.3A LOC-IC	85.08	99.03	8,961
	6.6A LOC-IC	85.08	99.03	8,961
	10A LOC-IC	85.08	99.03	8,961
	16A LOC-IC	85.08	99.03	8,961
	33A LOC-IC	85.08	99.03	8,961
	33B LOC-IC	85.08	99.03	8,961
Defective chips	Base LOC	73.78	97.02	1,505
	Repeat-fill LOC	50.20	89.90	2,848
	3.3A LOC-IC	73.78	97.02	1,505
	6.6A LOC-IC	73.78	97.02	1,505
	10A LOC-IC	73.78	97.02	1,505
	16A LOC-IC	73.78	97.02	1,505
	33A LOC-IC	73.78	97.02	1,505
	33B LOC-IC	73.78	97.02	1,505

Fault coverage can be calculated in two ways because the base LOC test set and repeat-fill LOC test set are targeting for the reduced faults. Third column in Table 7 presents the fault coverage with respect to entire faults. Fourth column in Table 7 presents the fault coverage with respect to reduced faults. Note that fault coverage and test set length of LOC-IC test sets are same as those of the base LOC test set. However, total number of vectors is different due to the idle cycle insertion. Test sets presented in Table 7 are applied as follows.

1) The base LOC and the repeat-fill LOC test sets generated for overkill candidates are applied to 89 overkill candidates, which are categorized as rated-speed failures at hot temperature only.

2) Among 89 overkill candidates, chips that fail the base LOC test set are also tested using LOC-IC test sets.
3) The base LOC and the repeat-fill LOC test sets generated for defective chips are applied to 20 defective chips, which are categorized as rated-speed failures at hot temperature only
4) Among 20 defective chips, chips that fail the base LOC test set are also tested using LOC-IC test sets.

5.5 Experimental results

5.5.1 Repeat-fill LOC test set

Table 8 presents the experimental results of the base and repeat-fill LOC test sets applied to 119 ELF13 chips that are categorized as rated-speed failures at hot temperature only. 10 overkill candidates and 8 defective chips pass the base LOC test sets. 18 chips (10 overkill candidates and 8 defective chips) that pass the base LOC test sets pass the test because defects may not be covered by the base LOC test sets. Among 79 overkill candidates and 12 defective chips that fail the base LOC test sets, 58% of overkill candidates (46 out of 79) and 50% of defective chips (6 out of 12) pass the repeat-fill LOC test sets.

Table 8 Experimental results – base LOC vs. repeat-fill LOC

Chips		Overkill candidates			Defective chips		
Test sets		Repeat-fill LOC		Total	Repeat-fill LOC		Total
		Pass	Fail		Pass	Fail	
Base LOC	Pass	8	2	10	6	2	8
	Fail	46	33	79	6	6	12
Total		54	33	89	12	8	20

By reducing the switching activity of test patterns, not only 58% of overkill candidates can be survived but also test escapes increase. However, we cannot solely blame switching activity for the 58% of overkill candidates and 50% of test escapes because the base LOC and repeat-fill LOC have different fault coverages and faults may be initialized and propagated differently. In order to investigate switching activity as the cause of overkill, we need to eliminate as many variables as possible except switching activity. LOC-IC test sets

were applied to 79 overkill candidates and 12 defective chips that fail the base LOC test sets.

5.5.2 LOC test sets with idle cycles after scan enable signal transition

LOC-IC test sets are same as base LOC test sets except they have idle cycles between the last shift and the launch cycle. Therefore, if a chip fails the base LOC test set but passes an LOC-IC test set, idle cycles should explain the difference. Table 9 presents the experimental results on LOC-IC test sets whose idle cycles are inserted after scan enable signal transition. LOC-IC test sets were applied to 79 overkill candidates and 12 defective chips that fail the base LOC test set.

Table 9 Experimental results on LOC-IC test sets

Chips	Overkill candidates		Defective chips	
Test sets	Pass	Fail	Pass	Fail
3.3A LOC-IC	4	75	0	12
6.6A LOC-IC	4	75	0	12
10A LOC-IC	7	72	0	12
16A LOC-IC	20	59	0	12
33A LOC-IC	20	59	0	12

As can be seen from Table 9, the more idle cycles are introduced, the more overkill candidates pass LOC-IC test sets. However, no test escapes observed from LOC-IC test sets. There is no such chip that fails LOC-IC test set with more idle cycles but pass LOC-IC test set with less idle cycles. For example, all chips that fail 33A LOC-IC test set also fail all LOC-IC test sets which have less idle cycles than 33A LOC-IC test set.

Idle cycles between scan enable signal transition and the launch cycle provide chips with time to settle down in two ways: (1) during idle cycles, temperature increase due to shifting procedure could vanish away such that exacerbated delays due to temperature increase can be recovered, (2) during idle cycles, IR-drop due to shifting procedure recover the original power supply voltage such that exacerbated delays due to IR-drop can be recovered. In order to understand and identify the underlying physical mechanisms explained above, we applied LOC-IC test sets whose idle cycles are inserted between the last shift and scan enable signal transition, which will be discussed in the next section.

If the delay of a chip is so large that the portion of delays affected by idle cycles is negligible, it can still fail the LOC-IC test set. This will be further discussed by presenting the delay size of the chips.

5.5.3 LOC test sets with idle cycles before scan enable signal transition

33B LOC-IC test set was applied to 79 overkill candidates that fail the base LOC test set. All 79 overkill candidates fail 33A LOC-IC test set. The amount of relaxation time in 33B LOC-IC test set due to idle cycles are same as that in 33A LOC-IC test set. The only difference between the two test sets is the position of idle cycles. If a chip passes a test set with idle cycles because they introduce time for a chip to be cooled down, the position of idle cycles should not make any difference as long as the number of inserted idle cycles is the same. However, no chips pass LOC-IC test sets when idle cycles are inserted before scan enable signal transition. This implies that idle cycles introduce time for a chip to recover the power droop caused by IR-drop (especially IR-drop due to scan enable signal transition) during shifting procedure. Note that scan enable signal is fed to all scan flip-flops at the same time. Therefore, it is possible that there exist current peaks due to scan enable signal transition such that a chip suffers from IR-drop, which may cause overkill.

5.5.4 Delay size and minimum operating voltage

A chip that fails the base LOC test set and passes one or more LOC-IC test sets whose idle cycles are inserted after scan enable signal transition is called an *LOC-IC passing chip*. A chip that fails the base LOC test set and all LOC-IC test sets whose idle cycles are inserted after scan enable signal transition is called an *LOC-IC failing chip*. No LOC-IC passing chips are found from defective chips. Therefore, there are three categories of test chips: (1) LOC-IC passing chips which are overkill candidates (20 chips), (2) LOC-IC failing chips which are overkill candidates (59 chips), and (3) LOC-IC failing chips which are defective chips (12 chips). Delay size of the above three categories calculated from equation 3 is presented in Figure 11. Histogram is presented as the percentage of the occurrence out of total population of each category.

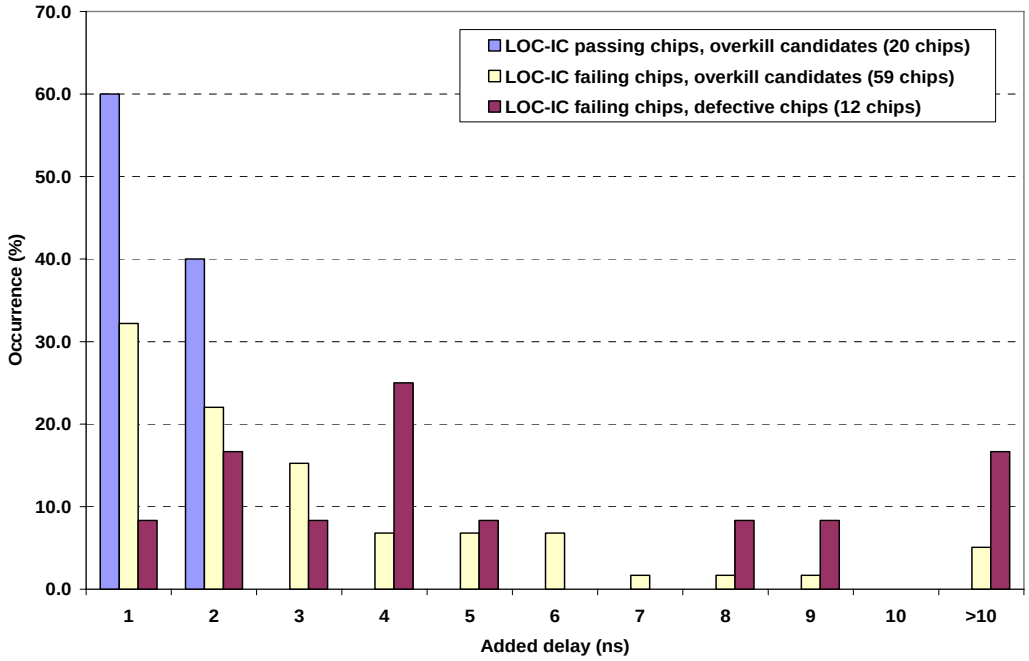


Figure 11 Histogram of added delay

All the overkill candidates that pass any LOC-IC test sets have less than 2ns of delays. Due to the smaller delay size of the chips in this category compared to the other categories, IR-drop during shifting procedure can be critical to them. Defective chips and overkill candidates that fail all LOC-IC test sets are distributed towards larger delays compared to the previous category of the chips. Therefore, they are less likely to be affected by IR-drop which could be recovered by idle cycles. Chips with small delay size do not necessarily pass LOC-IC test sets because delay defects are located where IR-drop is not significant. However, there are no chips with large delay which pass LOC-IC test sets. Small delay size is not a sufficient condition but a necessary condition for chips to pass LOC-IC test sets.

Minimum supply voltage that a chip passes the test is called V_{min}. We used the base LOC test sets to find V_{min} values. Supply voltage is increased by 0.02V from the nominal voltage (1.355V) to 1.555V and pass/fail results are logged for each chip. Figure 12 presents the histogram of V_{min} values for three categories.

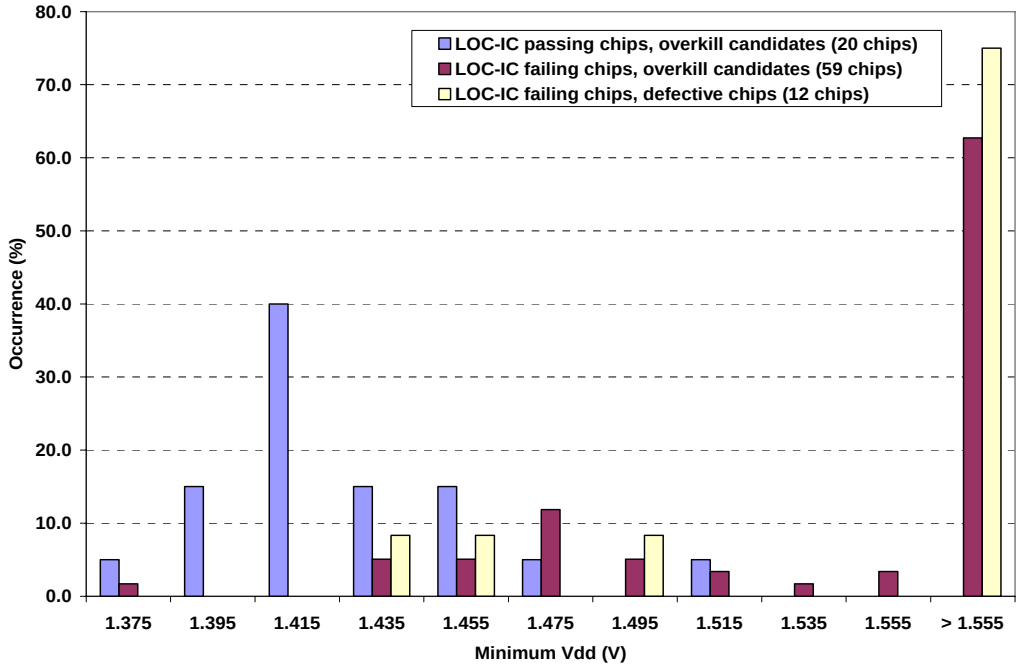


Figure 12 Histogram of minimum V_{min} values

60% (3 leftmost bars in Figure 12) of LOC-IC passing chips have V_{min} values of 1.415V or below. On the other hand, more than 60% (a rightmost bar in Figure 12) of LOC-IC failing chips fail at 1.555V regardless of overkill candidates or defective chips.

5.5.5 Test time cost

The more idle cycles are inserted, the more test time it takes. Additional test time due to idle cycles is given by the following equation.

$$Additional\ test\ time\ (s) = \frac{\#\ of\ inserted\ idle\ cycles\ per\ pattern \times \#\ of\ test\ patterns}{shift\ frequency} \quad (4)$$

Additional test time is also a function of test set length because idle cycles are inserted every pattern.

Test time of LOC test set without idle cycles can be calculated from equation 5.

$$Test\ time\ (s) = \frac{number\ of\ shifts + 2}{shift\ frequency} \times number\ of\ test\ patterns + \frac{number\ of\ shifts}{shift\ frequency} \quad (5)$$

Therefore, test time of LOC-IC would be the sum of equation 4 and 5.

Table 10 presents test time of various LOC test sets.

Table 10 Test time comparison

Chips	Test sets	Test time (sec)		
		Additional test time due to idle cycles	Test time without idle cycles	Total test time
Overkill candidates	Base LOC	0	3.91	3.91
	Repeat-fill LOC	0	9.0	9.0
	3.3A LOC-IC	0.13	3.91	4.04
	6.6A LOC-IC	0.26	3.91	4.17
	10A LOC-IC	0.38	3.91	4.29
	16A LOC-IC	0.64	3.91	4.55
	33A LOC-IC	1.28	3.91	5.19
	33B LOC-IC	1.28	3.91	5.19
Defective chips	Base LOC	0	0.66	0.66
	Repeat-fill LOC	0	1.24	1.24
	3.3A LOC-IC	0.02	0.66	0.68
	6.6A LOC-IC	0.04	0.66	0.70
	10A LOC-IC	0.06	0.66	0.72
	16A LOC-IC	0.11	0.66	0.77
	33A LOC-IC	0.22	0.66	0.88
	33B LOC-IC	0.22	0.66	0.88

Implementation of LOC-IC test set takes advantage of commercial ATPG tools. No new ATPG algorithm is required and any compaction algorithm in commercial ATPG tools can be utilized. We can generate a base LOC test set as compact as possible using commercial ATPG tools. After that, idle cycles can be easily inserted using a script.

5.5.6 Comparisons of scan-based LOC test sets

In this section, we will compare various scan-based LOC test sets in terms of (1) reduction in overkill, (2) increase in test escapes, (3) test set length, (4) fault coverage, and (4) test time.

Table 11 presents the comparisons of various scan-based LOC test sets. All comparisons are made against the base LOC test sets except the fault coverage. For example, the repeat-fill LOC test set reduced overkill candidates by 46 compared to the base LOC test set, and it has 11,679 more patterns than the base LOC test set. The repeat-fill LOC test set generated for overkill candidates take 5.09 seconds longer than the base LOC test set to apply patterns.

Table 11 Comparisons of scan-base LOC test sets

Chips	Test sets	Population change in overkill	Population change in test escapes	Change in test set length	Fault coverage (%)	Additional test time (s)
Overkill candidates	Base LOC	0	NA	0	85.08	0
	Repeat-fill	-46	NA	+11,679	71.42	+5.09
	3.3A LOC-IC	-4	NA	0	85.08	+0.13
	6.6A LOC-IC	-4	NA	0	85.08	+0.26
	10A LOC-IC	-7	NA	0	85.08	+0.38
	16A LOC-IC	-20	NA	0	85.08	+0.64
	33A LOC-IC	-20	NA	0	85.08	+1.28
	33B LOC-IC	0	NA	0	85.08	+1.28
Defective chips	Base LOC	NA	0	0	73.78	0
	Repeat-fill	NA	+6	+1,343	50.20	+0.58
	3.3A LOC-IC	NA	0	0	73.78	+0.02
	6.6A LOC-IC	NA	0	0	73.78	+0.04
	10A LOC-IC	NA	0	0	73.78	+0.06
	16A LOC-IC	NA	0	0	73.78	+0.11
	33A LOC-IC	NA	0	0	73.78	+0.22
	33B LOC-IC	NA	0	0	73.78	+0.22

From Table 11, the repeat-fill LOC test set has the largest reduction in overkill candidates. However, it also increases the number of test escapes and suffers from bigger test set size and long test time. On the other hand, LOC-IC test sets reduce the number of overkill candidates up to 20 depending on the size of idle cycles but do not increase the number of test escapes. Test time of LOC-IC test sets is longer than test time of the base LOC test set due to the idle cycles. However, it is shorter than test time of repeat-fill LOC test set.

6 Conclusions

This report investigates the cause of overkill and how overkill could be reduced. Experiments were conducted on the ELF13 graphics processor from NVIDIA manufactured using 0.13μm technology.

Excessive switching activity of test patterns could result in overkill. Switching activity of test patterns can be reduced by filling the don't-care bits with the last significant bit. Our experimental results suggest that not only overkill but also defective chips could pass structural test using this approach. Therefore, this approach may degrade the test quality.

In this report, we propose a new test set which could reduce overkill without any test quality degradation. With the proposed test patterns, 20 out of 79 overkill candidates pass the structural test, but no test escapes occur. In addition, proposed method is easy to implement and commercial ATPG tools can be directly used.

We suspect temperature increase and IR-drop as the underlying physical mechanisms of how switching activity of test patterns could cause overkill. Idle cycles were inserted before or after scan enable signal transition in order to identify the physical mechanisms. Experimental results show that IR-drop due to scan enable signal transition cause overkill.

7 Acknowledgements

This research is funded by SRC under contract No. 1175.001. This research is cooperation with NVIDIA. We would like to thank Bruce Cory of NVIDIA for his valuable help. We also would like to thank to Subhasish Mitra of Stanford CRC, Erik Volkerink of Agilent and Stanford CRC, Intaik Park of Stanford CRC for their valuable comments and suggestions.

References

[Chang 98] Chang, J.T.-Y., Chao-Wen Tseng, Yi-Chin Chu, S. Wattal, M. Partell and E.J. McCluskey, "Experimental results for IDDQ and VLV testing," *VLSI Test Symposium, 1998. Proceedings. 16th IEEE , 26-30 April 1998,* pp. 118 – 123

[Chou 97] Chou, R.M., Saluja, K.K., and Agrawal, V.D., "Scheduling tests for VLSI systems under power constraints," *IEEE Trans. on VLSI Systems*, vol. 5, no. 6, pp. 175-185, 1997

[Dabholkar 98] Dabholkar, V., Chakravarty, S., Pomeranz, I., and Reddy, S., "Techniques for minimizing power dissipation in scan and combinational circuits during test application," *IEEE Trans. On Computer-Aided Design*, vol. 17, no. 12pp. 1325 – 1333, 1998

[Franco 91] Franco, P., and E.J. McCluskey, "Delay Testing of Digital Circuits by Output Waveform Analysis," *Proc. 1991 Int. Test Conf.*, Nashville, TN, pp. 798-807, Oct. 26-30, 1991.

[Gerstendorfer 99] Gerstendorfer, S., and Wunderlich, H.J., "Minimized power consumption for scan-based BIST," *Proc. Intl. Test Conf.*, pp. 77-84, 1999.

[Hao 93] Hao, H., and E.J. McCluskey, "Very-low-voltage testing for weak CMOS logic ICs," *Proc. Intl. Test Conf.*, pp. 275-284, 1993.

[Hodges 03] Hodges, D.A., H.G. Jackson, R.A. Saleh, *Analysis and Design of Digital Integrated Circuits*, Third Edition, McGraw-Hill, 2003

[Jonathan 96] Chang, J.T.-Y., and E.J. McCluskey, "Detecting delay flaws by very-low-voltage testing," *Proc. Intl. Test Conf.*, pp. 367-376, 1996

[Kim 03] Kim, K.S., S. Mitra, and P.G. Ryan, "Delay Defect Characteristics and Testing Strategies," *IEEE Trans. on Design & Test of Computers*, vol. 20, Sept.-Oct. 2003 pp. 8 – 16.

[Kusko 01] Kusko, M., B.J. Robbins, T.J. Koprowski and W.V. Houtt, "99% AC test coverage using only LBIST on the 1 GHz IBM S/390 zSeries 900 Microprocessor," *Proc. Intl. Test Conf.*, pp. 586-592, 2001.

[Lesser 80] Lesser, J.D., and J.J. Shedletsky, "An Experimental Delay Test Generator for LSI Logic," *IEEE Trans. on Computers*, vol. C-29, No. 3, pp. 235-248, 1980

[Lim 84] Lim, H.K., J.G. Fossum, "Transient drain current and propagation delay in SOI CMOS," *IEEE Trans. on Electron Devices*, vol. 31, Issue 9, pp. 1251-1258, 1984

[McCluskey 00] McCluskey, E.J., Chao-Wen Tseng, "Stuck-fault tests vs. actual defects," *Proc. Intl. Test Conf.*, pp. 336-343, 2000.

[McCluskey 04] E.J. McCluskey, A.A. Al-Yamani, C.M. Li, C.W. Tseng, E. Volkerink, F. Ferhani, E. Li, and S. Mitra, "ELF-Murphy Data on Defects and Test Sets," *VLSI Test Symposium, 2004, Proceedings. 22th*, 25 April-29 April pp. 16 – 22.

[Millman 88] Millman, S.D. and E.J. McCluskey, "Detecting bridging faults with stuck-at test sets,**"** *Proc. Intl. Test Conf.*, pp. 773-783, 1988.

[Sankaralingam 00] Sankaralingam, R., Oruganti, R.R., and Touba, N.A., "Static compaction techniques to control scan vector power dissipation," *VLSI Test Symposium, 2000. Proceedings. 18th IEEE , 30 April-4 May 2000*, pp. 35-40

[Saxena 01] Saxena, J., K.M. Butler, L. Whetsel, "An analysis of power reduction techniques in scan testing," *Proc. Intl. Test Conf.*, pp. 670-677, 2001

[Saxena 02] Saxena, J., K.M. Butler, J. Gatt, R. Raghuraman, S.P. Kumar, C. Basu, D.J. and J. Berech, "Scan-based transition fault testing - implementation and low cost test challenges," *Proc. Intl. Test Conf.*, pp. 1120-1129, 2002.

[Saxena 03] Saxena, J., K.M. Butler, V.M. Jayaram, S. Kundu, N.V. Arvind, P. Sreeprakash, M. Hachinger, "A case study of IR-drop in structured at-speed testing," *Proc. Intl. Test Conf.*, pp. 1098-1104, 2003

[Shedletsky 78] Shedletsky, J.J., "Delay Testing LSI Logic," Dig. 8th Annu. Int. Symp. Fault-Tolerant Comput., pp. 159-164, 1978

[Smith 85] Smith, G.L., "Model for Delay Faults Based upon Path," *Proc. Intl. Test Conf.*, pp. 342-349, 1985

[Wang 98] Wang, S., S.K. Gupta, "ATPG for Heat Minimization During Test Application," *IEEE Trans. on Computers*, vol. 47, Issue 2, pp. 256-262, 1998