WHY DEFECTS ESCAPE SOME OF OUR TESTS

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A defect can escape detection either because (1) the test patterns applied do not expose the effects of the defect, or (2) the defect does not interfere with correct operation at the operating conditions of the tests.

Incomplete Tests

The first case occurs when the test patterns are not thorough enough, but it may be very difficult to determine how thorough the test patterns really are. As an example, let's consider testing of a combinational circuit — perhaps as part of an internal scan test. Further, suppose that the part was not to be operated at an aggressive speed so that delay fault testing was not necessary assuming that process drift was checked by some other means such as ring oscillators, etc. If we had generated a test set that had 100% single stuck fault coverage we would be confident that we were applying a very thorough test. Hidden in this confidence is the belief that the defects would not change the combinational circuit into a sequential circuit. How could this happen? One possibility is that a defect caused a bridging fault that inserted an asynchronous feedback loop into the circuit. Another, and probably much more likely explanation, is that a defect caused an open in the circuit. In our Murphy experiment [1], we found that 36 of the 116 defective chips exhibited sequence dependent behavior; that is, their output response changed if the order in which the inputs were applied was changed. One might think that the way to avoid this situation would be to apply a stuck-open test set; but in our experiment the stuck-open test set was very long and still missed many of the defective chips. There were several multiple-detect test sets that were shorter than the stuck-open test set and which detected all of the defective chips.

Operating Conditions Dependence

The second case in which the chip operates correctly for the specified operating conditions is one in which the defect is present but is not serious enough to interfere with correct operation. Such a defect is sometimes called a *flaw* and a chip containing such a defect is called a *weak chip.* Such defects are of interest since they are likely to cause *early life failures* — the chip does not operate for the normal lifetime of a defect-free chip. The main technique used to eliminate weak chips is burn in. There is interest in finding ways to avoid the necessity of burn in. (It's very expensive.) Two of the most prominent are Iddq testing and VLV (very low voltage) testing.

We have been studying tunneling open defects, very thin opens that allow electron or holes to tunnel through. Our interest in these came about because in the Murphy experiment we discovered 7 of the chips that failed VLV testing behaved as if tunneling opens were present. As expected, none of these chips failed temperature burn in and 2 of the 7 did not fail Iddq testing. Thus, there are 2 chips that have flaws that pass all tests except for VLV. These two chips clearly contain defects, but we don't know whether or not they will have a short operating life. The details relating to tunneling opens are given in [2].

Seems as if we need to keep looking for better ways to test chips!

References

[1] McCluskey, E.J. and C.W. Tseng, "Stuck-Fault Tests vs. Actual Defects,", Proc. 2000 International Test Conference, Atlantic City, NJ, 2000.

[2] Li, J.C.M. and E.J. McCluskey, "Testing for Tunneling Opens," Proc. 2000 International Test Conference, Atlantic City, NJ, 2000.