Experimental Data on Test Escapes

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Abstract

Defective chips may pass structural tests applied via scan chains (also called *test escapes*). We conducted many experiments on test chips fabricated in three different technologies (0.13µm, 0.18µm, and 0.35µm) to understand the extent of the number of test escapes and to develop techniques that minimize the number of test escapes. This paper presents the test chips, the setup of the experiments, the experimental data collected, and the results of analyzing the data.

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1. Introduction

Defective chips may pass structural tests applied via scan chains (also called *test escapes*). A significant fraction of the manufacturing defects in chips are defects that make the circuits fail at the designed speed, but operate correctly at a slower speed (also called *delay defects*) [Franco 91] [Lesser 80] [Shedletsky 78] [Smith 85]. Therefore, testing for delay defects is very important to keep the defect level, often measured in the number of Defective Chips Per Million (DPM), acceptably low [McCluskey 00] [Kim 03]. Delay testing via scan chains is being increasingly adopted in the industry for screening parts with delay defects [Kusko 01] [Saxena 02].

A test in which the chip is inserted into a system that tests the functionality of a chip according to a functional specification is called a *System Level Test (SLT)*. Unfortunately, testing for delay defects using a system level test is very expensive. Moreover, the system level test may still cause test escapes.

One of the main challenges in researching test escapes and yield loss is the danger of drawing conclusions from only a few data points. Hence, during the last year, we have developed an extensive test infrastructure to allow test escape and yield loss experiments using multiple EDA tools (commercial and academic), using multiple ATEs, using multiple test chips that use multiple technologies (from multiple vendors). Moreover, we have generated many different test patterns.

The SRC report [Lee 04] focuses on yield loss. This SRC report focuses on test escapes. Part of the work has been published in [McCluskey 04]. We have acknowledged SRC as a sponsor in [McCluskey 04].

Experiments were done on three test chips: NV2B, ELF35, and ELF18: NV2B is a graphics processor from nVidia. NV2B is manufactured in 0.13µm. ELF18 includes a Digital Signal Processor core from Philips [Mitra 04]. ELF18 is manufactured in the Philips 0.18µm technology. ELF35 was designed at Stanford CRC especially for performing test

experiments [Franco 94] [Franco 95] [McCluskey 04]. ELF35 is manufactured in LSI logic 0.35μm technology.

This paper is organized as follows.

Section 2 presents the three test chips in detail. Section 3 discusses the infrastructure for the test escape and yield loss experiments.

Section 4 presents the NV2B test experiments. Three different categories of test escapes were investigated. Test escapes in category 1 and 2 pass all the structural tests and functional test but fail the SLT. We have generated 2 different test patterns and applied them under 10 different test conditions. Test escapes in category 3 pass all tests.

Section 5 presents the ELF18 test experiments. N-detect and SSF test patterns with different fault coverages were applied. Both uncompacted and compacted SSF test patterns were applied and the number of test escapes will be presented. A transition test set that is designed to detect either slow-to-rise or slow-to-fall faults in each node is called *single-sided transition test set.* Single-sided transition test sets were applied to ELF18. The test set size reduction and the number of test escapes will be presented.

Section 6 presents the ELF35 test experiments. N-detect and SSF test patterns with different fault coverages were applied. Both uncompacted and compacted SSF test patterns were applied and the number of test escapes will be presented. Single-sided transition test sets were applied to six different cores of ELF35. The number of test escapes and test set size reduction will be presented. This paper concludes with Section 7.

2. Test Chips

This section presents the three test chips used in the experiments. Table 1 presents the characteristics of the test chips.

Table 1 Characteristics of test chips

Test chip		Feature size of the Technology	Number of Gates	Number of Flip-Flops	Number of Clock Domains	Number of I/Os	Number of Scan chains
NV2B		0.13μm	7.2 million	NA	>10	436	NA
ELF18		0.18μm	53,732	1,428	1	41	10
ELF35	LSI2901	0.35μm	12,338	544	1	125	1
	TOPS2901		18,090	961	1	105	1
	MA		4,499	0	0	98	0
	PB		17,468	0	0	24	0
	M12		1,309	0	0	36	0
	SQR		538	0	0	18	0
	Total		54,242	1505	2	406	2

NV2B is a graphics processor using 0.13μm technology. It has 7.2 million logic gates and more than 10 clock domains. The nominal supply voltage is 1.355V and the number of I/Os is 436.

ELF18 is manufactured in the Philips 0.18μm Corelib technology [Mitra 04]. Each chip consists of 26 cores – die-id cores, RAM cores, ROM cores, analog cores, library evaluation cores, 6 DSP cores and a chip controller core. The DSP core implements a R.E.A.L. Digital Signal Processor [Kievits 98].

ELF35 uses LSI Logic G10p 0.35μm cell-based technology [Li 99]. It has approximately 265k LSI Logic equivalent gates. There are six types of cores. Two cores are arithmetic processors, which perform the same function but were implemented in different

ways. These two cores are full-scan sequential circuits. The other four are combinational circuits. Three of these four combinational cores are datapath circuits. The other one is a translator that maps a pseudo-random sequence into a binary sequence.

3. Infrastructure

One of the main challenges in researching test escapes and yield loss is the danger of drawing conclusions from only a few data points. Hence, during the last year, we have developed an extensive test infrastructure to allow test escape and yield loss experiments using multiple EDA tools (commercial and academic), using multiple ATEs, using multiple test chips that use multiple technologies (from multiple vendors).

During the last year, we have invested relatively much time in developing the infrastructure, because the infrastructure will also supports next years SRC research objectives. The test infrastructure includes:

- Test pattern generation scripts for many EDA tools (Synopsys, Cadence, Syntest Mentor Graphics, and academic tools).
- UNIX scripts to analyze (and diagnose) test results. UNIX scripts to convert files to different EDA or ATE formats
- Test programs on two ATE systems (Advantest ATE and Agilent ATE) for many different test conditions.
- The above for 4 different test chips.

Developing such an infrastructure poses many practical challenges. For example, we were required to study many EDA tools, both the hardware and software features of multiple testers (ATE), many test chips, and System Level Test (SLT).

For example, in order to generate the test patterns that we needed for our experiments, we were required to understand the netlist of the four test chips in detail (even though we were only involved in the design of the ELF35 chips). Some scan flip-flops in the netlist need to be masked to prevent incorrect logic values from being propagated and captured at the scan flip-flops.

Moreover, to apply certain test patterns we needed to understand the functionality of the four test chips in detail. For example, certain input pins need to be fixed to certain values during test pattern generation (and test pattern application).

After the test pattern generation, test patterns need to be converted to a tester (ATE) specific format to load the patterns on the tester. A *timing table* defines all the timing

specifications and it controls the tester such that it applies the correct system clocks at the correct time slots with the specified speeds. To apply test patterns, we needed to generate the timing tables based on a careful analysis of the functional specification of the four test chips.

A significant part of the infrastructure can only be developed and debugged using a tester. Unfortunately, our tester time was very limited (i.e., only 2 to 3 hours a week).

4. NV2B Experiments

4.1. Test flow

Three different categories of test escapes were collected and tested.

1. Test escapes that pass all the structural tests and functional test but fail the SLT once.
2. Test escapes that pass all the structural test and functional test but fail the SLT twice.
3. Test escapes that pass all our test patterns (under all conditions).

Fig. 1 presents the test flow used to obtain test escapes f category 1 and 2.

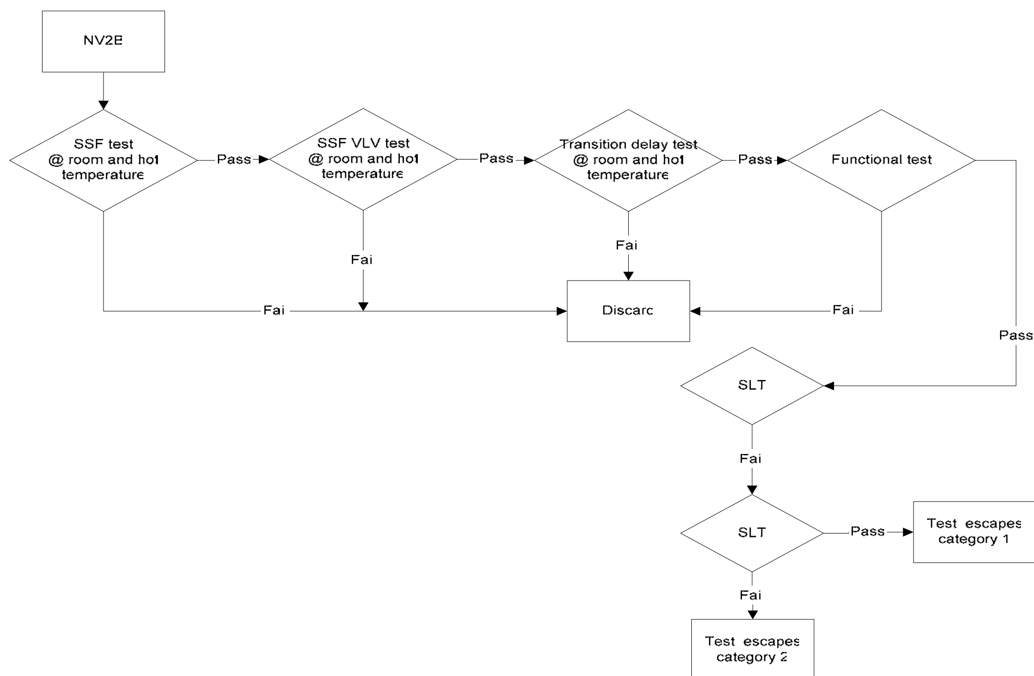

Figure 1 Test flow of NV2B SLT failing chips

SLT was applied twice under the same conditions to identify intermittent failures. Test escapes in category 1 and 2 pass all structural tests at both room temperature (25°C) and hot temperature (100°C). Functional testing is applied after structural testing. SLT was applied at the end. Test escapes in category 1 fail the SLT once but pass the second SLT. Test escapes in category 2 fail the SLT twice.

Fig. 2 presents the test flow used to obtain test escapes of category 3.

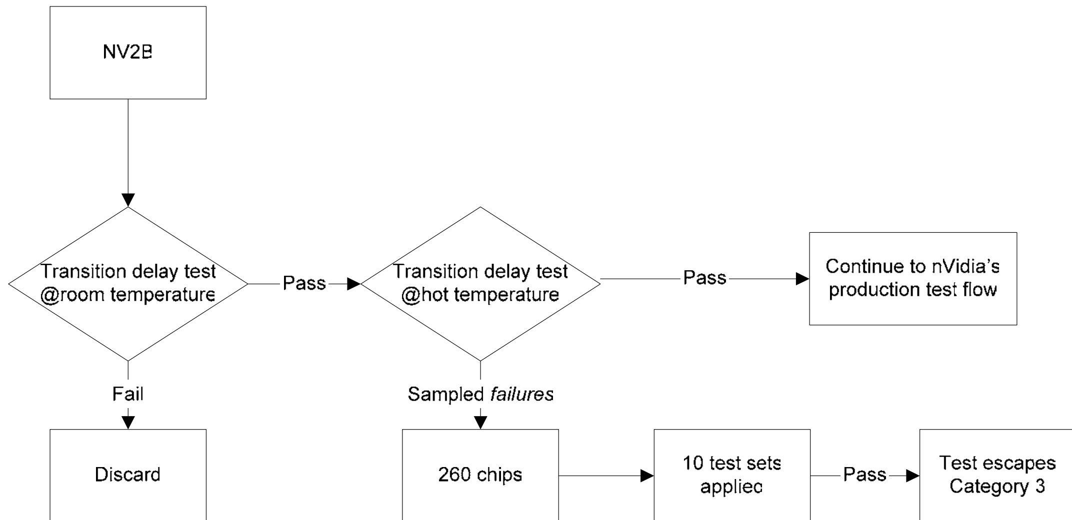

Figure 2 Test flow of NV2B LOC failing chips

Test escapes in category 3 are the chips that pass 10 different test conditions. Table 2 presents the 10 test conditions applied to test escapes of category 3.

Table 2 Test conditions

Test	Test conditions			
	Test set	Speed (MHz)	Voltage (V)	Temperature (°C)
Test 1	LOC	Nominal	1.355	25
Test 2	LOC	10	1.355	25
Test 3	2-detect	<10	0.9	25
Test 4	2-detect	<10	1.355	25
Test 5	2-detect	<10	1.6	25
Test 6	LOC	Nominal	1.355	100
Test 7	LOC	10	1.355	100
Test 8	2-detect	<10	0.9	100
Test 9	2-detect	<10	1.355	100
Test 10	2-detect	<10	1.6	100

Launch-On-Capture (LOC) transition tests patterns force the scan enable signal to low after the scan chain data is shifted into the scan flip-flops. Subsequently, the system clock is applied twice to launch logic values and capture the response of the chip.

39 test escapes of category 1 were tested at room temperature (test 1, 2, 3, 4, and 5 in Table 2). 61 test escapes of category 2 were tested at room and hot temperatures (test 1 through 10 in Table 2). 80 test escapes of category 3 were tested at room and hot temperatures (test 1 through 10 in Table 2).

A defect that does not depend on the clock speed is also called a *timing-independent defect* [McCluskey 04] [Chang 98]. A defect that is not a *timing-independent defect* is called a *timing-dependent defect* [McCluskey 04] [Chang 98]. LOC transition test patterns were applied at very slow speed to differentiate the timing-dependent defects from timing-independent defects.

2-detect test patterns were applied at three different supply voltages to investigate the voltage dependent defects: low *Vdd (0.9V)*, nominal *Vdd (1.355V)*, and high *Vdd (1.6V)*. Table 3 presents the summary of the test length and the fault coverage of the test sets.

Table 3 Structural test sets

Test set	Test set length	Fault coverage (%)
LOC[1]	409	72%
2-detect	11,777	94.3%

4.2. Test Results

4.2.1. Test Results on SLT failing chips (Category 1 and 2)

The 5 tests (test 1, 2, 3, 4, and 5 in Table 2) are applied on 39 test escapes that pass all the structural tests and functional tests but fail the SLT once (i.e., category 1). 39 test escapes of category 1 pass all test sets (test 1, 2, 3, 4, and 5 in Table 2).

The 10 tests (test 1 through 10 in Table 2) are applied on 61 test escapes that pass all the structural tests and functional tests but fail the SLT twice (i.e., category 2). 2 chips of category 2 are detected. One chip fails the nominal speed LOC transition test at room temperature (test 1, see Table 2) and the other chip fails the 2-detect test with high supply voltage at hot temperature (test 10, see Table 2). 59 chips of category 2 pass all test sets (test 1 through 10 in Table 2).

4.2.2. Test Results on LOC transition test failing chips (Category 3)

Fig. 3 presents the classification of test escapes in (1) chips that fail the tests at room temperature (25°C), but escape the tests at hot temperature (100°C), (2) chips that escape the tests at both hot and room temperature, and (3) chips that fail the tests at hot temperature, but escape at room temperature.

[1] Test patterns of higher fault coverage are currently being generated

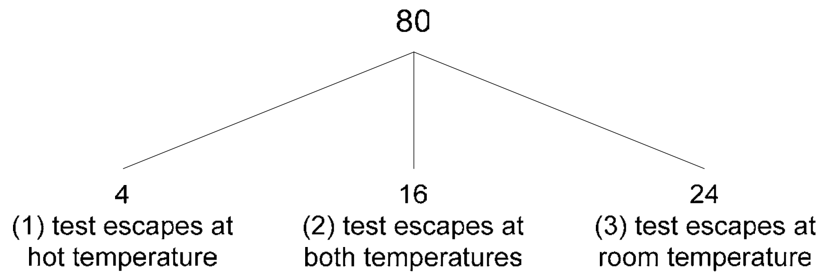

Figure 3 Classification of test escapes

Table 4 presents detailed test results of the chips that fail at room temperature, but escape the tests at hot temperature

Table 4 Test escapes at hot temperature detected at room temperature

chip ID	2det low vdd	2det nom vdd	2det high vdd	LOC slow speed	LOC nom speed
1	P	F	P	P	P
22	P	F	P	P	P
45	F	P	P	F	F
70	F	P	P	P	F
# of detection	2	2	0	1	1

Table 5 presents detailed test results of the chips that fail at hot temperature, but escape the tests at room temperature.

Table 5 Test escapes at room temperature detected at hot temperature

Chip ID	2-det low vdd	2-det nom vdd	2-det high vdd	LOC slow speed	LOC nominal speed
3	P	P	P	P	F
5	F	P	P	P	F
6	P	P	F	P	F
8	P	P	P	P	F
9	F	P	P	P	F
11	P	P	P	P	F
12	P	F	P	P	F
13	F	P	P	P	P
15	F	P	P	P	F
16	P	P	P	P	F
18	F	P	P	P	P
21	F	F	F	P	P
26	P	F	F	F	F
32	P	P	P	P	F
33	F	P	P	P	P
38	P	P	P	P	F
42	F	P	P	P	P
46	P	P	P	P	F
47	F	P	P	P	F
49	F	P	P	P	F
50	P	P	P	P	F
62	P	F	F	P	P
65	F	F	F	P	P
72	F	P	P	P	P
# of detection	12	5	5	1	16

20 more test escapes were observed at room temperature in comparison to the number of test escapes at hot temperature.

5. ELF18 Experiments

5.1. Test flow

Fig. 4 presents the ELF18 test flow.

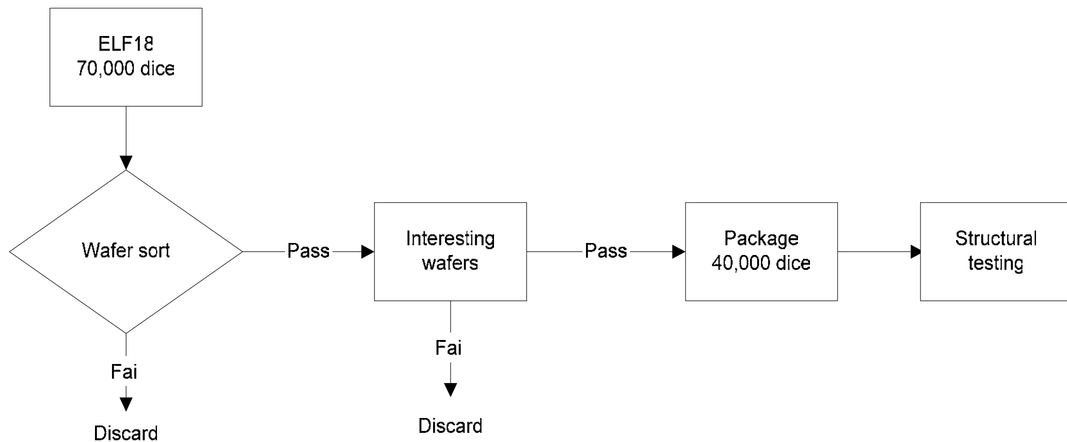

Figure 4 ELF18 Test flow

Wafer sort tests were applied to about 70,000 dice. Wafers with a number of chips that failed a certain set of tests were classified as interesting wafers. All the dice on a subset of interesting wafers were packaged. Subsequently, we've applied additional tests to filter the interesting dies. We have applied our experiments on the set of interesting dies.

5.2. Test results

5.2.1. Test set compaction and fault coverage reduction

The number of test patterns determines the test time (and test cost). Therefore, to reduce the test cost, techniques have been developed that reduce the number of test patterns.

Test set compaction can reduce the number of patterns while preserving the fault coverage. Our commercial tool supports 2 compaction techniques: (1) dynamic compaction and (2) static compaction:

1. *Dynamic compaction* is performed by running fault simulation at several stages of the test pattern generation process and dropping the faults that are detected by the generated patterns.

2. *Static compaction* is performed by combining the patterns that do not have any conflicts in the specified bit positions.

Although both compaction techniques preserve the faults coverage, we have demonstrated in [McCluskey 04] that the number of escapes increases with compaction.

Compacted and uncompacted SSF test sets with different fault coverage were applied to ELF18 chips. Our compacted test sets were obtained by applying both dynamic and static compaction. Fig. 5 presents the test results.

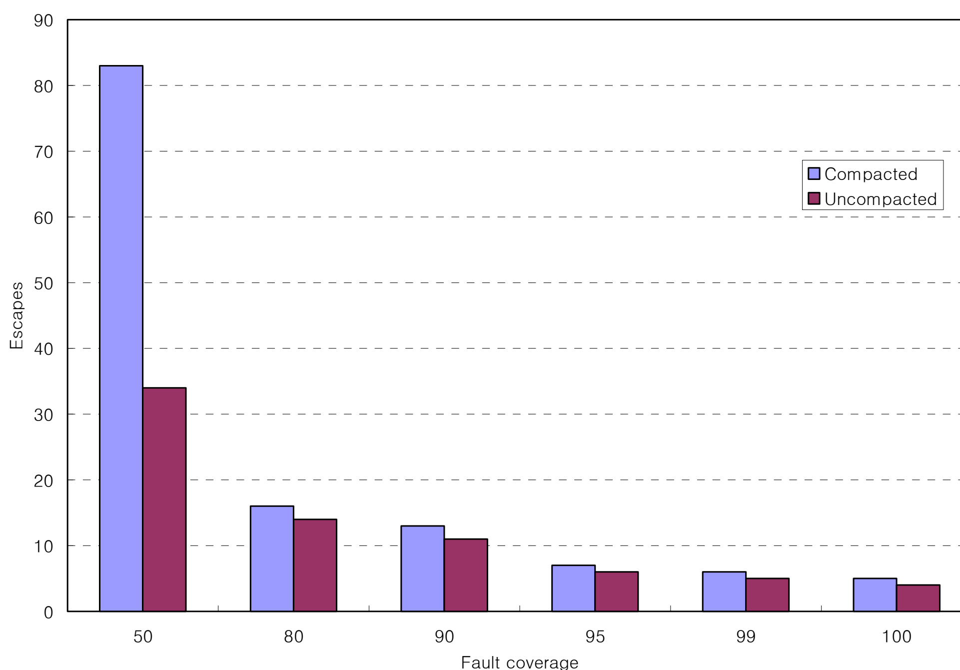

Figure 5 Changes in test escapes due to compaction and fault coverage

The results demonstrate that compaction increases the number of test escapes. For example, compacting the 100% fault coverage test set causes one additional test escape. Moreover, compacting the 50% fault coverage test set causes 49 additional test escapes.

Note that test set length can also be reduced by fault coverage reduction. SSF patterns with the fault coverage between 50% and 100% were applied. Our results suggest that

reducing fault coverage always comes with an increase in the number of test escapes (see Fig. 5).

5.2.2. N-detect

A test set in which each single stuck-at fault is detected more than once is called a *N-detect test set* [Ma 95] [McCluskey 00] [McCluskey 04]. In a 2-detect test set, each single stuck-at fault is detected by at least two different test patterns.

2, 3, 5, 10, and 15-detect test sets were applied. Fig. 6 presents the test results of N-detect test sets.

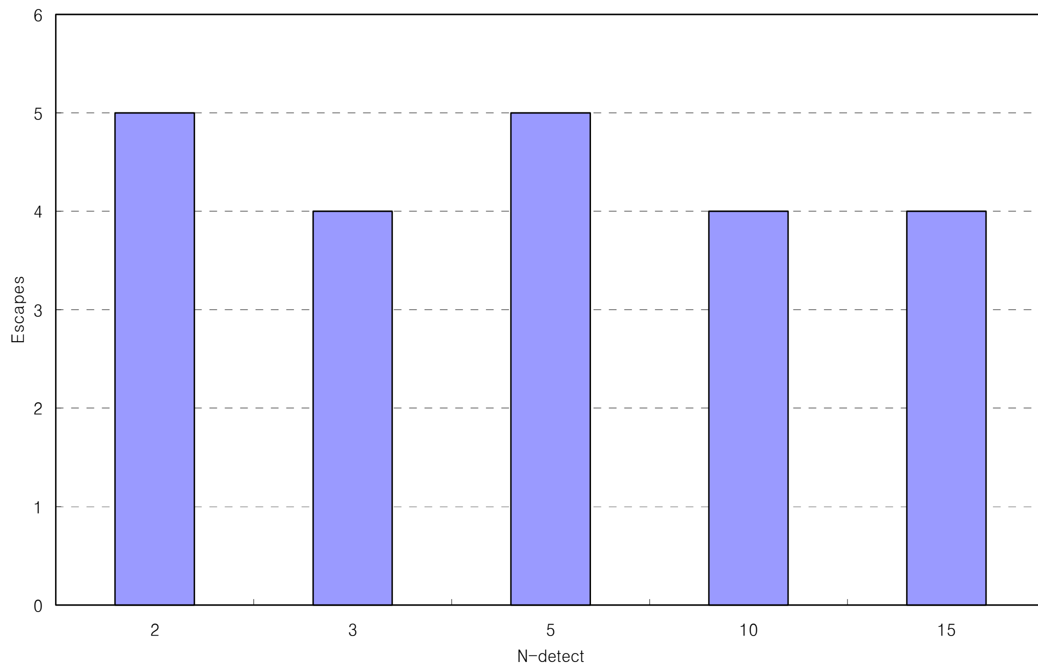

Figure 6 Test results of N-detect test sets

5.2.3. Transition test set

A transition delay test set is generated to detect both the slow-to-rise and the slow-to-fall faults in each node in the circuit – this is referred to as a *double-sided transition test* set.

A transition test set that is designed to detect either the slow-to-rise or the slow-to-fall fault in each node is called a *single-sided transition test set* [Benware 03].

The single-sided transition patterns were generated by a commercial ATPG tool.

We will also analyze the reduction in the number of test patterns. The test set size reduction is calculated using the following equation.

$$\text{Test set size reduction} = \frac{\text{Double-sided transition test set length - Single-sided transition test set length}}{\text{Double-sided transition test set length}} \times 100$$

Table 6 presents the comparison of single-sided transition test set and double-sided transition test set experiments.

Table 6 Experimental Results on single-sided Transition Delay Patterns on ELF18

Number of defective cores	Transition test set	Test set length	Number of test escapes	Test set size reduction (%)
464	Double-sided	757	1	NA
	Single-sided	347	4	54.20

The single-sided transition test caused three more defective escapes than the double-sided transition test. Test set length is significantly reduced from 757 to 347 (54.2%).

6. ELF35 Experiments

6.1. Test flow

Fig. 7 presents the ELF35 test flow.

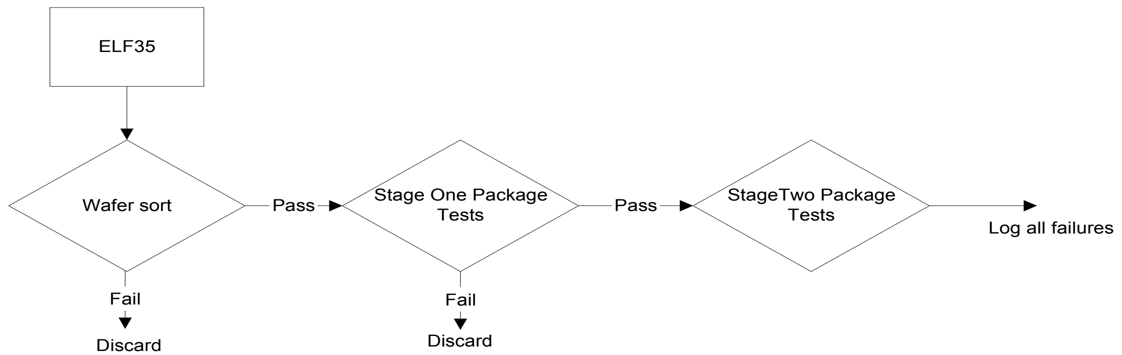

Figure 7 ELF35 Test Flow

Any chip that fails the first package stage tests did not go on to the next stage. Any chip that passes the first package tests, but fails some or all of the second stage package tests we call "interesting cores". A total of 495 interesting cores are identified. Details of classification of the interesting cores are in [McCluskey 04]. Details of the wafer and package tests can be found in [Li 99].

6.2. Test Results

This paper will present the experimental results on test escapes.

6.2.1. Test set compaction and fault coverage reduction

Table 7 presents test set length for different test sets.

Table 7 Test set length comparisons

	100% Fault Coverage		99% Fault Coverage		95% Fault Coverage	
	Uncomp Test length	Δ Test length (Comp)	Uncomp Test length	Δ TL (Comp)	Uncomp Test length	Δ Test length (Comp)
LSI	318	128	317	124	173	27
TOPS	518	202	502	174	310	122
SQR	42	20	40	18	36	13
M12	72	31	58	19	47	19
MA	103	50	66	6	32	0
PB	3176	489	2887	364	2198	174

Fig. 8 presents the comparisons of test escapes with different fault coverage and compaction.

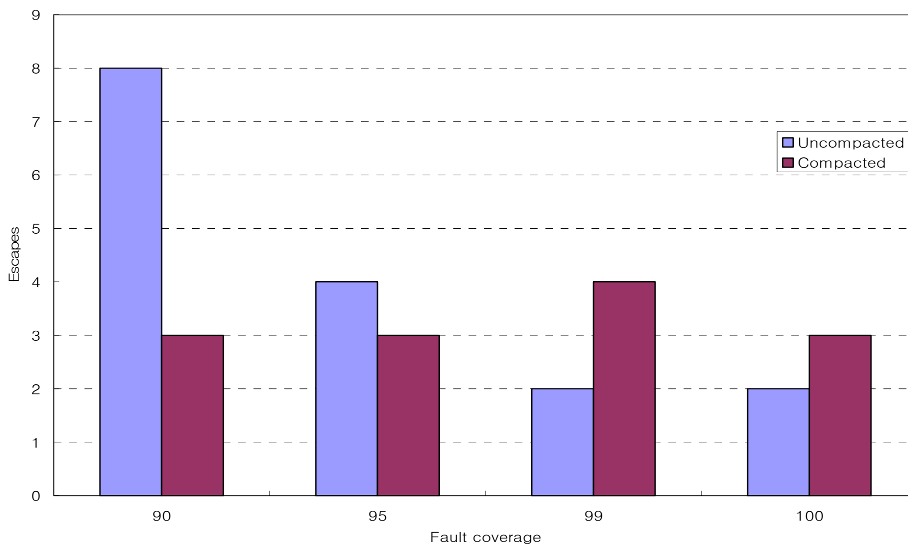

Figure 8 Increase in test escapes due to compaction and fault coverage

Impact of compaction and fault coverage reduction on the number of test escapes is similar to that of ELF18. Compaction does not preserve the defect coverage.

Reducing the fault coverage also comes with an increase in the number of test escapes.

6.2.2. N-detect

Table 8 [McCluskey 04] presents the number of test escapes for test sets with a single stuck-at fault coverage varying from 100% to 50%. Also we applied N-detect varying from 15-detect to 2-detect. The columns labeled 1C, 4C, and 9C correspond to three different commercial ATPG tools.

Table 8 Number of test escapes vs. fault coverage of compacted test sets

Tools			1C	4C	9C
SSF	N-Detect	15	0	3	-
		10	1	2	-
		5	2	1	-
		3	2	4	-
		2	3	5	-
	Fault Coverage	1.00	2	5	4
		0.99	1	6	3
		0.95	4	7	6
		0.90	9	10	8
		0.80	18	28	19
		0.50	92	68	79

The data suggests that the *thoroughness* of a test set measured by the number of defective chips that escape detection by that test set is strongly correlated to the test set fault coverage.

6.2.3. Transition test set

Table 9 presents the number of test escapes on single-sided transition test sets.

Table 9 Experimental Results on single-sided Transition Delay Patterns on ELF35

		Double-sided transition test set		Single-sided transition test set		Test set size reduction (%)
	Defective cores	Test set length	Escapes	Test set length	Escapes	
LSI	92	786	1	343	0	56.36
TOPS	30	957	0	440	0	54.02
M12	38	105	0	56	0	46.67
MA	28	131	0	72	0	45.04
PB	133	5604	0	2945	0	47.45
SQR	15	48	0	30	1	37.50

Although the single-sided transition test sets consists of a smaller number of test patterns than the double-sided transition test sets (see table 9), there was only one additional test escape for the SQR core (see chapter 2, page 3 and 4 for an overview of the ELF35 cores). Moreover, the single-sided transition test set caused a reduced number of LSI core escapes compared to the double-sided transition test set. The number of single-sided transition test escapes was the same as the number of double-sided transition test escapes if applied to TOPS, M12, MA, and PB cores.

7. Summary

One of the main challenges in researching test escapes and yield loss is the danger of drawing conclusions from only a few data points. We have developed an extensive test infrastructure to allow test escape and yield loss experiments using multiple EDA tools (commercial and academic), using multiple ATEs, using multiple test chips that use multiple technologies (from multiple vendors). Test chips manufactured in three different technologies were used to quantify the number of test escapes.

We have generated 2 different test patterns (2-detect test patterns and LOC transition test patterns) and applied them under 10 different test conditions (i.e., slow speed LOC transition test, nominal speed LOC transition test, 2-detect test with low Vdd, nominal Vdd, high Vdd, all both at room temperature and hot temperature). 100 SLT failing chips, which pass the structural and functional tests, but fail the SLT, were tested with the 10 tests. Among 100 chips, 2 chips fail our 10 tests.

Temperature dependency of test escapes was discussed. Our experiments suggest that the number of test escapes is reduced if the same test sets are applied at a hot temperature compared to room temperature. Our experiments suggest that VLV testing is more effective in detecting chips at hot temperature.

The number of test patterns can be reduced by compaction techniques. However, our experiments demonstrate that the number of test escapes increase with compacted test sets. Reducing the fault coverage can also reduce the number of test patterns. Our experiments demonstrate that reducing fault coverage always comes with an increase in the number of test escapes.

N-detect test sets varying from 2-detect to 15-detect were applied and the resulting number of test escapes were discussed.

Single-sided transition test patterns were applied to the ELF35 and ELF18 chips. Our experiments suggest that test set size can be reduced by 56% by using single-sided transition test patterns compared to using double-sided transition test patterns. In four cores of the ELF35 chip, the number of test escapes of the single-sided transition test patterns was the same as that in double-sided transition test patterns. We observed an increase in the

number of SQR test escapes (ELF35). Moreover, we observed an increase in the number of ELF18 test escapes.

8. Future work

The last year, we have spent a lot of time and effort to make the infrastructure. We intend to continue to use the infrastructure to get more experimental results in order to draw more conclusions and to meet the objectives of our research program.

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