Experimental Data on the Extent of Yield Loss

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Abstract

Chips that operate under normal conditions (*good chips*) may fail structural tests applied via scan chains (also called *yield loss*). For example, the structural test may sensitize paths that are not sensitized during normal operation (also called *false paths)*.

We conducted many experiments on test chips fabricated in four different technologies (0.13μm, 0.14μm, 0.18μm, and 0.35μm) to understand the extent of yield loss and to develop techniques to minimize yield loss. This paper presents the test chips, the setup of the experiments, the experimental data collected, and the results of analyzing the data.

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1 Introduction

Structural test patterns applied via scan chains can potentially cause good chips to be rejected (*yield loss*). A significant fraction of the manufacturing defects in chips are defects that make the circuits fail at the designed speed, but operate correctly at a slower speed (also called *delay defects*) [Franco 91] [Lesser 80] [Shedletsky 78] [Smith 85]. Therefore, testing for delay defects is very important to keep the defect level, often measured in the number of Defective Chips Per Million (DPM), acceptably low [McCluskey 00] [Kim 03]. Delay testing via scan chains is being increasingly adopted in the industry for screening parts with delay defects [Kusko 01] [Saxena 02].

Yield loss occurs due to: (1) false path or (2) multi-cycle path.

1. A number of paths can be sensitized during normal operation of a chip (also called the *valid sensitizable paths*). A path that cannot be sensitized during normal operation is called a *false path*. It is very difficult to guarantee that all patterns applied by the scan chains only sensitize valid paths and no false path. For example, a good chip may fail a test because the test sensitizes a false path. Therefore, the false path may cause yield loss.
2. Designs may require two or more clock cycles to propagate a response through a path and to capture the response at the scan chain flip-flops (also called *multi-cycle path*) [Saxena 02]. During normal operation, it is guaranteed by design that the contents of the scan chain flip-flops of multi-cycle paths are sampled only at appropriate times. However, during the test mode, the scan chain flip-flops may be sampled at incorrect times. Therefore, the multi-cycle paths may cause yield loss.

A test in which the chip is inserted into a system that tests the functionality of a chip according to a functional specification is called a *System Level Test (SLT)*. Unfortunately, testing for delay defects using a system level test is very expensive. Moreover, the system level test may still cause test escapes.

One of the main challenges in researching test escapes and yield loss is the danger of drawing conclusions from only a few data points. Hence, during the last year, we have developed an extensive test infrastructure to allow test escape and yield loss experiments using multiple EDA tools (commercial and academic), using multiple ATEs, using multiple test chips that use multiple technologies (from multiple vendors). Moreover, we have generated many different test patterns.

The SRC report [Lee 04] focuses on test escapes. This SRC report focuses on yield loss.

Experiments were done on four test chips: NV18, NV2B, ELF35, and ELF18: NV18 is a graphics processor from nVidia. NV18 is manufactured in 0.14μm. NV2B is a graphics processor from nVidia. NV2B is manufactured in 0.13μm. ELF18 includes a Digital Signal Processor core from Philips [Mitra 04]. ELF18 is manufactured in the Philips 0.18μm technology. ELF35 was designed at Stanford CRC especially for performing test experiments [Franco 94] [Franco 95] [McCluskey 04]. ELF35 is manufactured in LSI logic 0.35μm technology.

This paper is organized as follows.

Section 2 presents the four test chips in detail. Section 3 discusses the infrastructure for test escape and yield loss experiments.

Section 4 presents the NV18 test experiments. We classified NV18 test chips according to the structural test experiments and the system level test experiments. Based on the experiments, we analyzed the correlation between the chips that pass the SLT and fail the SLT.

Section 5 presents the NV2B test experiments. We have generated 2 different test patterns and applied them under 10 different test conditions. Tests were done at two different temperatures in order to investigate the temperature dependency of test escapes. N-detect patterns and transition patterns were applied to identify the chips that have the timing defects. The quality of the N-detect tests is compared to the quality of slow speed

transition tests. We also varied the supply voltages to investigate the voltage dependent behavior. Experiments were conducted with three different supply voltages at two different temperatures.

Section 6 presents the ELF35 test experiments. A transition test set that is designed to detect either slow-to-rise or slow-to-fall faults in each node is called a s*ingle-sided transition test set*. Single-sided transition test sets were applied to six different cores of ELF35 and the effectiveness of single-sided transition test sets will be discussed by presenting the number of test escapes and the test set size reduction.

Section 7 presents the ELF18 test experiments. Single-sided transition test sets were applied to ELF18. Test set size reduction and the number of test escapes will be presented. This paper concludes with Section 8.

2 Test Chips

This section presents the four test chips used in the experiments. Table 1 presents the characteristics of the test chips.

Table 1 Characteristics of test chips

Test chip		Feature size of the Technology	Number of Gates	Number of Flip-Flops	Number of Clock Domains	Number of I/Os	Number of Scan chains
NV18		0.14μm	3.8 million	NA	>10	403	NA
NV2B		0.13μm	7.2 million	NA	>10	436	NA
ELF18		0.18μm	53,732	1,428	1	41	10
ELF35	LSI2901	0.35μm	12,338	544	1	125	1
	TOPS2901		18,090	961	1	105	1
	MA		4,499	0	0	98	0
	PB		17,468	0	0	24	0
	M12		1,309	0	0	36	0
	SQR		538	0	0	18	0
	Total		54,242	1505	2	406	2

NV18 is a graphics processor using 0.14μm technology. There are 3.8 million logic gates. It has about 57 million transistors and more than 10 clock domains. The nominal supply voltage is 1.44V. Three major clock domains operate more than 90% of the chip area. It has 403 I/Os.

NV2B is also a graphics processor using 0.13μm technology. It has 7.2 million logic gates and more than 10 clock domains. The nominal supply voltage is 1.355V and the number of I/Os is 436.

ELF18 is manufactured in the Philips 0.18μm Corelib technology [Mitra 04]. Each chip consists of 26 cores – die-id cores, RAM cores, ROM cores, analog cores, library evaluation cores, 6 DSP cores and a chip controller core. The DSP core implements a R.E.A.L. Digital Signal Processor [Kievits 98].

ELF35 uses LSI Logic G10p 0.35μm cell-based technology [Li 99]. It has approximately 265k LSI Logic equivalent gates. There are six types of cores. Two cores are arithmetic processors, which perform the same function but were implemented in different ways. These two cores are full-scan sequential circuits. The other four are combinational circuits. Three of these four combinational cores are datapath circuits. The other one is a translator that maps a pseudo-random sequence into a binary sequence.

3 Infrastructure

One of the main challenges in researching test escapes and yield loss is the danger of drawing conclusions from only a few data points. Hence, during the last year, we have developed an extensive test infrastructure to allow test escape and yield loss experiments using multiple EDA tools (commercial and academic), using multiple ATEs, using multiple test chips that use multiple technologies (from multiple vendors).

During the last year, we have invested relatively much time in developing the infrastructure, because the infrastructure will also supports next years SRC research objectives. The test infrastructure includes:

- Test pattern generation scripts for many EDA tools (Synopsys, Cadence, Syntest Mentor Graphics, and academic tools).
- UNIX scripts to analyze (and diagnose) test results. UNIX scripts to convert files to different EDA or ATE formats
- Test programs on two ATE systems (Advantest ATE and Agilent ATE) for many different test conditions.
- The above for 4 different test chips.

Developing such an infrastructure poses many practical challenges that are very time consuming. For example, we were required to study many EDA tools, both the hardware and software features of multiple testers (ATE), many test chips, and System Level Test (SLT).

For example, in order to generate the test patterns that we needed for our experiments, we were required to understand the netlist of the four test chips in detail (even though we were only involved in the design of one of the test chips: the ELF35 chip). Some scan flip-flops in the netlist need to be masked to prevent incorrect logic values from being propagated and captured at the scan flip-flops.

Moreover, to apply certain test patterns we needed to understand the functionality of the four test chips in detail. For example, certain input pins need to be fixed to certain values during test pattern generation (and test pattern application).

The generated test patterns need to be converted to a tester (ATE) specific format. A *timing table* defines all the timing specifications and it controls the tester such that it applies the correct system clocks at the correct time slots with the correct speeds. To apply test patterns, we needed to generate the timing tables based on a careful analysis of the functional specification of the four test chips.

A significant part of the infrastructure can only be developed and debugged using a tester. Unfortunately, our tester time was very limited (i.e., only 2 to 3 hours a week).

4 NV18 Experiments

4.1 Test flow

Fig. 1 presents the test flow for NV18.

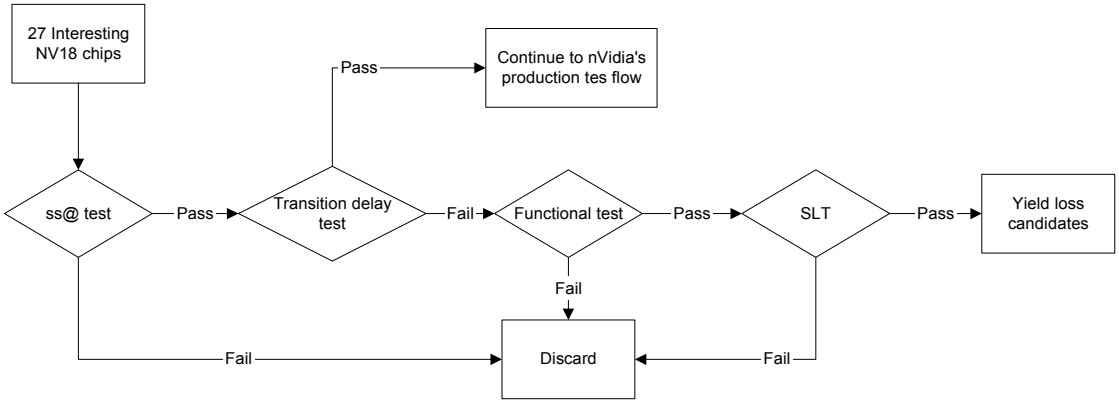


Figure 1 NV18 Test flow

NVidia selected 27 chips that pass nVidia's single stuck-at test and fail nVidia's transition delay test from 8 different lots for further research (nVidia does not want to disclose the exact selection criteria). We call the 27 chips *interesting chips*. Table 2 presents the 4 test sets applied to the NV18 chips at room temperature.

Table 2 Structural test sets for NV18

Test set		Number of test patterns	Fault coverage (%)
LOC	Clock 1	2344	56.55
	Clock 2	456	19.51
	Clock 3	801	22.92
SSF		3734	96.89

Launch-On-Capture (LOC) transition test patterns force the scan enable signal to low after the scan chain data is shifted into the scan flip-flops. Subsequently, the system clock is applied twice to launch logic values and capture the response of the chip.

Due to the large size of the chip, the test set is very large. Therefore, during production testing, the fault coverage target of the SSF and the LOC transition test patterns is often less than 100%.

A test in which the chip is inserted into a system that tests the functionality of a chip according to a functional specification is called a *System Level Test (SLT)*. System Level Testing is done at room temperature only (25°C).

We have applied our SSF tests, transition tests (LOC), and System Level Tests to the 27 interesting chips. A chip that passes the System Level Test, functional test, and SSF test but fails transition tests is classified as yield loss candidate, because it is not yet known whether they are really good chips.

Functional testing was also applied to the interesting chips. The functional test patterns are generated based on the Verilog simulation.

4.2Test results

4.2.1 Classification of NV18

Fig. 2 presents the classification of 27 NV18 chips. Table 3 presents the experimental results in detail.

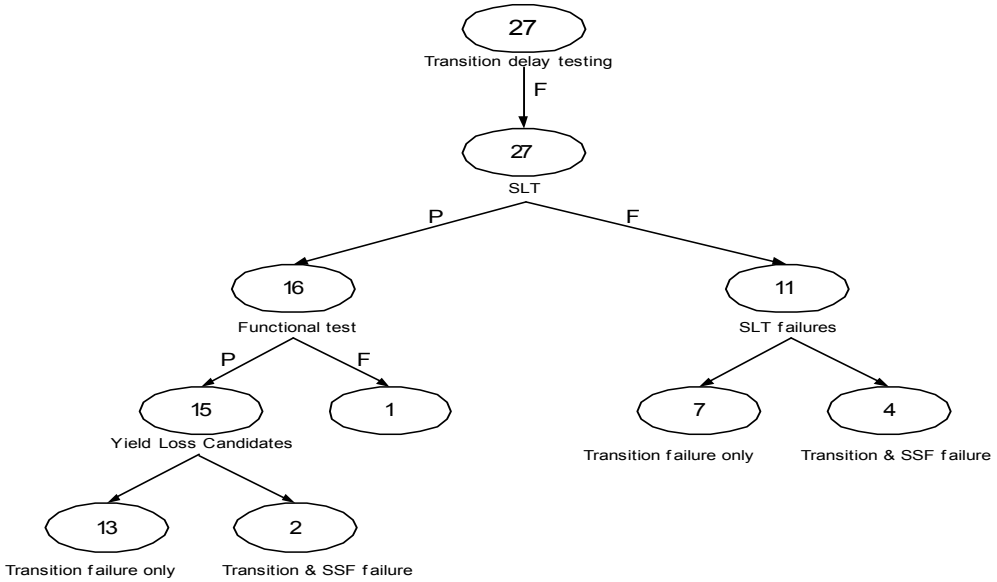


Figure 2 Classification of NV18 chips

Table 3 Experimental results on NV18[1]

Chip ID	SSF	LOC			Functional	SLT	Yield loss candidate
		Clock 1	Clock 2	Clock 3			
1	P	F	P	P	P	F	N
2	P	P	F	P	P	P	Y
3	P	F	P	P	P	P	Y
4	P	F	P	F	P	P	Y
5	P	F	P	P	P	P	Y
6	P	P	F	P	P	P	Y
7	P	F	P	P	P	P	Y
8	P	P	F	P	P	F	N
9	F	F	P	P	P	F	N
10	P	F	P	P	P	F	N
11	F	F	P	P	P	P	Y
12	P	F	P	P	P	F	N
13	P	F	P	P	F	P	N
14	P	F	P	P	P	P	Y
15	P	P	P	F	P	P	Y
16	P	F	P	P	P	P	Y
17	F	F	P	P	P	F	N
18	P	P	P	F	F	F	N
19	F	F	P	P	F	F	N
20	F	P	P	F	P	F	N
21	P	F	P	P	P	F	N
22	P	F	P	P	P	F	N
23	F	F	P	P	P	P	Y
24	P	F	P	P	P	P	Y
25	P	P	P	F	P	P	Y
26	P	F	P	P	P	P	Y
27	P	P	P	F	P	P	Y

[1] P: Pass, F: Fail, Y: Yes, N: No

The fault coverage of our SSF test is higher than the fault coverage of nVidia's SSF test (i.e., the SSF test that was used to identify the 27 interesting chips). Therefore, some chips fail our SSF test, even though the chips pass the nVidia SSF test.

In the remaining part of the paper, *failure* refers to the chips that fail the test. For example, transition fault test failures are the chips that fail the transition fault test.

All 27 chips fail the LOC transition test. 16 chips pass the SLT. Out of the 16 chips that pass the SLT, one chip fails the functional test. Therefore, we have 15 yield loss candidates (i.e., chips that fail the LOC transition test, pass the functional test and pass the SLT).

6 chips fail the SSF test. Out of the 6 chips that fail the SSF test, 2 chips pass the SLT and 4 chips fail the SLT. Chip 4 passes SLT, but fails the LOC transition test of clock domain 1 and 3 (see Table 3). Except for this chip, all chips fail at only one clock domain out of the three clock domains.

4.2.2 Comparison between yield loss candidate and SLT failure

A scan cell that captures the failing bits is called a *failing scan cell*. A scan chain that contains a failing scan cell is called a *failing scan chain*. Failing scan chains and failing scan cells of chips that pass SLT were compared to failing scan chains and failing scan cells of chips that fail SLT. We can make the following 3 observations:

1. Some failing scan cells are only associated with the chips that pass SLT. Hence, false path may be sensitized through those scan cells.
2. Some failing scan cells are only associated with the chips that fail SLT. Hence, the scan cells only capture the valid failing bits and are not associated with false path sensitization.
3. Only a very few failing scan cells (<5%) captures failing bits associated with both chips that pass SLT and chips that fail SLT.

To clearly present the experiments and motivate our observation, we introduce new terminology. We will explain the new terminology using the example test results in Table 4.

Table 4 Example Test Results

Chip	Pattern 1	Pattern 2	Pattern 3	Pattern 4	SLT	Failing scan chain (Failing scan cells)
1	F	F	P	P	P	1 (1, 2), 2 (2)
2	P	F	F	P	F	1 (3), 2 (2), 3 (1)
3	F	P	P	F	P	2 (2)

For example, the defect(s) in Chip 1 are detected by pattern 1 and 2. The SLT did not detect the defect(s). The failing bits of Chip 1 are captured in Scan cell 1 and 2 of Scan chain 1, and Scan cell 2 of Scan chain 2.

Definition 4.2.2.1 (Failing Pattern of SLT Pass, Fail, or Common): A chip that fails the structural test can either pass or fail the SLT. The failing structural patterns of a chip that passes the SLT are called *'SLT pass'*. The failing structural patterns of a chip that fails the SLT are called *'SLT fail'*.
Note that a failing structural pattern that detects a chip that passes the SLT, may also detect another chip the fails the SLT. Hence, this pattern is called both 'SLT pass' and 'SLT fail' or also called *'Common'*.

Example 4.2.2.1: Pattern 1, 2, and 4 fail the structural test of the chips that pass the SLT (i.e., Chip 1 and 3). Therefore, pattern 1, 2, and 4 are called 'SLT pass'.
Pattern 2 and 3 fail the structural test of the chip that fails the SLT (i.e., chip 2). Therefore, pattern 3 is called 'SLT fail'.
Pattern 2 is called both 'SLT fail' and 'SLT pass'. Hence, Pattern 2 is also called 'Common'

Definition 4.2.2.2 (Failing Scan chain of SLT Pass, Fail, or Common)*:* The failing scan chains of a chip that passes the SLT are called *'failing scan chains of SLT pass'*. The failing scan chains of a chip that fails the SLT are called *'failing scan chains of SLT fail'*.
A failing scan chain that is called 'failing scan chain of SLT pass' and 'failing scan chain of SLT fail' is also called *'failing scan chain of Common'*.

Example 4.2.2.2: Scan chain 1 and 2 capture the failing bits of chip 1 and 3. Because chip 1 and 3 pass the SLT, scan chain 1 and 2 are 'failing scan chains of SLT pass'.
Scan chain 1, 2, and 3 capture the failing bits of chip 2, which fails the SLT. Therefore, scan chain 1, 2, and 3 are 'failing scan chains of SLT fail'.
Scan chain 1 and 2 are common. Hence, they are called 'failing scan chains of Common'.

Definition 4.2.2.3 (Failing Scan cell of SLT Pass, Fail, or Common)*:* The failing scan cell of a chip that passes the SLT is called *'failing scan cell of SLT pass'*. The failing scan cell of a chip that fails the SLT is called *'failing scan cell of SLT fail'*.
A failing scan cell that is called 'failing scan cell of SLT pass' and 'failing scan cell of SLT fail' is also called *'failing scan cell of Common'*.

Example: Scan cell 1 in scan chain 1 and scan cell 2 in scan chain 1 and 2 are 'failing scan cells of SLT pass' because they capture the failing bits of chip 1 and 3, which pass the SLT. Scan cell 3 in scan chain 1, scan cell 2 in scan chain 2, and scan cell 1 in scan chain 3 are 'failing scan cells of SLT fail' because they capture the failing bits of chip 2, which fails the SLT.
Note that scan cell 2 in scan chain 2 is called both 'failing scan cell of SLT pass' and 'failing scan cell of SLT fail'. Hence, we call scan cell 2 in scan chain 2 'failing scan cell of Common'.

The failing scan chains for each failing test pattern were collected. The number of failing patterns ranges from 1 to 366 patterns. However, the maximum number of failing

scan chains per chip was only three (only one chip has three different failing scan chains). Fig. 3 presents the summary of comparing the number of failing scan chains of the LOC transition test and the SSF test. Note that the failing scan chains of SLT pass are the union of the failing scan chains of common and the failing scan chains of SLT pass only.

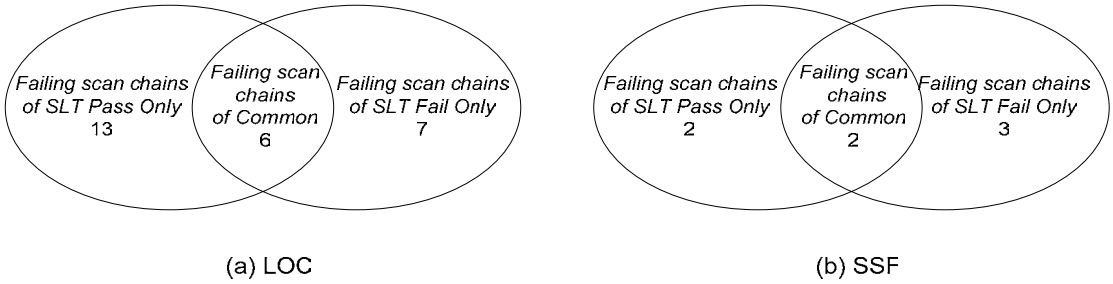


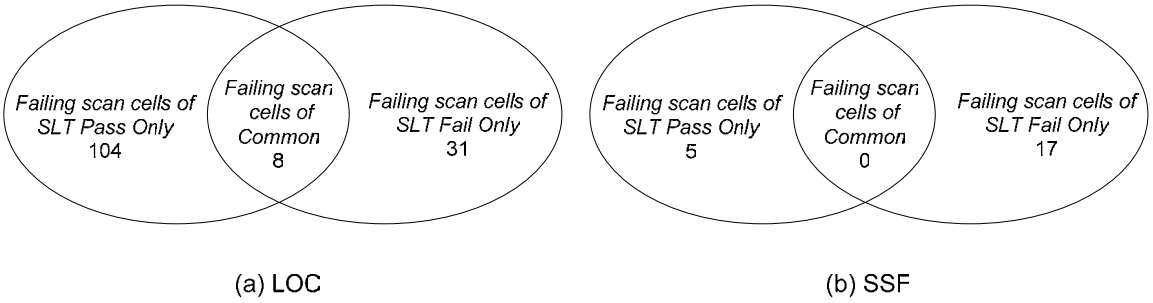
Figure 3 The number of failing scan chains for (a) LOC test and (b) SSF test

Fig. 3a demonstrates the results of 26 failing scan chains (i.e., 13 of 'SLT Pass Only', 6 of 'Common', and 7 of 'SLT Fail Only'). We have observed 19 failing scan chains in 15 yield loss candidates (i.e., 13 failing scan chains of SLT Pass Only and 6 of 'Common'). There are 7 failing scan chains that are only observed from the chips that fail the SLT.

Fig. 3b demonstrates the results of 7 failing scan chains (i.e., 2 from 'SLT Pass Only', 2 from 'Common', and 3 from 'SLT Fail Only') that were observed by applying SSF tests on the 27 interesting NV18 chips.

Note that the 'failing scan chains of Common' are 23% in Fig. 3a and 28 % in Fig. 3b out of total different failing scan chains.

Fig. 4 presents the summary of comparing the failing scan cells of the LOC transition test with the failing scan cells of the SSF test.



(a) LOC (b) SSF

Figure 4 The number of failing scan cells for (a) LOC test and (b) SSF test

The ‘failing scan cells of Common’ are 5.6% for the LOC transition test (see Fig. 4a). There are no ‘failing scan cells of Common’ for the SSF test (see Fig. 4b).

More than 20% of the total failing scan chains are commonly observed from the SLT failing chips and SLT passing chips (see Fig. 3). Fig. 4a demonstrates that only 5.6% of the failing scan cells are commonly observed from the SLT failing chips and SLT passing chips.

Our experiments demonstrate that a small number of failing scan cells captures a large amount of failing bits (also called *clustering*). For example, Fig. 5 presents the clustering of the 104 ‘failing scan cells of SLT Pass Only’ for the LOC transition test.

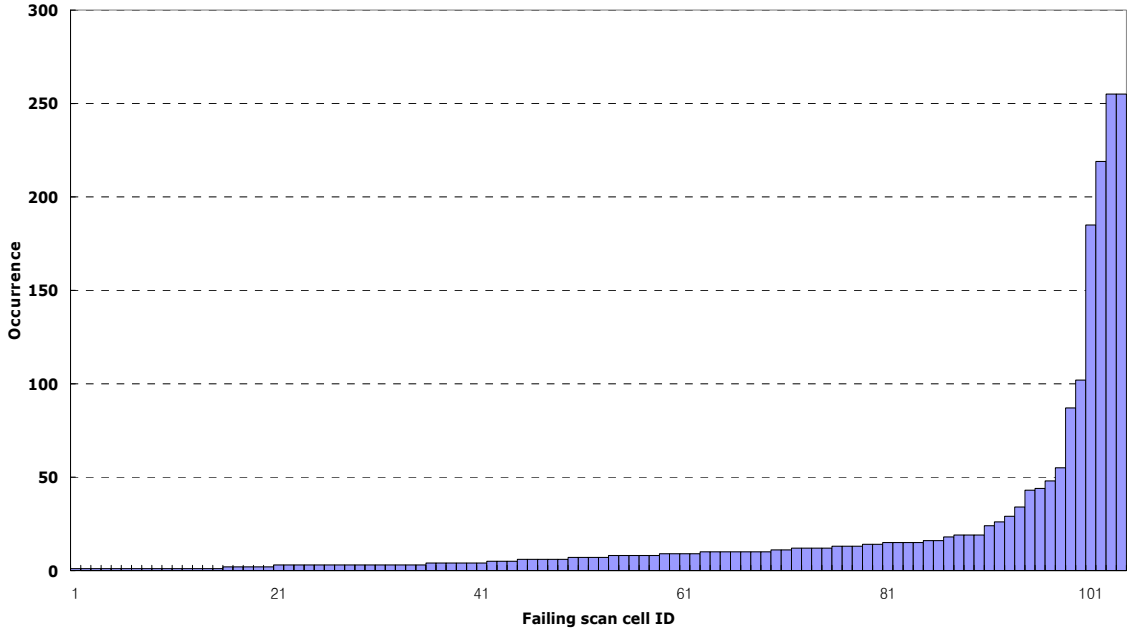


Figure 5 Clustering - Failing scan cells of SLT Pass Only, LOC test

The X-axis represents each failing scan cell (represented by an identification number) and the Y-axis represents the number of failing bits captured at each failing scan cell. The results demonstrate that 10% of the ‘failing scan cells of SLT Pass Only‘ captures 64% of the total failing bits. The remaining 90% of the ‘failing scan cells of SLT Pass Only’ captures 36% of the total failing bits.

The LOC transition test resulted in 31 ‘failing scan cells of SLT Fail Only’ (see Fig. 4a). Fig. 6 presents the clustering of the 31 failing scan cells.

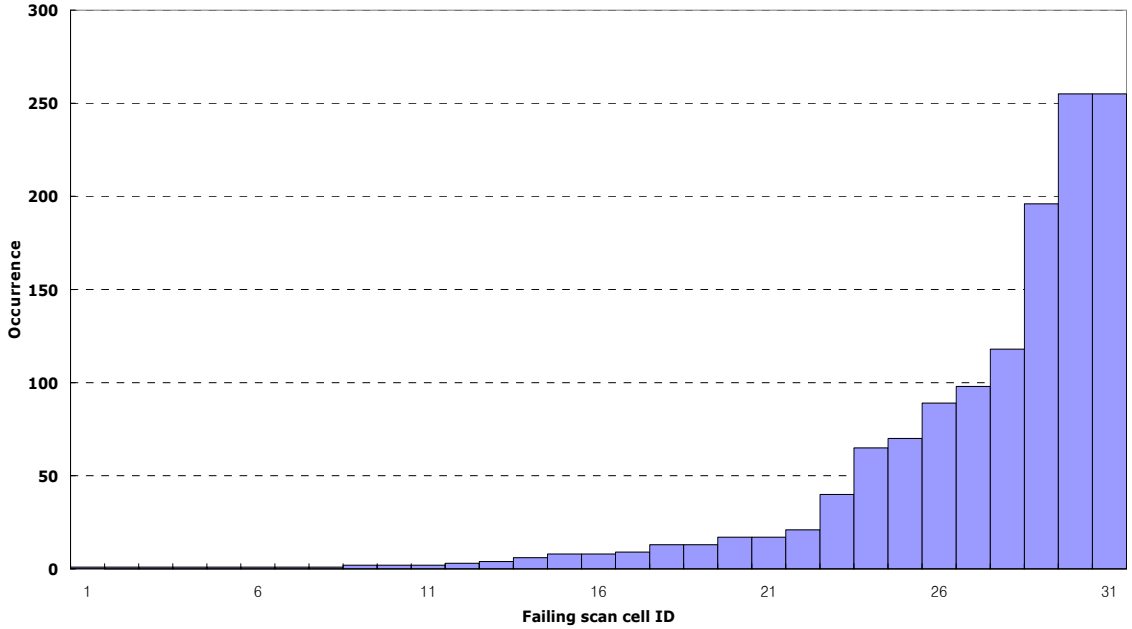


Figure 6 Clustering - Failing scan cells of SLT Fail Only, LOC test

10% of the ‘failing scan cells of SLT Fail Only’ captures 54% of total failing bits in the LOC transition test. The remaining 90% of the ‘failing scan cells of SLT Fail Only’ captures 46% of total failing bits in the LOC transition test.

Fig. 7 presents the results of the 8 ‘failing scan cells of Common’ for the LOC transition test (see Fig. 4a).

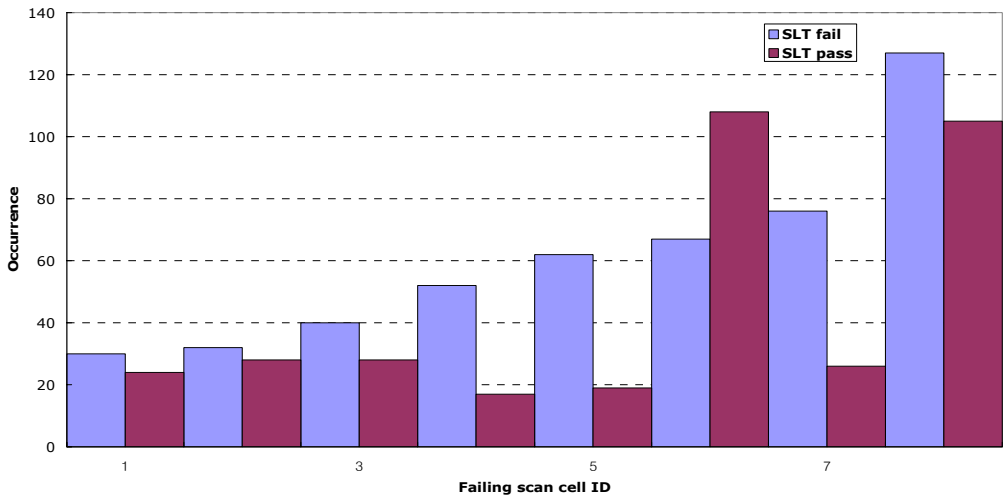


Figure 7 Clustering - Failing scan cells of Common, LOC test

12% of the ‘failing scan cells of Common’ (see the red bar in Fig. 7) captures 30% of the failing bits of the total failing bits. 12% of the ‘failing scan cells of Common’ (see the blue bar in Fig. 7)’ captures 26% of the failing bits of the total failing bits.

Compared to ‘failing scan cells of SLT Pass Only’, clustering of ‘failing scan cells of Common’ is reduced from 64% to 30% (for SLT pass) and 26% (for SLT fail). Compared to ‘failing scan cells of SLT Fail Only’, clustering of ‘failing scan cells of Common’ is reduced from 54% to 30% (for SLT pass) and 26% (for SLT fail).

Fig. 8 and Fig. 9 present the results of analyzing the clustering of SSF tests.

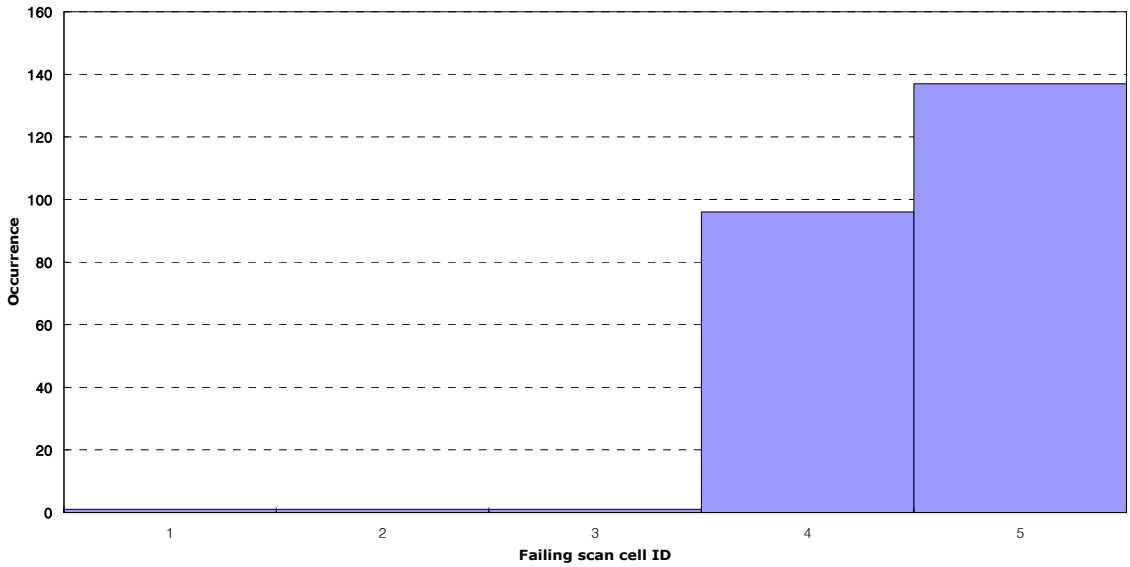


Figure 8 Clustering - Failing scan cells of SLT Pass Only, SSF test

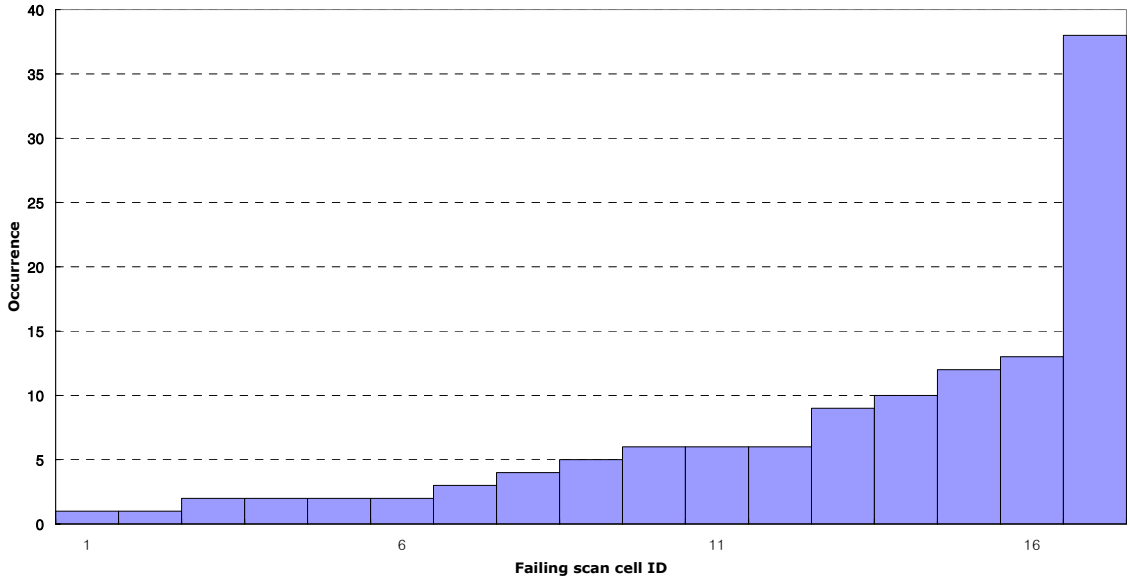


Figure 9 Clustering - Failing scan cells of SLT Fail Only, SSF test

11% of the ‘failing scan cells of SLT Fail Only’ capture 42% of the failing bits.

5 NV2B Experiments

5.1 Test flow

Fig. 10 presents the test flow.

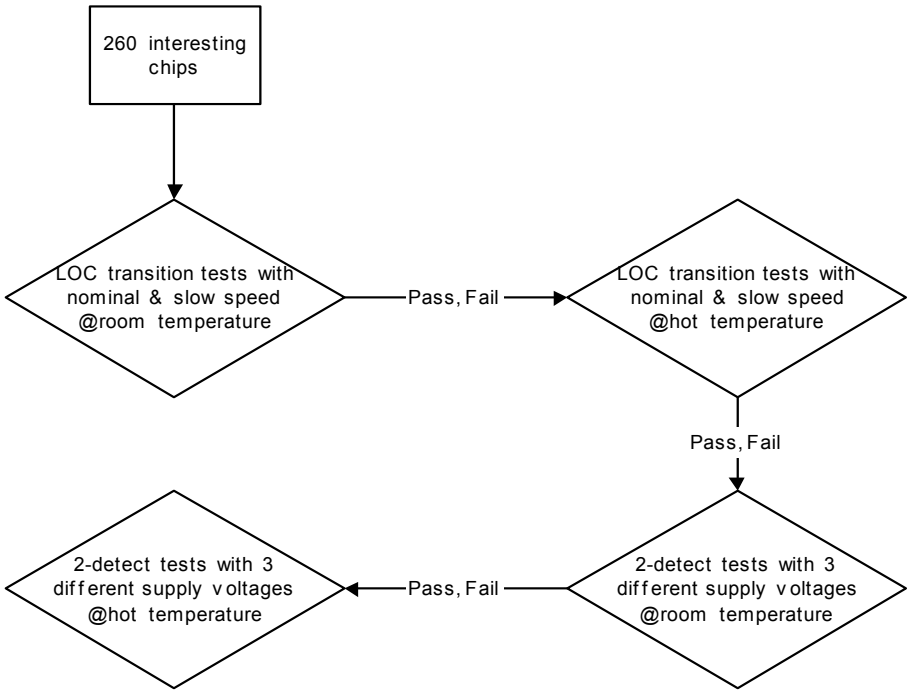


Figure 10 NV2B Test flow

260 chips that fail the LOC transition test at hot (100°C) temperature but pass the LOC transition test at room (25°C) temperature were collected. We will refer to these chips as being *interesting chips.* Nvidia selected 260 interesting chips and we applied the experiments with our own test sets and test conditions.

Table 5 presents the test sets applied to the interesting NV2B chips.

Table 5 Test conditions

Test	Test conditions			
	Test set	Speed (MHz)	Voltage (V)	Temperature (°C)
Test 1	LOC	Nominal	1.355	25
Test 2	LOC	10	1.355	25
Test 3	2-detect	<10	0.9	25
Test 4	2-detect	<10	1.355	25
Test 5	2-detect	<10	1.6	25
Test 6	LOC	Nominal	1.355	100
Test 7	LOC	10	1.355	100
Test 8	2-detect	<10	0.9	100
Test 9	2-detect	<10	1.355	100
Test 10	2-detect	<10	1.6	100

A defect that does not depend on the clock speed is also called a *timing-independent defect* [McCluskey 04] [Chang 98]. A defect that is not a *timing-independent defect* is called a *timing-dependent defect* [McCluskey 04] [Chang 98]. The LOC transition test patterns were applied at very slow speed to differentiate the timing-dependent defects from timing-independent defects.

2-detect test patterns were applied at three different supply voltages to investigate the voltage dependent defects: low *Vdd (0.9V)*, nominal *Vdd (1.355V)*, and high *Vdd (1.6V)*. Table 6 presents the summary of the test length and the fault coverage of the test sets.

Table 6 Structural test sets

Test set	Test set length	Fault coverage (%)
LOC[2]	409	72%
2-detect	11,777	94.3%

[2] Test patterns of higher fault coverage are currently being generated.

5.2Test Results

5.2.1 Temperature dependency of Test escapes

Fig. 11 presents the classification of test escapes in (1) chips that fail the tests at room temperature (25°C), but escape the tests at hot temperature (100°C), (2) chips that escape the tests at both hot and room temperature, and (3) chips that fail the tests at hot temperature, but escape at room temperature.

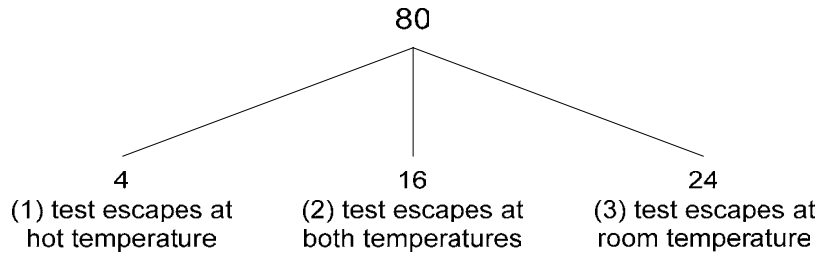


Figure 11 Classification of test escapes

Table 7 presents detailed test results of the chips that fail at room temperature, but escape the tests at hot temperature.

Table 7 Test escapes at hot temperature detected at room temperature

chip ID	2det low vdd	2det nom vdd	2det high vdd	LOC slow speed	LOC nom speed
1	P	F	P	P	P
22	P	F	P	P	P
45	F	P	P	F	F
70	F	P	P	P	F
# of detection	2	2	0	1	1

Table 8 presents detailed test results of the chips that fail at hot temperature, but escape the tests at room temperature.

Table 8 Test escapes at room temperature detected at hot temperature

chip ID	2-det low vdd	2-det nom vdd	2-det high vdd	LOC slow speed	LOC nominal speed
3	P	P	P	P	F
5	F	P	P	P	F
6	P	P	F	P	F
8	P	P	P	P	F
9	F	P	P	P	F
11	P	P	P	P	F
12	P	F	P	P	F
13	F	P	P	P	P
15	F	P	P	P	F
16	P	P	P	P	F
18	F	P	P	P	P
21	F	F	F	P	P
26	P	F	F	F	F
32	P	P	P	P	F
33	F	P	P	P	P
38	P	P	P	P	F
42	F	P	P	P	P
46	P	P	P	P	F
47	F	P	P	P	F
49	F	P	P	P	F
50	P	P	P	P	F
62	P	F	F	P	P
65	F	F	F	P	P
72	F	P	P	P	P
# of detection	12	5	5	1	16

20 more test escapes were observed at room temperature in comparison to the number of test escapes at hot temperature.

5.2.2 Timing-dependent defects

Test 2, 3, 4, and 5 from Table 5 are applied to identify the timing-dependent defects. Chips that fail test 1 (i.e., the LOC nominal speed transition test at room temperature), but pass tests 2, 3, 4, and 5 (i.e., the LOC slow speed transition test and 2-detect tests with low Vdd, nominal Vdd, and high Vdd, all at room temperature) are considered to have timing-

dependent defects. At room temperature, 20 chips fail the LOC nominal speed transition test. At hot temperature, 36 chips fail the LOC nominal speed transition test, and 14 chips fail at both temperatures. Fig. 12 presents the delay defect classification. The numbers in parenthesis in Fig. 12 presents the number of chips that have timing-dependent defects.

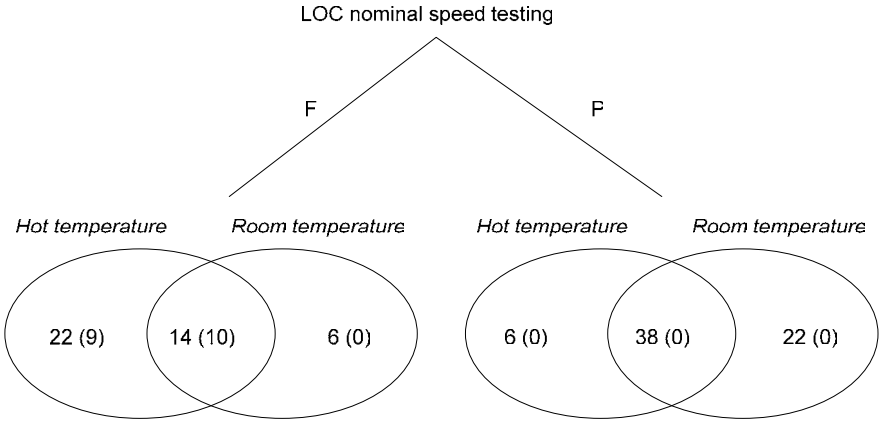


Figure 12 Delay defect classification

Among 80 chips, 19 chips have timing-dependent defects and no timing-independent defects. All six chips that fail the LOC transition test at room temperature, but pass the LOC transition test at hot temperature, also fail one of the test 2, 3, 4, and 5 (i.e., the LOC slow speed transition test and 2-detect tests with low Vdd, nominal Vdd, and high Vdd, all at room temperature) more than once: 6 chips have timing-dependent defects and timing-independent defects. Out of 14 chips that fail the LOC transition test at both temperatures, 10 chips pass all other tests. Therefore, 10 chips only have timing-dependent defects (and no timing-independent defects). Among 22 chips that fail the LOC transition test at hot temperature, but pass the LOC transition test at room temperature, 9 chips pass all other tests. Therefore, 9 chips only have timing-dependent defects (and no timing-independent defects). Out of those 9 chips, 8 escape all tests including LOC nominal speed transition test. One chip fails all test sets.

5.2.3 Slow speed and 2-detect testing

The slow speed LOC transition test and the 2-detect test with three different supply voltages were applied to identify the chips that have timing-independent defects. Chips that fail at least one 2-detect test pattern set (see Test 3, 4, 5, 8, 9, and 10 in Table 5) are also called *2-detect failures*.

At hot temperature, 41 chips are 2-detect failures. 37 out of 41 chips pass the slow speed LOC transition test. At room temperature, 30 chips are 2-detect failures. 23 chips out of 30 chips pass the slow speed LOC transition test. All chips that fail the slow speed LOC transition test were also 2-detect failures.

5.2.4 Voltage dependent behavior

Chips that fail the 2-detect tests (i.e., test 3, 4, 5, 8, 9, and 10 in Table 5) were further analyzed to investigate the effect of supply voltage changes on test results. Fig. 13 presents the classification of 2-detect failures.

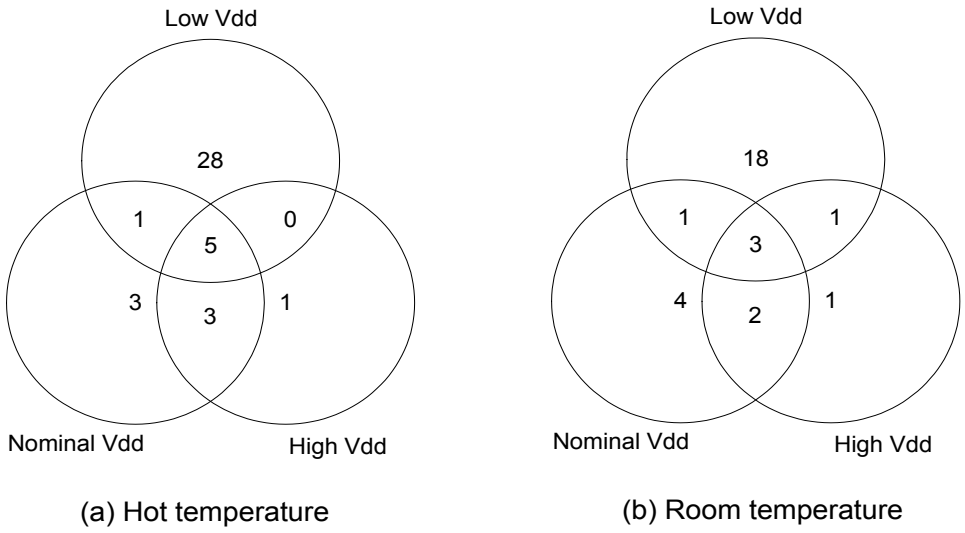


Figure 13 Classification of *2-detect failures for (a) hot temperature and (b) room temperature*

At hot temperature, 83% of the 2-detect failures occurred at a low supply voltage. At room temperature, 77% of the 2-detect failures occurred at a low supply voltage. When VLV testing is applied at high temperature, the number of chips that are only detected by VLV testing increase from 18 (see Fig. 13b) to 28 (see Fig. 13a). The number of chips that

were detected by either nominal voltage or high voltage testing was temperature independent.

6 ELF35 Experiments

6.1 Test flow

Fig. 14 presents the ELF35 test flow.

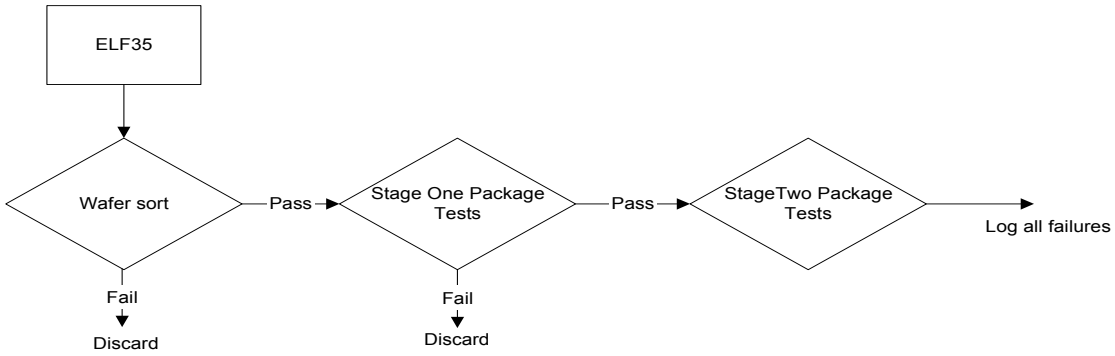


Figure 14 ELF35 Test flow

Any chip that fails the first package stage tests did not go on to the next stage. Any chip that passes the first package tests, but fails some or all of the second stage package tests we call "interesting cores". A total of 495 interesting cores are identified. Details of classification of the interesting cores are in [McCluskey 04]. Details of the wafer and package tests are in [Li 99].

A transition delay test set is generated to detect both the slow-to-rise and the slow-to-fall faults in each node in the circuit – this is referred to as a *double-sided transition test* set. A transition test set that is designed to detect either the slow-to-rise or the slow-to-fall fault in each node is called a *single-sided transition test set* [Benware 03].

If the yield loss occurs because the scan-based transition test is too thorough or detects faults that should not have been detected, applying a less thorough test set may reduce yield loss. A single-sided transition test set is less thorough than double-sided transition test set because it targets only one transition fault instead of both transition faults in each node.

Single-sided transition test sets were applied to 324 defective ELF35 cores to evaluate the effectiveness of single-sided transition test sets. The single-sided transition patterns were generated from commercial ATPG tool.

We will also analyze the reduction in the number of test patterns. The test set size reduction is calculated using the following equation.

$$\text{Test set size reduction} = \frac{\text{Double-sided transition test set length - Single-sided transition test set length}}{\text{Double-sided transition test set length}} \times 100$$

6.2 Test results

Table 9 presents the test results of single-sided transition test sets.

Table 9 Experimental Results on single-sided Transition Delay Patterns on ELF35

		Double-sided transition test set		Single-sided transition test set		Test set size reduction (%)
	Defective cores	Test set length	Escapes	Test set length	Escapes	
LSI	92	786	1	343	0	56.36
TOPS	30	957	0	440	0	54.02
M12	38	105	0	56	0	46.67
MA	28	131	0	72	0	45.04
PB	133	5604	0	2945	0	47.45
SQR	15	48	0	30	1	37.50

Although the single-sided transition test sets have smaller number of patterns than double-sided transition test sets (see table 9), there was only one increase in test escapes for the SQR core (see chapter 2, page 5 for an overview of the ELF35 cores). The single-sided transition test set caused a reduced number of LSI core escapes compared to the double-sided transition test set. The number of test escapes of single-sided transition test was the same as the number of test escapes of the double-sided transition test if applied to TOPS, M12, MA, and PB cores.

7 ELF18 Experiments

7.1 Test flow

Fig. 15 presents the ELF18 test flow.

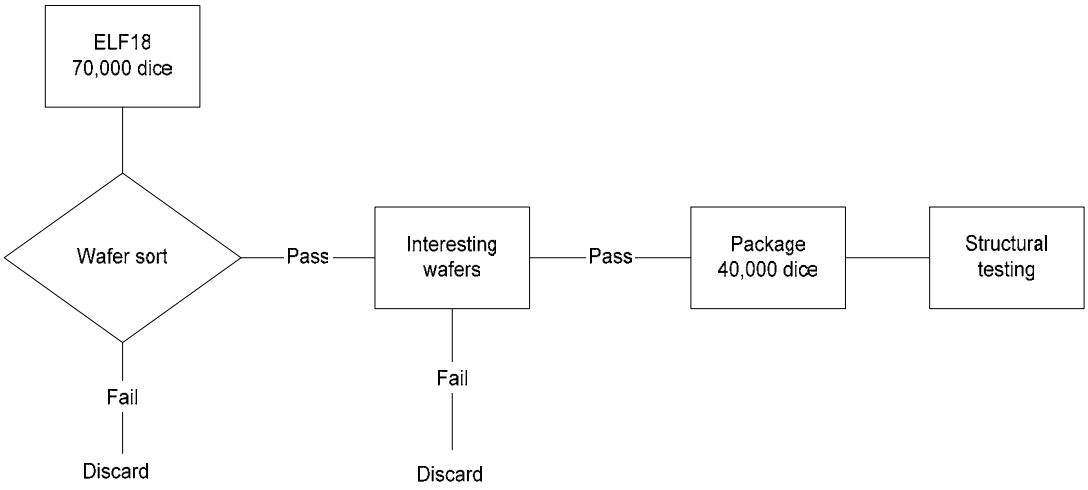


Figure 15 ELF18 Test flow

Wafer sort tests were applied to about 70,000 dice. Wafers with a number of chips that failed a certain set of tests were classified as interesting wafers. All the dice on a subset of interesting wafers were packaged. Subsequently, we've applied additional tests to filter the interesting dies. We have applied our experiments on the set of interesting dies.

7.2 Test results

Both single-sided transition patterns and double-sided transition patterns were applied to ELF18. Table 10 presents the comparison of single-sided transition test set and double-sided transition test set experiments.

Table 10 Experimental Results on single-sided Transition Delay Patterns on ELF18

Number of defective cores	Transition test set	Test set length	Number of test escapes	Test set size reduction (%)
464	Double-sided	757	1	NA
	Single-sided	347	4	54.20

The single-sided transition test caused three more defective escapes than the double-sided transition test. Test set length is significantly reduced from 757 to 347 (54.2%).

8 Summary

One of the main challenges in researching test escapes and yield loss is the danger of drawing conclusions from only a few data points. We have developed an extensive test infrastructure to allow test escape and yield loss experiments on multiple EDA tools (commercial and academic), multiple ATEs, multiple test chips of multiple technologies (from multiple vendors).

A test in which the chip is inserted into a system that tests the functionality of a chip according to a functional specification is called a *System Level Test (SLT)*. Failing scan chains and failing scan cells of chips that passed SLT were compared to failing scan chains and failing scan cells of chips that failed SLT. We can make the following 3 observations:

1. Some failing scan cells are only associated with the chips that passed SLT. Hence, false path may be sensitized through those scan cells.
2. Some failing scan cells are only associated with the chip that failed SLT. Hence, the scan cells only capture the valid failing bits and are not associated with false path sensitization.
3. Only a very few failing scan cells (<5%) captures failing bits associated with both chips that passed SLT and chips that failed SLT.

   This paper proposed metrics to quantify above observations.

We identified the clustering of failing scan cells: 10% of the failing scan cells capture more than 50% of the total failing bits.

Two structural test sets with 10 different test conditions were applied to NV2B chips. Our experiments suggest that test escapes are reduced if the same test sets are applied at a hot temperature compared to room temperature. Based on our experiments, we identified 19 chips that have timing-dependent defects and no timing-independent defects. Among those 19 chips, 9 chips could be identified only at hot temperature. Out of those 19 chips, 10 chips could be identified at both room and hot temperature. Our experiments suggest that all chips that fail the LOC slow speed transition test also fail the 2-detect test. Our experiments suggest that VLV testing detects more defective chips than nominal or high

voltage testing. Moreover, our experiments suggest that the effectiveness of VLV test is more emphasized when temperature is increased.

Single-sided transition test patterns are applied to ELF35 and ELF18 chips. Our experiments suggest that test set size can be reduced by 56% by using single-sided transition test patterns compared to using double-sided transition test patterns. In four cores of the ELF35 chip, the number of test escapes of the single-sided transition test patterns was the same as that in double-sided transition test patterns. We observe an increase in the number of SQR test escapes (ELF35) and ELF18 test escapes.

9 Future work

The last year, we have spent a lot of time and effort to make the infrastructure. We intend to continue to use the infrastructure to get more experimental results in order to draw more conclusions and to meet the objectives of our research program.

References

[Benware 03] Benware, B.R., Madge, R. Lu, C. and Daasch, R., "Effectiveness Comparisons of Outlier Screening Methods for Frequency Dependent Defects on Complex ASICs," *VLSI Test Symposium, 2003, Proceedings. 21st*, 27 April – 1 May pp. 39-46.

[Chang 96a] Chang, J.T.-Y. and McCluskey, E.J., "Quantitative analysis of very-low-voltage testing," *VLSI Test Symposium,1996, Proceedings. 14th*, 28 April – 1 May pp. 332-337.

[Chang 96b] Chang, J.T.-Y. and McCluskey, E.J., "Detecting delay flaws by very-low-voltage testing," *Proc. Intl. Test Conf.*, pp. 367-376, 1996.

[Chang 98] Chang, J.T.-Y., Chao-Wen Tseng, Yi-Chin Chu, Wattal, S., Partell, M. and McCluskey, E.J." Experimental results for IDDQ and VLV testing,*" VLSI Test Symposium, 1998. Proceedings. 16th IEEE , 26-30 April 1998,* pp. 118 – 123

[Franco 91] Franco, P., and McCluskey, E.J., "Delay Testing of Digital Circuits by Output Waveform Analysis," *Proc. 1991 Int. Test Conf.*, Nashville, TN, pp. 798-807, Oct. 26-30, 1991.

[Franco 94] Franco, P., et al., "An Experimental Chip to Evaluate Test Techniques, Part 1: Description of Experiment," *Stanford University CRC Technical Report*, No. 94-5, 1994

[Franco 95] Franco, P., et al., "An Experimental Chip to Evaluate Test Techniques Chip and Experiment Design," *Proc. 1995 ITC, Washington, D.C.*, pp. 653-662, Oct. 21-25, 1995

[Hao 93] Hao, H., and E.J. McCluskey, "Very-Low-Voltage Testing for Weak CMOS Logic IC's," *Proc. 1993 Int. Test Conf.*, Baltimore, MD, pp. 275-284, Oct. 17-21, 1993. (CRC TR 93-1 and CRC TR 93-2)

[Kim 03] Kee Sup Kim, Mitra, S. and Ryan, P.G., "Delay Defect Characteristics and Testing Strategies," *Design & Test of Computers*, IEEE , Volume: 20 , Issue: 5 , Sept.-Oct. 2003 pp. 8 – 16.

[Kievits 98] Kievits, P., E. Lambers, C. Moerman and R. Woudsma, “R.E.A.L. DSP Technology for Telecom Broadband Processing,” *Proc. Intl. Conf. Signal Processing Applications and Technology*, 1998

[Kusko 01] Kusko, M., B.J. Robbins, T.J. Koprowski and W.V. Houtt, “99% AC test coverage using only LBIST on the 1 GHz IBM S/390 zSeries 900 Microprocessor,” *Proc. Intl. Test Conf.*, pp. 586-592, 2001.

[Lee 04] Lee, D., and E.J. McCluskey, “Experimental Data on Test Escapes”, SRC annual report, Dec. 2004

[Lesser 80] J. D. Lesser and J. J. Shedletsky, “An Experimental Delay Test Generator for LSI Logic,” IEEE Trans. Computers, Vol. C-29, No. 3, pp. 235-248, 1980

[Li 01] Li, J.C.M., J.T.-Y. Chang, C.W. Tseng, and E.J. McCluskey, "ELF35 Experiment - Chip and Experiment Design, CRC TR 99-3, Oct. 1999.

[Li 02] Li, J. C.M., “Test and Diagnosis of Open Defects in Digital CMOS Integrated Circuits,” TR 02-1, Center for Reliable Computing, Stanford University, 2002.

[Ma 95] Ma, S.C., P. Franco, and E.J, McCluskey, “An Experimental Chip to Evaluate Test Techniques Experimental Results,” *Proc. 1995 Int. Test Conf.*, pp. 663-672.

[McCluskey 00] McCluskey, E.J., Chao-Wen Tseng, “Stuck-fault tests vs. actual defects,” *Proc. Intl. Test Conf.*, pp. 336-343, 2000.

[McCluskey 04] McCluskey, E.J., A.A. Al-Yamani, C.M. Li, C.W. Tseng, E. Volkerink, F. Ferhani, E. Li and S. Mitra, “ELF-Murphy Data on Defects and Test Sets,” *VLSI Test Symposium, 2004, Proceedings. 22th*, 25 April-29 April pp. 16 – 22.

[Millman 88] Millman, S.D.and McCluskey, E.J., *“*Detecting bridging faults with stuck-at test sets,**”** *Proc. Intl. Test Conf.*, pp. 773-783, 1988.

[Rearick 01] Rearick, J., “Too Much Delay Fault Coverage is a Bad Thing,” *Proc. Intl. Test Conf.*, pp. 624-633, 2001.

[Saxena 02] Saxena, J., Butler, K.M., Gatt, J., Raghuraman, R., Kumar, S.P., Basu, Campbell, D.J. and Berech, J., “Scan-based transition fault testing - implementation and low cost test challenges,” *Proc. Intl. Test Conf.*, pp. 1120-1129, 2002.

[Shedletsky 78] J. J. Shedletsky, “Delay Testing LSI Logic,” Dig. 8th Annu. Int. Symp. Fault-Tolerant Comput., pp. 159-164, 1978

[Smith 85] G. L. Smith, “Model for Delay Faults Based upon Path,” *Proc. Intl. Test Conf.*, pp. 342-349, 1985

[Tseng 01] Chao-Wen Tseng and McCluskey, E.J., “Multiple-output propagation transition fault test,” *Proc. Intl. Test Conf.*, pp. 358-366, 2001.

[Tseng 02] Chao-Wen Tseng and McCluskey, E.J., “Experimental results for slow-speed testing,” *VLSI Test Symposium, 2002, Proceedings. 20th*, 28 April-2 May pp. 37 – 42.