Classifying Bad Chips and Ordering Test Sets

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Abstract

This paper shows data related to choosing a pair of test sets for Digital IC production test. This data demonstrates that the choice of the second set of the pair should take into account the test metric used for the first test set. An approach for making this choice by taking defect coverage and total test length into account is presented.

1. Introduction

Previous work [Maxwell 93] [Nigh 97] has shown the importance of using different metrics to test integrated circuits. Production testing of digital ICs often applies two test sets. These test sets are derived using two different test metrics: single-stuck fault and transition fault for example. This paper addresses the question of how to choose the pairs of test metrics.

Each test pattern is a sequence of input combinations and we classified our defective chips according to their sensitivity to the sequence or timing in which these input combinations are applied. Those chips whose response to a test set depends on the sequence in which they are applied are called *sequence dependent chips*. If, in addition, the response depends on the speed of application, they are called *sequence and timing dependent*. The remaining chips are called *timing independent combinational chips* or *TICs* for short. Figures 1, 2 and 3 show the classification for the three chips studied here.

Not too surprisingly, we found that the effectiveness of test metrics varies according to the defective class of the chip being tested. The single-stuck fault metric is very effective in detecting TIC chips but not as effective as the transition fault test metric for sequence-dependent chips.

In [McCluskey 04] the authors compare the effectiveness of different test metrics by applying different test sets and comparing the number of escapes. In this paper we show new results by comparing their effectiveness for different defective chip classes. We do so by taking into account the defective behavior of the escapes in addition to comparing their number.

Previous work studied the physical characteristics of defects in order to find better tests [Hawkins 94] or understand yield learning [Maly 03]. Defect-based testing research studies how to test integrated circuits based on those physical characteristics [Soden 95] [Baker 99] [Segura 02] [Sengupta 99]. In this paper however, we only take into account the behavior of the defective chip instead of the defect's physical characteristics and our goal is to find the right combination of metrics to test them.

The paper is organized the following way: section 2 describes the experiment: the test chips and their defective classification. Section 3 presents the data collected in the

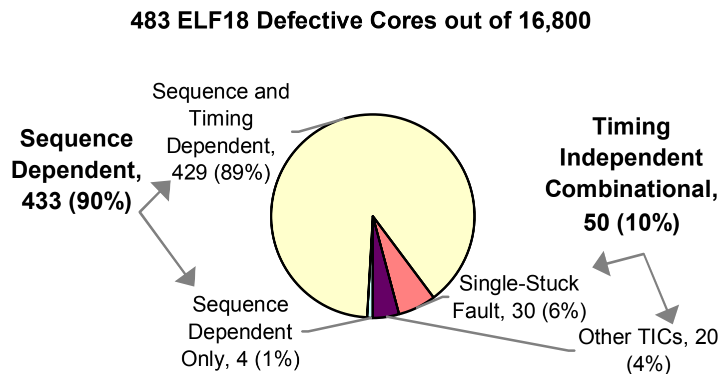

Figure 1: ELF18 Defective Chip Classification

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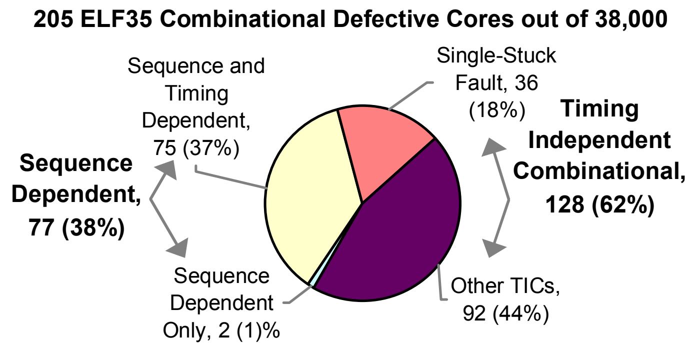

Figure 2: ELF35 Defective Chip Classification

study described here. Section 4 concludes on how to choose test metrics and how to order them.

2. Experiment

2.1. Test Chips

For our experiment we applied our test sets on three designs in three different CMOS technologies: ELF18 (0.18μm), ELF35 (0.35μm) [McCluskey 04], and Murphy (0.7μm) [Franco 95]. LSI Logic and Philips manufactured 2,800 ELF18 chips, 9,000 ELF35 chips, and 5,500 Murphy chips for our experiment. ELF18 has 320,000 gates implementing six instances of a sequential core, ELF35 has 265,000 gates implementing forty-four instances of two sequential and four combinational cores, and Murphy has 25,000 gates implementing twenty instances of five different combinational cores. The sequential cores are full-scan. Supply voltages are 1.8 V for ELF18, 3.5 V for ELF35, and 5 V for Murphy. Since gross failures are generally easy to test, the ability of tests to detect the difficult failures is more important for achieving high quality levels [Franco 95]. We therefore started by taking the chips with gross failures out of our sample. We listed the tests we used for this in the appendix. We then tested all cores in every chip as thoroughly as possible (e.g. we applied I_{DDQ}, structural and exhaustive tests in different test conditions [Ma 95] [McCluskey 04]). A chip fails a structural or exhaustive test if one of its outputs has an erroneous value and it fails an I_{DDQ} test if it is above a certain current threshold (see the appendix for more details). We varied the test condition by varying the supply voltage and the timing of the test: for ELF18, we applied each test at two different supply voltages (1.8-V and 0.65-V) and three different timings (fastest, 20% slower and three times slower); for ELF35, we applied each test at two different supply voltages (3.5-V and 1.4-V) and three different test speeds (fastest, 20% slower and three times slower); and for Murphy, we applied each test at three different supply voltages (5-V, 2.5-V and 1.7-V) and four different timings (fastest, 20% slower, three times slower and thirty times slower). We compiled more information about the chips and their tests in the appendix.

In the chips without gross failures, 483 ELF18 cores, 205 ELF35 combinational cores, and 116 Murphy cores failed at least one of the applied tests. We study those 804 cores in our experiment.

2.2. Defective Chip Classes

When a test set is applied to a core, its *failure trace* is the list of patterns and observable points (flip-flops or

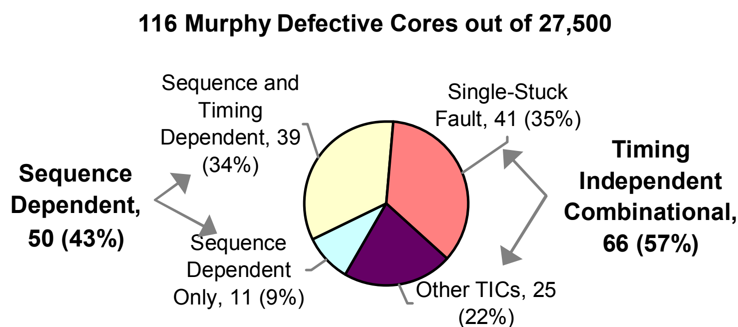

Figure 3: Murphy Defective Chip Classification

outputs) that failed, if any. The failure trace of some of our defective cores depends on the sequence and the timing of the input combinations forming the patterns. We used this property to classify our defective cores into three defective chip classes.

- The defective cores whose failure trace is always the same whatever the sequence or the timing of the input combinations forming the patterns. We named those *Timing Independent Combinational* (TICs). Defects behaving like stuck-at or bridging faults can explain this behavior. We ran several single-stuck fault diagnosis tools to find which of the TICs behaved like single-stuck faults
- The defective cores whose failure trace depends on the sequence of the input combinations forming the patterns but not their timing. We named those *Sequence Dependent Only* (SD) and their behavior can be explained for example by a defect behaving like a stuck-open fault [Li 02].
- The defective cores whose failure trace depends on both the sequence and the timing of the input combinations forming the patterns. We named those *Sequence and Timing Dependent* (TD) and their behavior can be explained for example by a delay fault.

Timing dependent cores are all sequence dependent since their timing dependence implies that a transition occurs early or late and this transition is created by the sequence of input combinations forming the patterns.

We changed this sequence to change the sequence of logic values on the circuit nodes. For combinational cores each pattern contains only one input combination, so we can change the sequence of logic values on the circuit nodes by simply shuffling the patterns. For a full-scan core however, each pattern contains several input combinations because of the scan shift, so shuffling the patterns would not change the sequence of logic values on the circuit nodes because this sequence is determined by the scan shift. To solve this problem, we applied to our full-scan cores a launch on capture and a launch on shift test with the same expected values. Figure 4 shows how shifting in the same logic state than after the first clock cycle of the launch on capture test set changes the sequence of values on the circuit nodes without changing the expected values of the pattern.

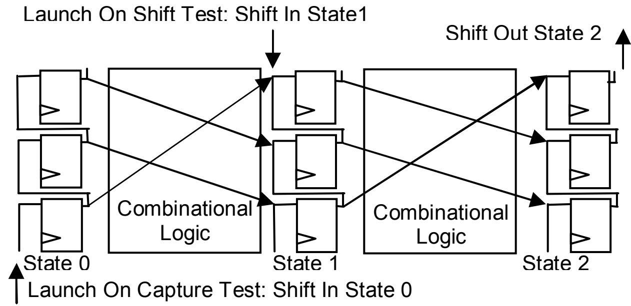

Figure 4: Launch on capture and launch on shift tests with same expected values

In addition to changing the sequence of the input combinations, we also changed their timing to do the classification and Figures 1, 2 and 3 show the results.

We found that a majority of defective cores were TICs but as technology evolved the sequence and timing dependent cores outnumbered them.

2.3. Test Metrics

This experiment compares the effectiveness of the following test metrics: single-stuck fault, transition fault, N-Detect [Ma 95] [McCluskey 04] gate exhaustive [McCluskey 93] [Cho 05] and TARO [Tseng 01] [Park 05].

A single-stuck fault occurs when a gate input or output has a fixed logic value, independently of the values of other signals. Figure 5 illustrates how single-stuck fault test sets detect single-stuck faults by setting the gate input or output at the opposite of its stuck value and by sensitizing this gate input or output to a flip-flop or a primary output.

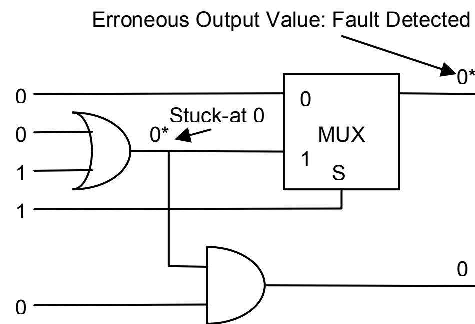

Figure 5: Single-stuck fault test set pattern detecting a single-stuck fault

A transition fault occurs when a gate input or output is slow to transition. Figure 6 illustrates how transition fault test sets detect transition faults by propagating a transition from the gate input or output to a flip-flop or a primary output.

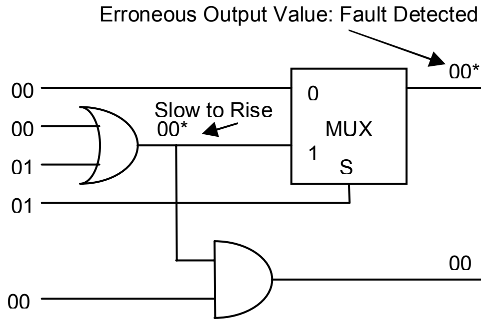

Figure 6: Transition fault test set pattern detecting a transition fault

N-Detect test sets [Ma 95] [McCluskey 00] detect the faults N times instead of just once.

Gate exhaustive test sets [McCluskey 93] [Cho 05] apply all possible input combination to each gate and observe the gate response at a flip-flop or a primary output.

TARO test sets [Tseng 01] [Park 05] propagate a transition from a gate input or output to all the flip-flops and primary outputs it can reach, whereas the transitions test sets propagate the transition to only one flip-flop or output.

3. Experimental Results

3.1. Defective Chip Class of Escapes

We applied one or more test sets generated with these metrics to our 804 defective cores. The test conditions were all the same: room temperature, nominal voltage: 1.8-V for ELF18, 3.5-V for ELF35 and 5-V for Murphy, and rated speed: 20% slower than the fastest we could test good chips.

652 of our 804 defective cores fail at least one test set under those conditions (the 152 remaining defective cores are only detected at a faster timing). 594 out of those 652

Table 1: ELF18 SSF, TR, gate exhaustive, N-Detect and TARO escapes and their defective chip class

(152 defective cores out of 483 can be detected at this speed, out of which 24 escape at least one of these test sets)

Test Sets	**Cores**																							
	Sequence and Timing Dependent																				SD	TIC SSF		
Test Length; SSF Fault Coverage; TR Fault Coverage	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
15-Detect Transition 18,726; 98.4%; 97.4%														E			E							
TARO 9,982; 98.3%; 97.4%														E										
15-Detect SSF 5,043; 98.4%; 96.5%		E	E	E	E			E	E	E	E	E	E	E	E	E	E	E	E	E	E			
2-Detect Transition 3,060; 98.2%; 97.3%		E	E		E									E			E				E			
5-Detect SSF 1,688; 98.4%; 95.1%		E	E	E	E			E	E	E	E	E	E	E	E	E	E	E	E	E	E			
Gate Exhaustive 1,556; 98.4%; 93.6%		E	E	E	E			E	E	E	E	E	E	E	E	E	E	E	E	E	E			
Transition Fault 1,453; 98.2%; 97.1%		E	E		E					E				E			E							
2-Detect SSF 674; 98.4%; 92.0%		E	E	E	E			E	E	E	E	E	E	E	E	E	E	E	E	E	E			
SSF 100% 437; 98.4%; 89.8%		E	E	E	E			E	E	E	E	E	E	E	E	E	E	E	E	E	E			
SSF 99% 226; 97.5%; 86.5%		E	E	E	E			E	E	E	E	E	E	E	E	E	E	E	E	E	E			
SSF 95% 107; 93.6%; 78.8%		E	E	E	E	E		E	E	E	E	E	E	E	E	E	E	E	E	E	E	E		
SSF 90% 61; 88.8%; 70.2%	E	E	E	E	E		E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E

Test Conditions: Room Temperature, Nominal Voltage (1.8V) and transition test at Rated Speed (70MHz)

defective cores fail all the test sets in this experiment. The 58 remaining defective cores are detected under those test conditions by some test sets, but not all. Tables 1, 2 and 3 show their test results and their defective chip class.

Table 2: ELF35 SSF, TR, gate exhaustive, N-Detect and TARO escapes and their defective chip class

(All 205 defective cores can be detected at this speed and 14 escape at least one of these test sets)

Test Sets Test Length; SSF Fault Coverage; TR Fault Coverage	Cores													
	Seq. And Tim. Dep.					SD	TIC NonSSF		TIC SSF					
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
15-Detect SSF 43,035; 99.3%; 99.2%														
TARO 29,208; 99.3%; 98.7%														
5-Detect SSF 14,727; 99.3%; 98.7%														
Transition Fault (Tool 2) 6,571; 99.3%; 99.2%			E			E								
2-Detect SSF 6,099 99.3%; 96.8%				E	E									
Transition Fault (Tool 3) 6,036; 98.3%; 97.6%										E				
Transition Fault (Tool 1) 5,888 99.2%; 98.9%														
Gate Exhaustive 4,027; 99.3% 95.0%														
SSF 100% (Tool 2) 3,371; 99.3% 93.4%					E	E								
SSF 100% (Tool 3) 3,204; 99.3% 92.5%				E	E									
SSF 100% (Tool 1) 3,165; 99.3%; 92.9%			E		E									
SSF 99% (Tool 2) 3,109; 98.8%; 92.2%					E	E								E
SSF 99% (Tool 3) 2,892; 98.4%; 90.8%				E		E								
SSF 99% (Tool 1) 2,840; 97.8%; 90.4%			E			E								
SSF 95% (Tool 2) 2,315; 95.2%; 86.0%					E	E						E	E	E
SSF 95% (Tool 1) 2,065; 95.1%; 85.4%			E		E									
SSF 95% (Tool 3) 2,060; 94.0%; 84.6%				E	E						E			
SSF 90% (Tool 2) 1,695; 90.8% 78.6%					E	E		E				E	E	E
SSF 90% (Tool 1) 1,503; 90.0% 79.1%	E	E	E		E		E					E	E	
SSF 90% (Tool 3) 1,461; 89.3% 76.2%				E	E				E	E	E			

Test Conditions: Room Temperature, Nominal Voltage (3.5V) and Rated Speed (16 to 61MHz depending on core type)

Table 3: Murphy SSF, TR, gate exhaustive, N-Detect and TARO escapes and their defective chip class

(All 116 defective cores can be detected at this speed and 20 escape at least one of these test sets)

Test Sets Test Length; SSF Fault Coverage; TR Fault Coverage	Cores																			
	Sequence and Timing Dependent										SD			TIC NonSSF			TICSSF			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
15-Detect SSF 7,186; 99.7%; 99.6%																				
5-Detect SSF 2,403; 99.7%; 98.8%																				
Transition Fault 1,426; 99.7%; 99.7%	E												E			E				
SSF 100% 547; 99.7%; 88.9%	E						E				E									
SSF 99% 443; 98.8%; 85.4%									E	E						E		E		
SSF 95% 351; 94.8%; 79.6%	E	E	E	E			E	E						E	E		E	E		
SSF 90% 262; 90.0% 71.3%	E	E	E	E	E	E					E	E	E		E	E	E	E	E	E

Test Conditions: Room Temperature, Nominal Voltage (5V) and Rated Speed (16 to 61MHz depending on core type)

Those tables show that, contrary to what we expected, the single-stuck fault test sets detected all our TICs. They also show that single-stuck fault test sets with less than 100% coverage escaped some TICs.

As reported in other silicon experiments [Benware 03] [Amyeen 04], the gate exhaustive and N-Detect test sets detect more defective cores than the single-stuck fault test set. Our results in tables 1, 2 and 3 show that those cores are sequence dependent (i.e. sequence dependent only or timing and sequence dependent).

The gate exhaustive and N-Detect test sets therefore did better than the single-stuck test sets only because they found more sequence dependent chips.

3.2. Sequence Dependent Coverage

To understand why N-Detect and gate exhaustive do so well with sequence dependent chips, we fault graded our test sets using different metrics and compared the results. Two metrics take into account the sequence of vectors: transition and TARO. We used these two metrics to fault grade our patterns, along with the single-stuck fault and bridging fault metrics which do not take the sequence of vectors into account. Tables 4, 5 and 6 show our results.

We found that N-Detect and gate exhaustive test sets have better sequence dependent coverage (ie transition fault or TARO coverage) than single-stuck fault test sets, which is consistent with our observation that they detect more sequence dependent cores. Figure 7 shows that the transition test coverage of single-stuck fault N-Detect patterns increases monotonically with N so the sequence dependent coverage increases with N although the single-stuck fault coverage stays the same. Furthermore, Tables 4, 5 and 6 show that N-Detect and gate exhaustive test sets have higher TARO coverage than the transition and single-stuck fault test sets. They cannot have higher transition coverage than the transition test set since this test set has been generated to have the highest possible transition coverage. Therefore, TARO seems to be a better metric than the other three to detect sequence dependent chips. Table 5 also shows that the gate exhaustive test set's high TARO coverage is not due to its longer length since it has higher TARO coverage than other test sets of similar length.

Test coverage is a different measure of test quality than fault coverage in that it ignores the untestable single-stuck and transition faults. Test sets therefore have higher test coverage than fault coverage. To know if our fault grading results would change by considering test coverage instead of fault coverage, we compiled the difference between those two measures in tables 4, 5 and 6. We found the difference between the two measures to be so small that our results would not change.

3.3. Test sets ordering

Table 4: ELF18 Fault Grading Results

Test Sets	Fault Coverage (Test Coverage-Fault Coverage)			Test Length
	Transition Fault	Single-Stuck Fault	Bridging Fault	
15-Detect Transition	**97.4% (0.2%)**	**98.4% (0.2%)**	**88.0%**	**18,726**
TARO	**97.4% (0.2%)**	**98.3% (0.2%)**	**88.0%**	**9,982**
5-Detect Transition	**97.4% (0.2%)**	**98.3% (0.2%)**	**87.8%**	**6,515**
15-Detect SSF	**96.5% (0.2%)**	**98.4% (0.1%)**	**87.0%**	**5,043**
10-Detect SSF	**96.0% (0.2%)**	**98.4% (0.1%)**	**87.0%**	**3,369**
2-Detect Transition	**97.3% (0.2%)**	**98.2% (0.2%)**	**87.7%**	**3,060**
5-Detect SSF	**95.1% (0.2%)**	**98.4% (0.1%)**	**86.8%**	**1,688**
Gate Exhaustive	**93.6% (0.2%)**	**98.4% (0.1%)**	**86.6%**	**1,556**
Transition Fault	**97.1% (0.2%)**	**98.2% (0.2%)**	**87.6%**	**1,453**
3-Detect SSF	**93.5% (0.2%)**	**98.4% (0.1%)**	**86.6%**	**1,068**
2-Detect SSF	**92.0% (0.2%)**	**98.4% (0.1%)**	**86.4%**	**674**
100% SSF	**89.8% (0.2%)**	**98.4% (0.1%)**	**86.0%**	**437**
99% SSF	**86.5% (0.1%)**	**97.5% (0.1%)**	**85.6%**	**226**
95% SSF	**78.8% (0.1%)**	**93.6% (0.1%)**	**83.8%**	**107**
90% SSF	**70.2% (0.1%)**	**88.8% (0.2%)**	**81.1%**	**61**
80% SSF	**57.4% (0.2%)**	**79.2% (0.1%)**	**74.5%**	**25**
50% SSF	**29.7% (0.0%)**	**52.7% (0.0%)**	**45.7%**	**5**

Test ordering is a fundamental issue in the design of test generation and test application flows. The order of test set generation and application varies widely in industry. Some engineers generate single-stuck fault patterns before generating transition fault patterns and apply those test sets in the same order. Others apply a small percentage of all the stuck-at patterns to detect as many defective chips as possible during wafer sort, and then apply the full test set during package test at several voltage and temperature corners.

Previous researchers [Butler 00] have studied the optimal test ordering of stuck-at and transition test sets along with functional and I_{DDQ} test sets and they concluded that the functional test set should be placed early in the test flow to minimize the overall test time. Our experiment is different because our test chips do not have functional patterns.

Other researchers have studied how to use fault simulation to reduce test length. When ATPG tools generate a test set, they do not target all the faults at once. Instead, they select a subset of the faults, generate a few patterns targeting them, and then do fault simulation to eliminate the untargeted faults that were detected by the last patterns generated [Eichelberger 91]. Faults can be similarly eliminated when generating BIST patterns by doing fault simulation at every reseeding [Al-Yamani 05]. In [Crouch 00] the authors go a step further by first generating a path delay test set and then generating a transition test set

Table 5: ELF35 Fault Grading Results

Test Sets	Fault Coverage (Test Coverage-Fault Coverage)				Test Length
	TARO	Transition Fault	Single-Stuck Fault	Bridging Fault	
15-Detect	**79.0%**	**99.2% (0.0%)**	**99.3% (0.1%)**	**86.7%**	**43,035**
TARO	**90.1%**	**98.7% (0.0%)**	**99.3% (0.1%)**	**86.8%**	**29,208**
5-Detect	**76.6%**	**98.7% (0.0%)**	**99.3% (0.0%)**	**86.6%**	**14,727**
Bridging Fault	**72.7%**	**95.3% (0.0%)**	**98.2% (0.1%)**	**86.8%**	**7,105**
2-Detect	**72.8%**	**96.8% (0.0%)**	**99.3% (0.0%)**	**86.2%**	**6,099**
Transition Fault	**75.0%**	**98.9% (0.1%)**	**99.2% (0.0%)**	**86.1%**	**5,888**
Gate Exhaustive	**77.8%**	**95.0% (0.1%)**	**99.3% (0.0%)**	**86.8%**	**4,027**
100% SSF	**67.1%**	**92.9% (0.0%)**	**99.3% (0.0%)**	**85.6%**	**3,165**
99% SSF	**64.4%**	**90.4% (0.1%)**	**97.8% (0.0%)**	**84.5%**	**2,840**
95% SSF	**58.8%**	**85.4% (0.1%)**	**95.1% (0.0%)**	**83.6%**	**2,065**
Toggle	**26.3%**	**51.9% (0.0%)**	**69.8% (0.0%)**	**62.7%**	**323**

Table 6: Murphy Fault Grading Results

Test Sets	Fault Coverage (Test Coverage-Fault Coverage)						Test Length
	TARO	Transition Fault		Single-Stuck Fault		Bridging Fault	
15-Detect	**89.2%**	**99.6%**	**(0.3%)**	**99.7%**	**(0.1%)**	**85.5%**	**7,186**
5-Detect	**83.2%**	**98.8%**	**(0.3%)**	**99.7%**	**(0.1%)**	**85.4%**	**2,403**
Transition Fault	**77.9%**	**99.7%**	**(0.3%)**	**99.7%**	**(0.1%)**	**83.7%**	**1,426**
Bridging Fault	**69.4%**	**91.4%**	**(0.3%)**	**97.7%**	**(0.2%)**	**85.4%**	**1,062**
100% SSF	**65.4%**	**88.9%**	**(0.3%)**	**99.7%**	**(0.1%)**	**84.6%**	**547**
99% SSF	**59.1%**	**85.4%**	**(0.3%)**	**98.8%**	**(0.1%)**	**81.5%**	**443**
95% SSF	**53.2%**	**79.6%**	**(0.3%)**	**94.8%**	**(0.1%)**	**79.1%**	**351**
Toggle	**26.3%**	**54.9%**	**(0.1%)**	**74.0%**	**(0.1%)**	**59.5%**	**130**

targeting only the transition faults not detected by the path delay test set, and finally generating a single-stuck fault test set targeting only the single-stuck faults not detected by the previous two test sets.

Our results lead us to the following test set ordering conclusions:

Tables 1, 2 and 3 show that those of the test sets we applied that had the maximum achievable single-stuck fault coverage detected all the TICs, except for the Murphy transition test set, who missed a TIC despite detecting the same single-stuck faults as the single-stuck fault test set. We therefore concluded that the single-stuck fault metric was effective at detecting all the TICs.

Furthermore, tables 1, 2 and 3 show that the single-stuck fault, N-Detect and gate exhaustive test sets escapes are

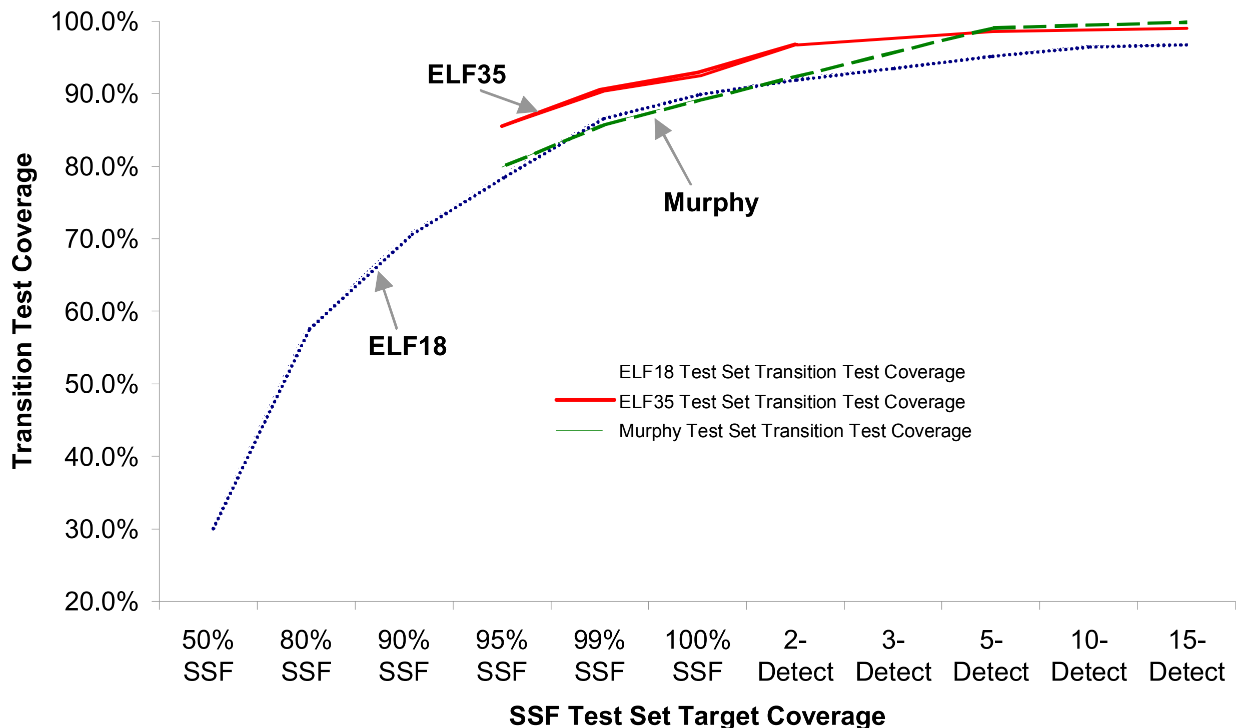

Figure 7: Transition Test Coverage of SSF and N-Detect Test Sets

all sequence dependent. Those tables also show that the transition test set is more effective than the single-stuck fault test set at detecting sequence dependent chips, particularly for ELF18 in Table 1 because the transition test set is applied at a faster timing than the single-stuck fault test set (70 MHz instead of 30 MHz) and therefore detects more sequence and timing dependent cores.

Our results therefore suggest that test engineers should first generate a transition fault test set and then generate additional patterns by targeting only the single-stuck faults undetected by the transition fault test set, like [Crouch 00].

In addition, our results show that the proportion of sequence dependent is increasing and that the transition fault test sets are better suited at detecting them so this suggests that they should be applied before the additional stuck-at patterns so as to detect more defective chips earlier in the test flow.

4. Conclusion

The effectiveness of test metrics varies according to the defective class of the chip being tested. We found that single-stuck fault test sets detected all the TICs and that defective cores escaping thorough test sets like N-Detect or gate exhaustive are sequence dependent. Test engineers should take this into account when selecting test sets to apply because the choice of the second test set of a pair used for testing cannot be optimized without taking into account the nature of the first test set of the pair.

5. Acknowledgements

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Appendix: Characteristics of the Test Chips and their Tests

Characteristics		***Chip***		
		ELF18	**ELF35**	**Murphy**
Chips Tested		2,800	9,000	5,500
Technology Name		Corelib	G10P	LFT150K
Technology Type		CMOS	CMOS standard cell	CMOS gate array
Effective Channel Length		0.18µm	0.35µm	0.7µm
Number of Metal Layers		6	3	2
Number of Gates		320,000	265,000	25,000
Die Size		31 mm^2	103 mm^2	
Pins	I/O	39	208	96
	Supply	39	64	24
	Outputs Tristateable?	No	No	No
IDDQ Threshold		100µA	300µA	100µA
Tests before ATPG		Contact, Input Leakage	Power Supply Short, Continuity, VIH, VIL, Input Leakage	Gross IDDQ (<500µA), input thresholds, VOL/VOH, IOS, input leakage, tristate leakage
Nominal Voltage Tests	Supply Voltage	1.8 V	3.5 V	5 V
	VIL	0 V		0 V
	VIH	1.8 V		4.5 V
	VOL	0.81 V		1.5 V
	VOH	0.99 V		1.5 V
VLV Tests	Supply Voltage	0.65 V	1.4 V	1.7 V
	VIL	0 V		0 V
	VIH	0.65 V		1.7 V
	VOL	0.29 V		0.85 V
	VOH	0.36 V		0.85 V