AN EXPERIMENTAL CHIP TO EVALUATE TEST TECHNIQUES CHIP AND EXPERIMENT DESIGN

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Abstract

An experiment has been designed to evaluate multiple testing techniques for combinational circuits. To perform the experiment, a 25k gate CMOS Test Chip has been designed, manufactured (5491 devices), and evaluated with over 300 tests. The chip contains five types of CUTs derived from functions in production ASICs.

1. Introduction

Many test techniques have been proposed to achieve the quality levels now required for digital integrated circuits. In order to make optimum test choices, the various testing approaches can be compared with respect to several criteria. These include the impact on performance and area of the circuit, required design time, test vector size, test time, automated test equipment (ATE) requirements, and finally, thoroughness of the test in detecting faulty circuits. Of these factors, test thoroughness, usually specified as escape rate or defect level, is most difficult to quantify. The reason is that, while the other factors can be accurately calculated, escape rate predictions must be verified empirically.

This experiment is a collaboration among several organizations with the common interest to gather more information on test techniques and their associated escape rates. The partners include an ASIC manufacturer (LSI Logic), an ASIC user (Hughes Aircraft Co.), a test service (Digital Testing Services), and the Center for Reliable Computing (CRC) at Stanford University.

The experiment is designed to achieve the following objectives:

1. Evaluate a very large number of candidate test techniques.
2. Evaluate test techniques under constant conditions: on the same circuits and under identical test conditions.
3. Evaluate test techniques on logic circuits which are representative of real world design.
4. Include a set of exhaustive tests to provide an absolute reference.
5. Employ a dedicated gate array chip (25K used gates) which can easily be built on a variety of CMOS processes.
6. Evaluate the detection capability for real production failures, not artificially induced failures.

Similar experiments reported in the literature are summarized in Table 1-1. These experiments are either based on commercial products or specially designed chips. The advantage of production runs is that a large sample size is available, but the number of test techniques compared is usually small. Fairly small sample sizes have been reported for specially designed chips. The main distinguishing feature of the experiment described here is that a much more thorough comparison of test techniques than has previously been reported is attempted, with a reasonable sample size. 5491 devices have been evaluated (having been provided by LSI Logic as LFT150K series [8] CMOS gate arrays with L_{eff}=0.7μ).

This paper describes the experiment and the test vehicle IC (Test Chip). The companion paper [9] describes the tests which have been evaluated and the initial results.

2. Test Chip Architecture

Fundamental to our approach has been the design and manufacture of a dedicated test IC containing a number of combinational circuits-under-test (CUTs), which are representative of real world designs, and on which a wide range of different test methodologies may be evaluated. There are provisions to perform exhaustive tests on each CUT, as an absolute reference.

A number of practical considerations also enter into the design, to minimize both device and testing costs. Considerable support circuitry is provided to enable all evaluations to be performed by wafer probing, eliminating packaging. Support circuitry also minimizes the burden on Automated Test Equipment (ATE) by providing clocking and response strobing on-chip (even with low speed ATE and fixturing) and by performing all response evaluations (except I_{DDQ}) on-chip.

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Table 1-1. Recent Test Experiments Reported

Experiment	CUT	CUT Size	Sample Size	Tests Applied
Velazco, Grenoble [20]	6800, 68000 µP		75 IC's	Design Verification Vectors
Elo, Intel [3]	Gate Array	12.5K Gates	350,000 IC's	9 Modules of Boolean Tests
Das, Delco / U. Nebraska [2]		7,750 transistors	77,912 IC's	Stuck-At
Pancholy, Cypress / McGill U [12][13]	Special IC	9 Blocks	970 faulty blocks	Stuck-At, Open, Transition, Robust
Maxwell, HP [10]	Std. cell	8500 gates	18,500 IC's	Design Verification, Scan
Maxwell, HP [11]	Std. Cell	8577 gates	26,415 IC's	[Maxwell 91] + I_{DDQ}
Sawada, Mitsubishi [16],	Sea of Gates	3,000 gates 114K gates	48 IC's 400 IC's	Single I_{DDQ} vs. multiple I_{DDQ}
Perry, Storage Tech [14]	Various	2.5-5.6K gates	3 years of I_{DDQ}	Stuck-At, I_{DDQ}
Schiessler, AT&T [17]	Std. Cell	10K gates	1,400 IC's	Functional, scan, I_{DDQ}
Gayle, NCR [5]	Various	Various	> 10^6 IC's	Stuck-At, I_{DDQ}, At-Speed
Wiscombe, VLSI Tech. [21]	Gate Array	8K gates	10,000 dice	Stuck-At, I_{DDQ}
This Experiment	Gate Array	25K Gates 12K CUTs	5491 dice	Many techniques + exhaustive tests

Finally, a mechanism is provided by which experiments can be performed without revealing—or needing to know—the absolute yield attained at the source foundry. The protection of proprietary yield information simplifies the acquisition of devices for experiments and, along with the fact that the design is a gate array, makes multiple foundry sourcing a possibility.

Table 2-1 provides a summary of the test chip features, which are described in the remainder of this section.

Table 2-1 Test Chip Summary

CUT Selection	• Combinational - represent real control and data-path logic • Include logic synthesis and manual design • Multiple implementations of one function - Varying gate complexity - Robust delay-fault testable version
Multiple Test Pattern Sources	• External: any deterministic test vector set • Direct parallel • Simulated serial scan • Internally Generated Pseudo-random and exhaustive, including 2^N and 2^{2N} exhaustive test
Test Clocking	• Externally applied clocking • Internally generated clocking • Requires only low frequency ATE and fixturing
Response Analysis	• Boolean (voltage sampling), including serial and parallel signature analysis • I_{DDQ} (current sampling) • CrossCheck observation network [6] • Stability Checking [4]

The test chip is designed to be built as a standard CMOS gate array with 25K gates used. The technology selected for implementation is LSI Logic's LFT150K master slice, which has the CrossCheck test method as an embedded feature [8]. The design can be transported to other CMOS gate array families, (in which case the CrossCheck evaluations might not be included).

The chip includes 5 types of circuits-under-test (CUT) as well as test support circuitry, as shown in Fig. 2-1. Test support circuitry refers to both the on-chip data source logic for applying patterns to the CUTs, and the response analysis circuitry, as well as special clock and timing generation circuits. The CUTs are limited to 24 input bits in order to enable exhaustive tests to be executed in a reasonable length of time. There are four copies of each of

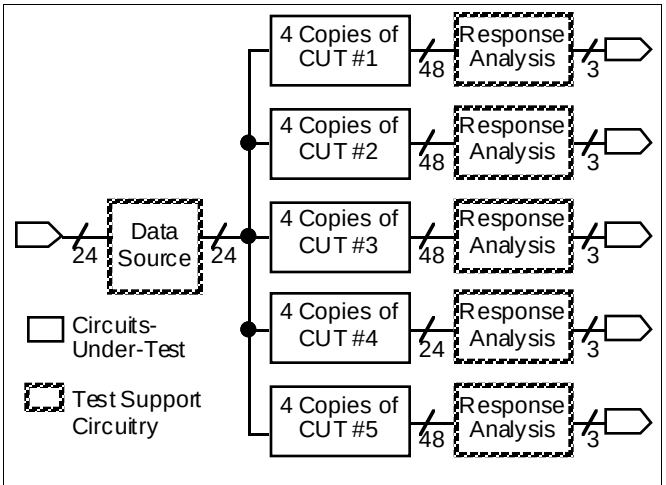

Figure 2-1 Basic Data-Flow Diagram of Test Chip

the 5 different combinational CUTs on the chip.

A common data source is used for all CUTs. Tests can be applied either by the built-in self-test (BIST) circuitry (for pseudo-random and exhaustive tests) or by an external tester (ATE). In either case, at-speed, shifted vector pairs, and timed two-pattern tests can be applied to the CUTs. Clocks may be applied directly by ATE or derived from slower ATE clocks. The derived clocks have periods which are set either from the applied clock pulse width, or from an internal delay line which tracks process and operating conditions. The internal delay line may be monitored as a ring oscillator to measure intrinsic chip speed.

The response analysis circuitry enables the use of long pseudo-random tests and the exhaustive tests (since the responses would otherwise overwhelm the ATE storage capability). The response analysis circuits are used for tests whose source is ATE as well. This relieves output pin requirements as well as ATE response storage.

The response analysis consists of a real time comparison of the outputs of the four identical copies of each CUT. Thus, failure of any CUT copy constitutes a detected fault within that CUT set. Each response analyzer records 1) the address of the first detected failure in a pattern set and 2) the total number of failure events occurring during a complete pattern set.

3. Testing Strategy

The two stage testing strategy shown in Fig. 3-1 resulted from the following considerations. A premise of this experiment is to make as much data publicly available as possible, without disclosing sensitive process information. Furthermore, the main interest is in failures that are difficult to detect. (Gross failures are generally easy to test; the ability of tests to detect the difficult failures is more important for achieving high quality levels.)

Stage 1:

The first test is a gross DC parametric test, consisting of gross I_{DD} (<500μA), input thresholds, VOL/VOH, IOS, input leakage, and tristate leakage. The CrossCheck test circuitry and the test support circuitry on the die are then tested. Only the data from the dice that pass all these tests were available for this experiment. The disadvantage is that the gross wafer yield is not known, but there is no constraint on reporting any data after this point.

Stage 2:`

The second stage is the testing of the actual CUTs on die that pass the Stage 1 tests. The sample size, N (in this case 5491), of die that will be tested thoroughly is the number of devices which pass stage 1.

Note that this strategy requires the test support circuitry to be well tested, to minimize erroneous responses in the subsequent CUT test experiments. Stuck-at tests of support circuitry achieve 98.8% coverage, based on fault grading by Zycad XPLUS. The support circuitry is also subjected to an I_{DDQ} test with 250 strobe points. (There has been no evidence of support circuitry failure on any actual testing done so far.)

Also, since this is a standard gate array, it is impossible to modify the base array to strictly isolate the test support circuits and the CUTs during I_{DDQ} tests and CrossCheck testing. In order to minimize ambiguity, the CUTs are held in fixed states while the support circuitry is screened with I_{DDQ} and CrossCheck tests.

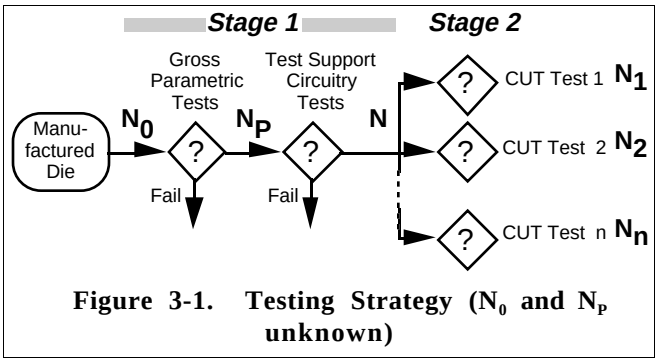

Figure 3-1. Testing Strategy (N_0 and N_P unknown)

4. Test Chip Implementation

The Test IC consists of seven principal parts, as shown in the block diagram, Fig. 4-1:

Circuits Under Test (CUTs)
Data Source
Response Evaluation Circuits
Failure Counters
Signature Register
Timing Generation
CrossCheck Observation Circuitry

These are described in the following sections.

4.1 Circuits Under Test

The circuits-under-test (CUTs) are described in this section. The CUTs are representative of data-path and control logic, as well as various design styles. The requirements for the CUTs were:

- Combinational logic
- 24 or fewer inputs. The number of inputs was limited in order to permit exhaustive testing.
- Few outputs, to reduce the response analysis circuitry, as well as increase the test difficulty by reducing fault detectabilities. The CUTs have either 6 or 12 outputs.

There are five CUT types: two multipliers and three control logic blocks, shown in Table 4-1. The three control logic blocks perform the same function, but were designed differently. The first implementation was synthesized using all available gates in the LFT150K library [8], the second was restricted to elementary gates

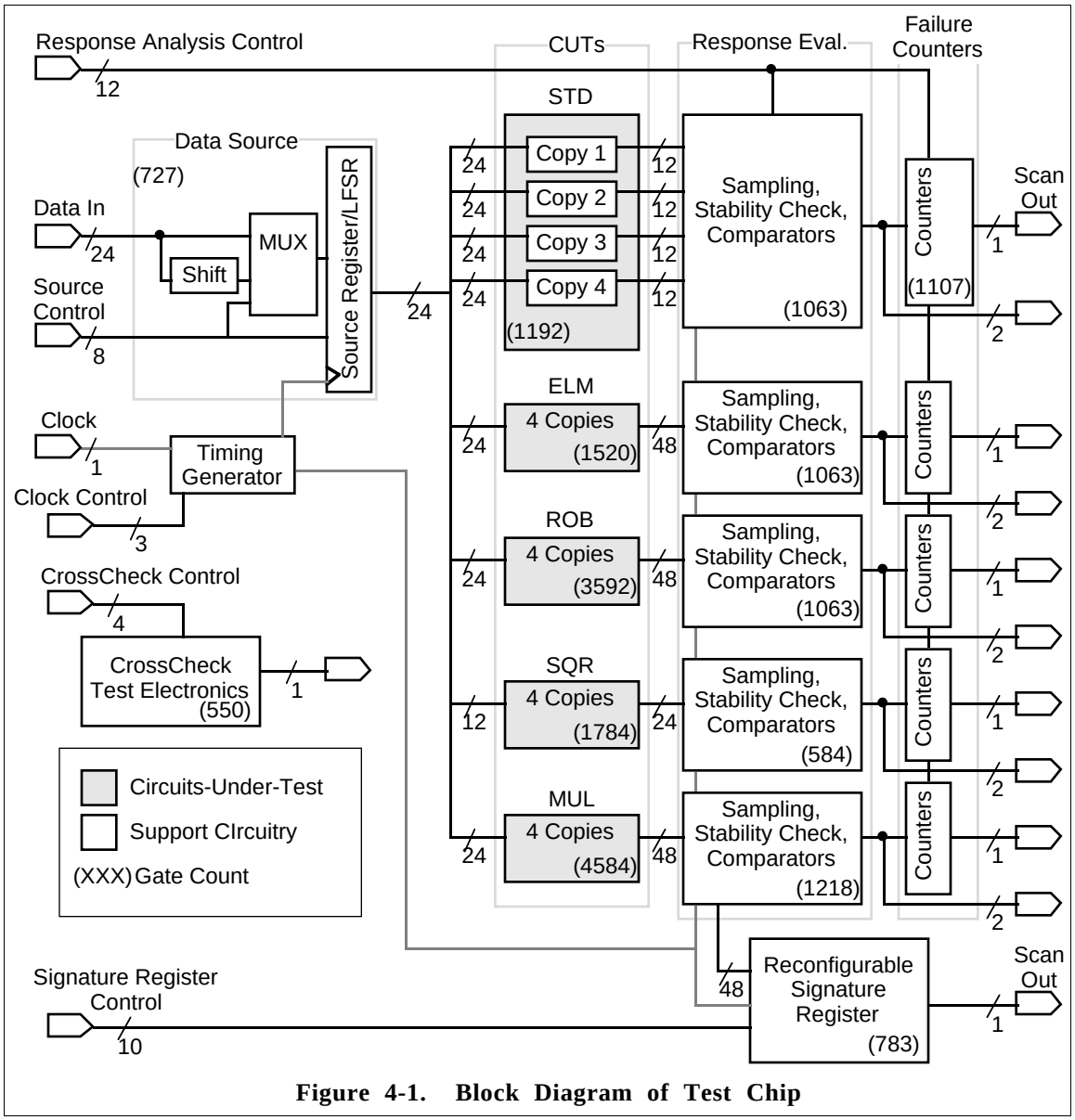

Figure 4-1. Block Diagram of Test Chip

(NOT, AND, OR, NAND, NOR), and the third is robust path-delay-fault testable.

4.1.1 Control Logic Blocks (STD, ELM, ROB)

The control logic blocks are various implementations of the same function, part of a control circuit from a DMA controller. The original circuit had 34 inputs and approximately 3,700 literals. Ten of the inputs were tied to 0 (to meet the 24 input CUT constraint) before synthesizing the three implementations.

One of the purposes of this part of the experiment was to investigate the effectiveness of multiple
test techniques on three different circuit implementations of an identical function. Fig. 4-2

Table 4-1. CUT Types

Name	Inputs	Outputs	LSI Gates	Description	Design Method
STD	24	12	298	control logic - any gates	Synthesis
ELM	24	12	380	control logic - elementary gates	Synthesis
ROB	24	12	898	control logic - robust path-delay fault testable	Synthesis
SQR	12	6	446	6x6 multiplier followed by a squarer	Manual
MUL	24	12	1,146	12x12 multiplier	Manual

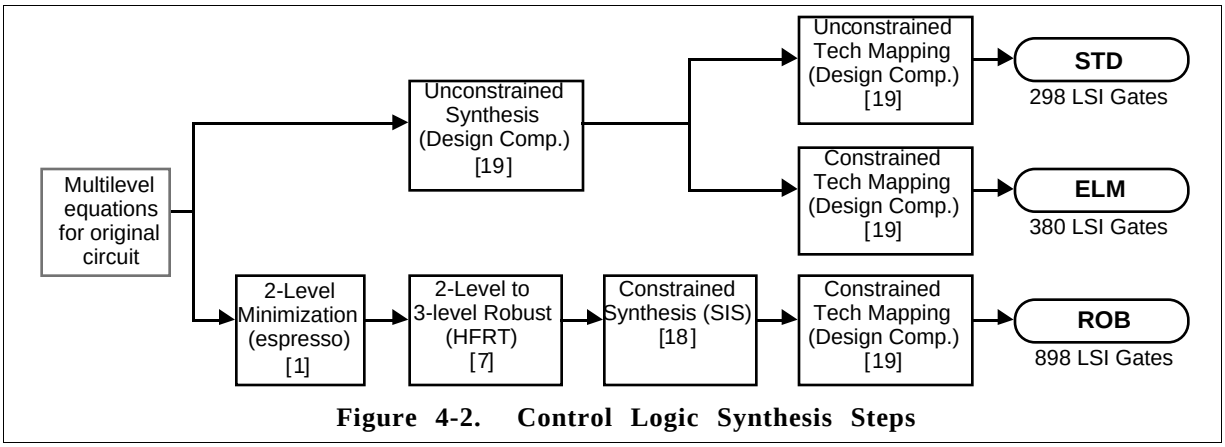

Figure 4-2. Control Logic Synthesis Steps

summarizes the steps taken to produce the final netlists.

The first implementation is STD, the "standard" implementation. It uses the unrestricted LFT150K library [8], including complex gates (such as XOR and AND-OR-INVERT). It was synthesized using Synopsys' Design Compiler [19], starting from the original multilevel netlist with 10 inputs tied to 0, with Boolean optimization turned on.

The second implementation is ELM, which uses only elementary gates. It was synthesized in the same way as STD, except that the target library was restricted to elementary gates (AND, OR, NOT, NAND, NOR) for technology mapping.

The third implementation is ROB, which was synthesized to be robust path-delay-fault testable. The original netlist was collapsed to 2 levels and simplified using espresso [1], since the synthesis tool used for achieving robust delay fault testability required a flattened netlist. A 3-level robust path-delay-fault testable circuit was then generated using the procedure described in [7]. The Sequential Interactive Synthesis Program (SIS, [18]) was then used with constrained algebraic optimizations that preserve robustness to get a multi-level circuit. The technology mapping was done using Synopsys, using both simple gates and complex gates with no internal reconvergence.

The final ROB circuit was generated first, optimizing delay, then STD and ELM were synthesized with the same target delays. The sizes of the three implementations are given in Table 4-2 in terms of LSI gate equivalents. For example, a 2-input NAND has a gate count of 1, and a 4-input NAND has a gate count of 3 [8]. The number of paths without single-path-propagating hazard-free robust tests (SPP-HFRT) [15] are also shown in the table. The nominal delays shown are post-layout, predicted by LSI Logic MDE toolset.

Table 4-2. Control Logic CUT Implementations

Circuit	Nominal Delay	LSI Gates	Physical Paths	Paths w/o SPP-HFRT
STD	12.1 nS	298	841	125
ELM	16.0 nS	380	841	125
ROB	14.7 nS	898	1773	6

4.1.2 12x12 Multiplier (MUL)

This is a 12x12 partial product multiplier composed of 6x6 multiplier building blocks, as shown in Fig. 4-3 Only the twelve most significant bits of the output are implemented. Using the most significant bits reduces the response evaluation circuitry, as well as decreasing the observability of some faults in the multiplier. This CUT has a nominal post-layout delay of 33.8 nS.

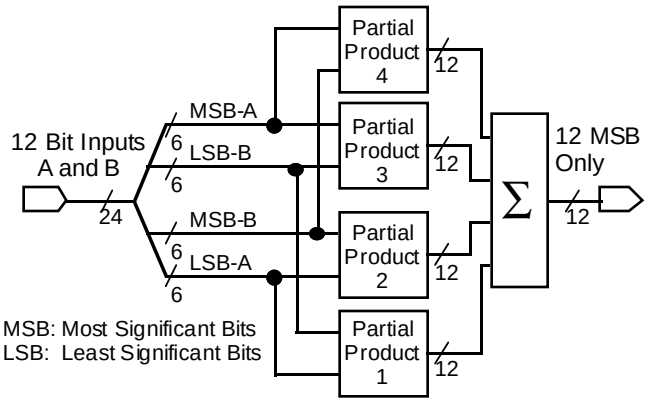

Figure 4-3. Partial Product 12x12 Multiplier

4.1.3 6x6 Multiplier Followed by Squarer (SQR)

This CUT consists of two 6x6 multipliers similar to those used on the 12x12 multiplier. The multipliers are cascaded, and the second multiplier acts as a squarer since both inputs are fed by the output of the first multiplier. Some redundancies were eliminated by hand in the final circuit, and only the 6 most significant bits of the output

are implemented. This CUT also has a nominal post-layout delay of 35.4 nS.

The main reason for including this circuit is to have at least one CUT with few enough inputs to permit 2^{2N} exhaustive testing, where all possible transitions are applied. The 2^{2N} exhaustive test provides a thorough reference for delay faults.

4.2 Data Source Features

4.2.1 Operating Modes

Data is applied to the CUTs using an on-chip parallel output linear feedback shift register (LFSR). There are three ways to apply data to the CUTs:

4.2.1.1 Parallel Load

In this mode, data at the parallel data inputs is clocked into the source register from ATE at the rising edge of the main clock. Both single and two-pattern delay tests are applied in this mode. For two-pattern tests, CUT outputs are observed on even input vectors, and masked on odd input vectors.

4.2.1.2 Simulated Scan

ATE test vectors can be applied in a "simulated scan" sequence in two clock cycles. At the first clock, the input vector rotated by one bit position is applied to the CUTs. At the second clock, the original input vector is applied. This mode is mainly for convenience in applying patterns generated for scan; an identical sequence is possible in Direct mode by modifying the patterns to supply the two-pattern tests from the ATE.

4.2.1.3 Pseudo-random

In this mode, the data source register is configured as an LFSR (linear feedback shift register) to provide an exhaustive test in 2^{24} clocks. The LFSR implements the primitive polynomial

$$f(x) = x^{23} + x^6 + x + 1$$

The all-zeros state must be supplied in the direct load mode. The LFSR must be initialized with a non-zero seed, by operating in direct load mode (mode 0) with the seed applied at the parallel data inputs, DIN(23:0).

The pseudo-random mode also supplies an 2^{2N} exhaustive test to the fifth CUT, the 12-input multiplier-squarer, in 2^{24} clocks.

4.2.2 CUT Isolation

Control inputs are provided to disable the data to each CUT type. When the corresponding control signal is asserted, the CUT inputs are forced to logic zero.

4.3 Response Evaluation Circuits

The response evaluation circuits, EVAL1 through EVAL5, evaluate the responses from each CUT type. As shown in Fig. 4-4, each EVALn circuit consists of a data register, compare logic, and post sample stability checkers [4].

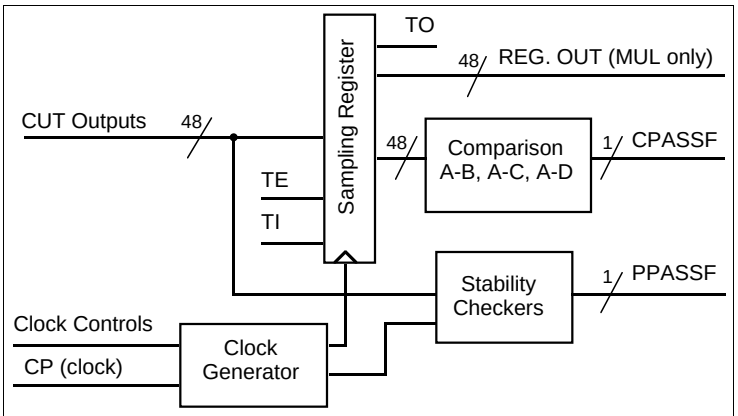

Figure 4-4. Response Evaluation Circuit

Using the data clocked into the register, the outputs of the second, third and fourth CUT copies are compared to the outputs of the first copy. The result appears at the CPASSF output.

The stability checkers observe each output for changes after the sample clock. If any output changes after the sample clock, the PPASSF output of the EVALn is asserted. The occurrence of a stability failure in the absence of a corresponding Boolean failure may indicate a fault being masked by a hazard.

The clock generator modes are described in section 4.6, "Timing".

4.4 Failure Counters

The counters record the first clock cycle in which a failure occurred and the total number of failures occurring during the test. There are five counters:

#	Function	Bits
1	First Clocked Failure	24
2	Total Clocked Failures	16
3	First Stability Failure	24
4	Total Stability Failures	16
5	Total Stability-only Failures	16

The counters for each CUT type are concatenated in a scan string, as shown in Fig. 4-5.

There are a total of 100 flip-flops in the chain, ordered LSB to MSB. To initialize the counters, the test pattern shifts zeros into the entire chain.

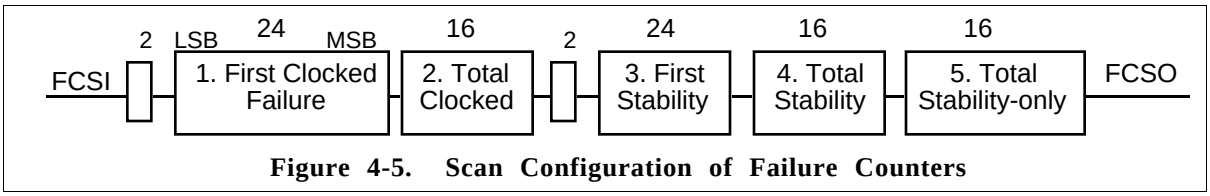

Figure 4-5. Scan Configuration of Failure Counters

The failure counters have a masking control signal (not shown) which causes the counters to ignore failures. This is used when failures are to be recorded only on certain cycles, as in delay testing or simulated scan.

In normal use, the tester reads and records the values of the counters at the end of the test.

4.5 Signature Register

Due to hardware constraints (available gate area) signature analsysis is applied to only one CUT, the 12 x 12 multiplier (MUL). The outputs of the MUL are fed to a configurable signature register, shown in Fig. 4-6.

The register is segmented to support signature compression in four configurations (parallel mode):

48 bit MISR x 1
24 bit MISR x 2
16 bit MISR x 3
12 bit MISR x 4

In serial mode, one of the 48 MUL outputs is selected as the serial input, and only the first (leftmost) portion of the signature register is used. The four signature sizes are also available in this mode.

For test and initialization, the register operates in a simple scan mode.

The scan output is brought to the chip I/O, and can be monitored to aid diagnosis of CUT failures.

4.6 Timing

The data sources and failure counters are clocked by the rising edge of the Source Clock (see Fig. 4-7 and Fig. 4-8). The output sample registers are clocked by the Sample Clock, generated by one of three methods: direct clocking based on tester cycle period, externally generated clocking, and internally generated clocking.

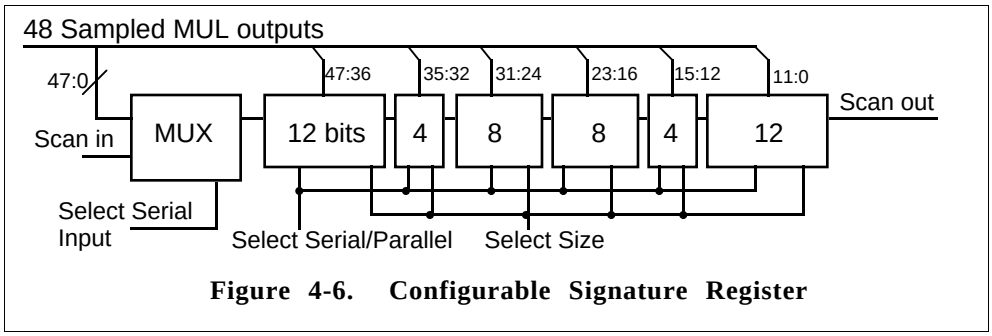

Figure 4-6. Configurable Signature Register

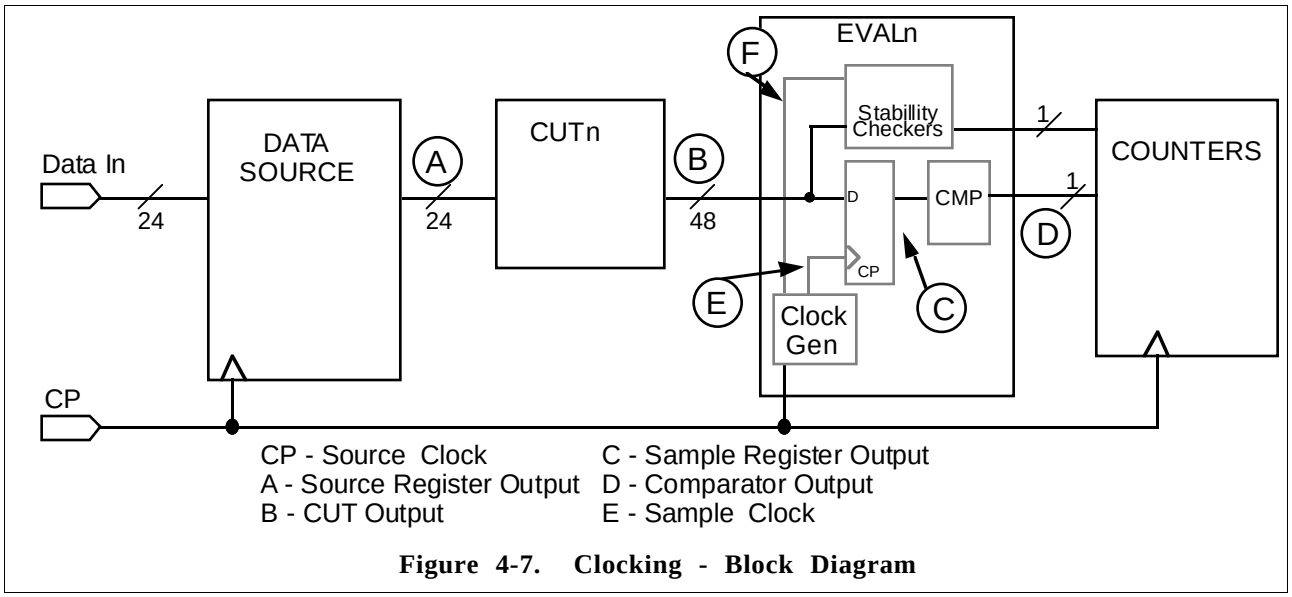

Figure 4-7. Clocking - Block Diagram

4.6.1 Direct Clocking from ATE

This is the simplest clocking mode, corresponding to single clock synchronous designs. A new pattern is applied on each rising edge of the master clock, and the outputs are sampled at the subsequent rising edge. The master clock from the ATE is used as both the Source Clock and the Sample Clock. Stability error detection is disabled in this clocking mode.

4.6.2 Pulse Width Generated Clocking

In the pulse width generated clocking mode, the time from CUT input pattern application to CUT output sampling is precisely controlled, independent of the tester clock period. This allows the tester and fixture to operate at a low data rate, provided it can deliver an accurate clock pulse width. As seen in Fig. 4-9, the output clock is generated from the falling transition of the master clock.

4.6.3 Internally Generated Clocking

In the internally generated clocking mode, the time from CUT input pattern application to CUT output sampling is determined by delay elements in the clock generators in each EVALn partition. This places minimal requirements on the tester and fixture, since the delay test is independent of pulse width as well as clock period. Also, the test is equally stringent for all dice, since process variations are taken into account automatically. Fig. 4-10 shows the timing relationships in this mode.

4.7 CrossCheck

The test chip includes the CrossCheck testability solution, which allows unobstructed observation of every node in the design [Gheewala 89].

Probe lines are embedded in the masterslice, and sense lines are routed in reserved first layer metal channels. A sense transistor is embedded at each probe/sense line intersection.

The macrocells are functional equivalents to the LSI Logic LCA100K library, restructured to allow connection of an

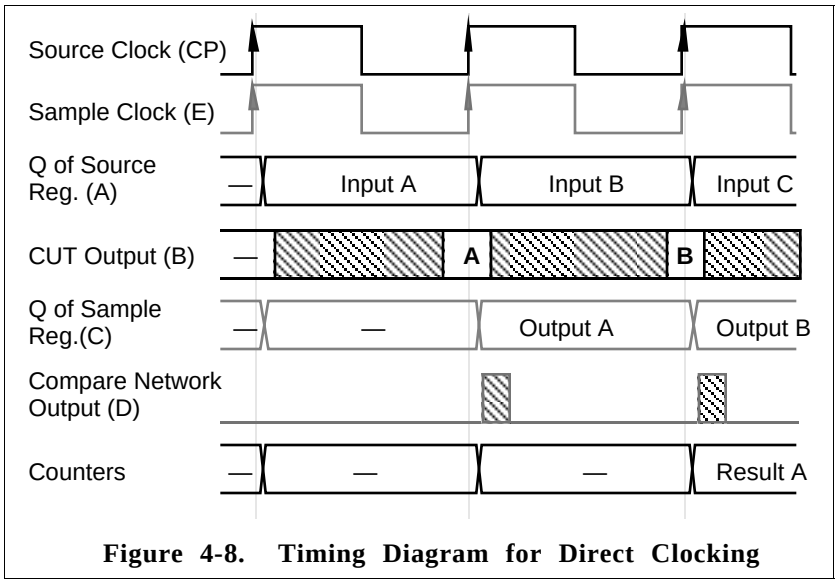

Figure 4-8. Timing Diagram for Direct Clocking

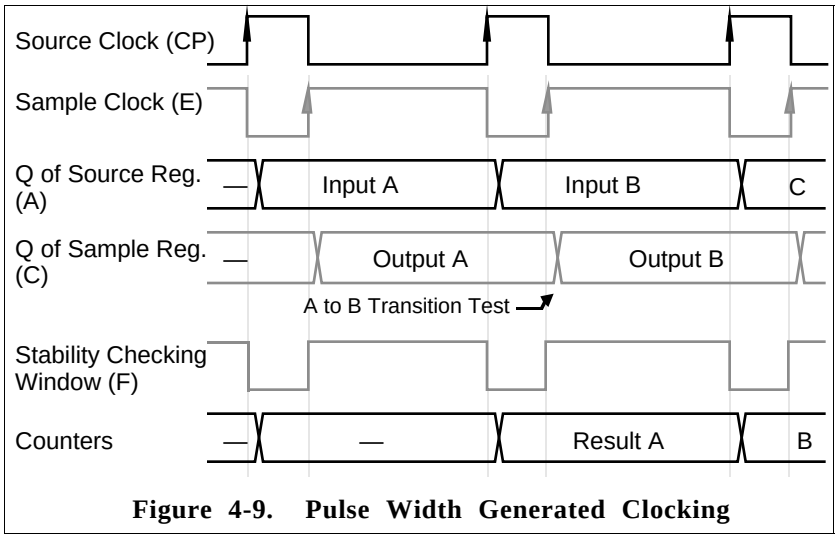

Figure 4-9. Pulse Width Generated Clocking

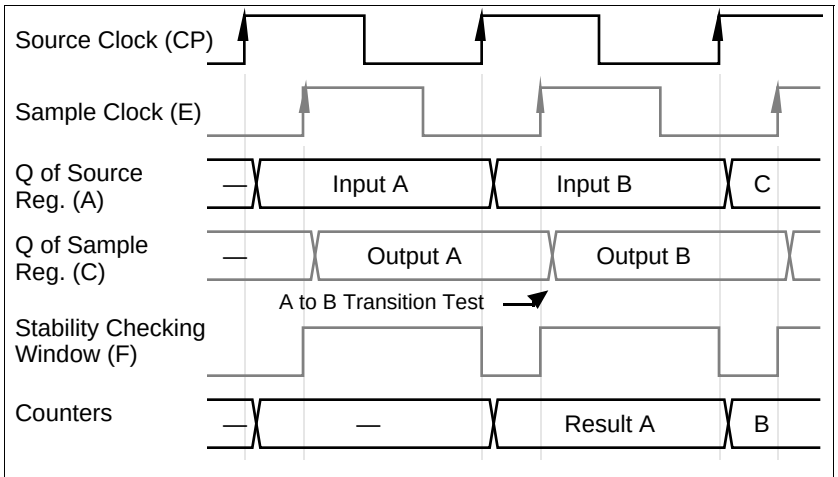

Figure 4-10. Timing Diagram, Internally Generated Clocking

embedded sense transistor to the output of each gate.

To test the chip, vectors are applied to achieve high toggle coverage in the logic. At each vector, the CrossCheck Test Electronics activates the probe lines in sequence, accumulating a signature of the data received on the sense lines. The signature is shifted out and compared with an expected signature derived from simulation.

5. Implementation

5.1 Netlists

The full chip netlist is available in hierarchical LSI Logic NDL and EDIF formats. The CUT netlists are also available separately in NDL and EDIF formats. The netlists may be obtained by contacting CRC.

5.2 Hardware Details

The Test Chip was implemented in LSI Logic LFT150K technology [8]:

- 1.0 micron drawn gate length (0.7 micron effective channel length)
- Two level metallization
- Embedded CrossCheck observation network.
- Macrocells functionally equivalent to LSI Logic LCA100K series

6. Summary

The experiment and chip design have met the requirements of the project:

1. Large number of test techniques: The chip supports externally applied patterns as well as internally generated exhaustive patterns, each of which can be applied in multiple clock modes. For result evaluation, it supports sampled output comparison, stability checking, signature compression, CrossCheck observation, and IDDQ testing. On-chip counters track quantity and first occurrence for sampled and stability failures.
2. Constant conditions: The experiment is designed so that all test techniques are applied and evaluated during a single pass wafer probe test (with common device, voltage, temperature, and timing.).
3. Real world design: Though practical considerations (mainly chip size) precluded the use of typical modern partitions, the DMA control logic circuit is a subset of a design currently in use, and the multipliers represent common arithmetic logic. The chip is built in 1 micron technology representative of commercial practice.
4. Exhaustive reference tests: The on-chip LFSR exercises every input state of the CUTs, as well as every two-state transition of the 6-bit multiplier.
5. The test chip is a gate array, adaptable to a variety of CMOS processes: The test chip uses standard macrocells, and the database is available in NDL or EDIF format.
6. Real production failures: All the failures arising in this experiment occured naturally in the manufacturing process; none were artifically induced. Future work may also investigate stress-induced failures.

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