ANALYSIS AND DETECTION OF TIMING FAILURES IN AN EXPERIMENTAL TEST CHIP

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ABSTRACT

A 25k gate Test Chip was designed and manufactured to evaluate different test methods for scan-designed circuits. The design of the chip, the experiment, and preliminary experimental results were presented at ITC'95. This paper presents results for different clock speeds and clocking modes (at-speed and delay), and uses this data to characterize the behavior of the defective parts. It was found that timing-related defects are common, and the escape rate for different test techniques on these parts is discussed.

1 INTRODUCTION

A Test Chip has been designed and manufactured to evaluate multiple test techniques for combinational or full-scan circuits. The objective of the experiment was to get a real-world comparison of many different test methods, as it is difficult to evaluate the effectiveness of tests without experimental data.

The design of the experiment and architecture of the Test Chip were described in [1], and preliminary experimental results were presented in [2]. This paper presents results for different clock speeds and clocking modes (at-speed and delay), and uses this data together with the data from the on-chip failure counters to characterize the behavior of the defective parts. Almost 44% of the defective parts were found to be timing or pattern dependent, and most of the test escapes were on parts with these defects. The Stability Checking results show that the Stability Checkers worked as intended, and accurate propagation delay measurements on a few CUTs show that a super-exhaustive test can exercise longer delays through a circuit than other test sets.

Several experiments have been reported in the literature that address the quality impact of the different test sets [3-14]. One of the main distinguishing features of this experiment is that many different test techniques were investigated, whereas previous experiments have generally compared only a few test techniques (e.g. stuck-at vs. delay vs. IDDQ).

The Test Chip architecture was designed in conjunction with Hughes Aircraft Corporation, where most of the detailed design was done. The Test Chips were fabricated at LSI Logic Corporation in four wafer lots, and the wafers were tested on a 100MHz Tester (Schlumberger ITS9000FX) by Digital Testing Services, Inc.

The Test Chip is a 25k gate CMOS gate array, manufactured using LSI Logic's LFT150K FasTest array series, and has 96 I/O pins. The chip area is divided equally between test support (DFT) circuitry, and circuits-under-test (CUTs). The CUTs on 5,491 dice have been tested.

The Test Chip includes 5 CUT types including both control and data-path logic, designed with different design styles, which were tested using design verification, exhaustive, pseudo-random, and deterministic ATPG vectors for various fault models (stuck-at, transition, delay faults, and IDDQ current testing). The CUTs were also tested using the CrossCheck embedded array [15], IDDQ testing, as well as other techniques, including Stability Checking [16] and Very-Low Voltage testing [17]. The experiment included an investigation of both serial and parallel signature analysis.

This paper is organized as follows. Section 2 briefly describes the relevant aspects of the Test Chip, more details can be found in [1,18]. Section 3 covers the test conditions and test sets applied, and the next sections focus on timing-related defects. Section 4 discusses the results for sampling at normal voltage, including a classification of defects. Section 5 discusses Stability Checking results, Sec. 6 discusses signature analysis, and Sec. 7 addresses the validity of the experimental data. Section 8 discusses some precise propagation delay measurements done on a few CUTs, and Sec. 9 concludes the paper.

2 TEST CHIP

2.1 Block Diagram

The Test Chip includes four copies of 5 different combinational circuits-under-test (CUT), as well as test

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Table 1: CUT Types

Name	Inputs	Outputs	LSI Gates per CUT copy	Description	Design Method
STD	24	12	298	Control logic - all gates in library used	Synthesis
ELM	24	12	380	Control logic - only elementary gates used	Synthesis
ROB	24	12	898	Control logic - robust path-delay fault testable	Synthesis
SQR	12	6	446	Datapath - 6x6 multiplier followed by a squarer	Manual
MUL	24	12	1,146	Datapath - 12x12 partial product multiplier	Manual

support circuitry for applying test vectors and observing responses. The overall data flow in the Test Chip is shown in the block diagram in Fig. 1. There is a common data source (parallel load LFSR which implements the primitive polynomial $f(x) = x^{24} + x^7 + x^2 + x + 1$), and a response analysis circuit for each CUT type. There is also a multiple input signature analyzer for the MUL CUT.

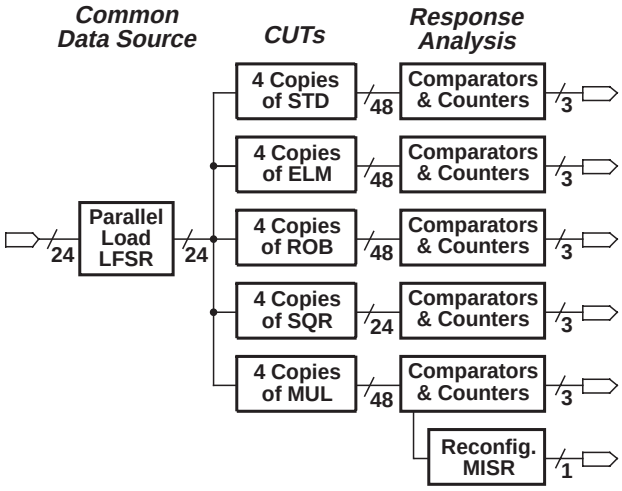

Fig. 1: Basic Data-Flow Block Diagram of Test Chip

2.2 CUTs

Table 1 lists the five types of CUTs that were designed, including two multipliers and three control blocks. The sizes of the CUTs are given in terms of LSI gate equivalents. For example, a 2-input NAND has a gate count of 1, and a 4-input NAND has a gate count of 3.

MUL is a 12x12 partial product multiplier with only the 12 most significant outputs observable. SQR consists of a 6x6 multiplier in which the 6 most significant outputs are fed into another 6x6 multiplier, such that the second multiplier acts as a squarer. The three control logic blocks implement the same function synthesized with different constraints. STD is implemented using the standard LFT150K library [19], ELM uses only elementary gates, and ROB is a robust path-delay-fault testable implementation. CUT details can be found in [1,18].

2.3 Response Analysis Circuits

The response analysis is done on chip to avoid storing prohibitively long test responses on the ATE. The corresponding outputs of four copies of each CUT are compared to determine if any errors have occurred, and counters are used to record the first-failing vector and the number of failing vectors for the test set.

The design of the comparison circuit is shown in Fig. 2. Each CUT output is latched, and has a Stability Checker [16]. The outputs of the comparators are ORed, so that the error is observed if any output is in error. Comparators are not necessary for Stability Checking, since the fault-free response is not required.

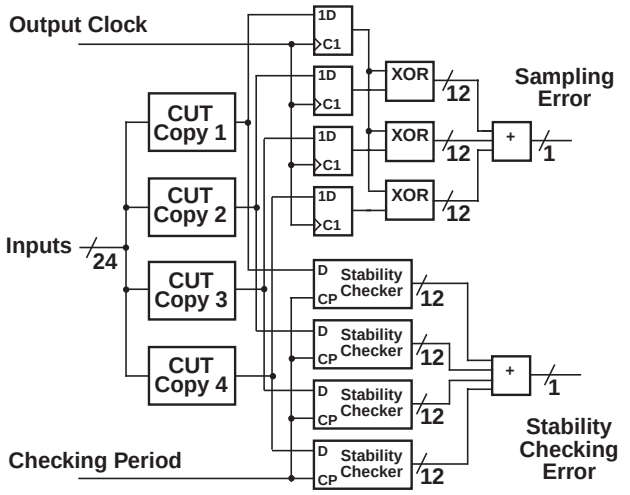

Fig. 2: Comparison Circuit for Response Analysis

Five counters are included for every CUT type. Two 24 bit counters record the first failing vector for sampling and Stability Checking. Three 16 bit counters record the number of failing vectors for sampling, Stability Checking, and Stability Checking only. The values recorded in these counters are used in the following sections to analyze the behavior of defects.

3 TESTS APPLIED

3.1 Test Plan

The two stage testing plan shown in Fig. 3 was adopted for the experiment [1]. Gross parametric and test support circuitry tests (Stage 1 tests) were first applied to each die, and those dice that failed Stage 1 tests were not considered as part of this experiment. This makes the experiment more focused since the gross failures have been removed, and we are interested in the ability of tests to detect the difficult or "elusive" failures.

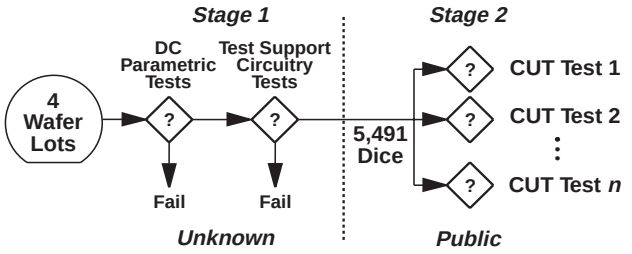

Fig. 3: Testing Stages and Test Result Statistics

CUT tests (Stage 2 tests) were applied to the 5,491 dice that passed Stage 1 tests. These tests include a design verification test set, several single stuck-at test sets using different ATPG tools and with various fault coverages, a switch-level ATPG test set, a stuck-open test set, two transition fault test sets, a gate delay fault test set, and several path delay fault (robust, non-robust, and critical path) test sets, an 2^n exhaustive test, a 2^{2n} super-exhaustive test for the SQR CUT, three I_{DDQ} test sets, and a CrossCheck test set. Most of these test sets were applied at both a normal supply voltage (V_{DD}=5V) and at very-low supply voltage (V_{DD}=1.7V). This paper will focus on tests at normal supply voltage. Results for CrossCheck and a preliminary analysis of Very-Low-Voltage and IDDQ tests were reported in [2].

Apart from IDDQ and CrossCheck tests, output responses of all test sets were captured by both sampling the output voltage and Stability Checking.

3.2 Test Conditions

Each test set was applied to the Test Chip under different test conditions to evaluate the different testing techniques used in practice. The test condition consists of the Data Source, the Clocking Mode, and the Test Timing, which are discussed in turn.

Data Sources

In scan designs, the scan-path ordering places restrictions on consecutive vectors, so not all 2-pattern tests can be applied to the CUT. One solution to this problem is to use an "enhanced" scan chain that can store two values, but this can be expensive. Other approaches include using a "skewed-load" test, where the second pattern is shifted one bit from the first, or functionally propagating the second pattern through the combinational logic [20,21].

Vectors can be applied to the CUTs in two ways, in order to investigate the effect of skewed-load:

- **parallel load**;
- **simulated scan**.

In parallel load, vectors are applied either directly from the ATE, or generated internally by a primitive LFSR. In simulated scan, before each vector is applied, a shifted copy of the vector is applied, to simulate the correlation between consecutive vectors when loading the vectors through a scan chain. Since there is no logic feeding the CUTs, functional propagation was not tested.

Clocking Modes

Delay tests assume that the transients settle before applying the second pattern, which can be difficult to implement in practice. One proposed alternative to delay testing is to apply functional or stuck-at vectors "at-speed", even though this is not necessarily a good delay test [22]. Delay testing uses *slow* and *fast* clocks, whereas at-speed testing uses only *fast* clocks. Methods that combine slow and fast clocks have been proposed, for example [23]. The effect of applying fast clocks instead of slow clocks is addressed in [24].

The main reason for investigating both the at-speed and delay clocking modes is that there has been interest in the tradeoffs between the two methods for detecting timing failures. Three clocking modes were investigated on the Test Chip:

- **DI** -- DIrect clocking mode (at-speed);
- **PU** -- PUlse-width generated clocking mode (delay);
- **IN** -- INternally generated clocking mode (delay).

The DI clocking mode represents "at-speed" or normal clocking of a circuit, while the other two clocking modes represent "delay" clocking, where the first vector is allowed time to settle before the second vector is applied. The first two clocking modes are derived from an external clock, while the third is generated internally by a delay line. Simplified timing diagrams for the different clocking modes are shown in Fig. 4. More details can be found in [1,18]. The *Input Clock* is used to apply data to the CUTs and the *Output Clock* is used to sample the outputs of the CUTs. For a 2-pattern test $<V_1,V_2>$ the time between the application of $<V_2>$ and sampling the output is always the cycle time T_C. The time between the application of $<V_1>$ and $<V_2>$ is T_C for at-speed testing and is large enough to allow the CUT to settle for delay testing.

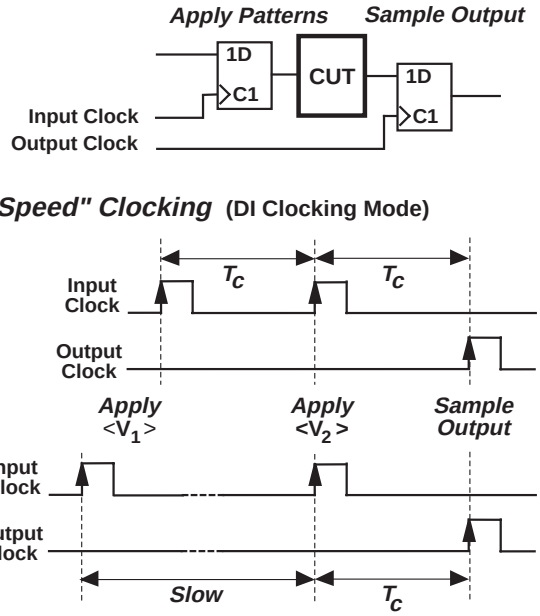

Fig. 4: Timing Waveforms for Clocking Modes

Table 2: Test Sets and Test Conditions

		Data Source:	Parallel Load			Simulated Scan	
		Clocking Mode:	DI	PU	IN	PU	IN
		Test Timing:	s,r,f	s,r,f	n/a	s,r,f	n/a
Test Set	1.1 2.1-13 3.1	Design Verification Single Stuck-At (SSF) Switch-Level		[2]			
	4.1	Pseudo-Random		[2]			
	5.1-2	Weighted Random		[2]			
	6.1	Stuck-Open		[2]			
	7.1-2 8.1-2 9.1-7	Transition Fault Gate Delay Fault Path Delay Fault		[2]			

Test Timing

The test sets were applied at three different clock speeds in order to explore the effect of running tests at different speeds:

- **r** -- *rated* speed of each CUT;
- **s** -- *slower* than rated speed (2/3 rated);
- **f** -- *faster* than rated speed (25% for MUL, SQR, 5% for others).

Table 2 summarizes the tests sets applied to the CUTs, as well as the data sources, clocking modes, and test timing. The shaded boxes in Table 2 indicate that the test was applied under the corresponding conditions. The parallel load PU clocking mode data was reported in [2].

4 SAMPLING TEST RESULTS

4.1 Estimating defective CUTs

The first step in the data analysis is establishing which CUTs are defective. Using this information, escape rates for each test set can be determined. Determining the number of defective die is more complicated than in [2], as the DI and IN clocking modes are also considered.

Note that since each CUT type (4 copies of the CUT) is tested independently of the others, we refer to defective CUT types or CUTs for short, and not defective die. For sampling (boolean) testing, if a CUT fails any of the tests, it will be considered to be defective. This is only an estimate of the true yield as the testing is imperfect and there can be errors in testing. This is not expected to be a major factor, since some of the tests are very thorough, and the repeatability of the testing was checked by repeating the exhaustive test at the end of the test program.

The Venn diagram in Fig. 5 shows the relationship between the failing CUTs for the different clocking modes and speeds. There were 128 CUTs that failed at least one test at either rated or slow timing, and one more CUT that failed at fast timing. The 128 CUTs were on 126 different die, but the analysis is done on a CUT by CUT basis.

These 128 CUTs will be used as the basis for comparing test sets in the remainder of this paper.

Figure 5 shows that there are 121 CUTs that failed at least one test set in each of the clocking modes and speeds, whereas the other 8 defective CUTs escaped some of the clocking modes and speeds. The CUT naming convention used is consistent with [2], except that each CUT starts at 1 (ELM17 and 18 were not in [2]). More detailed data for each test set is presented in Table 3 in the next section.

The fact that only one more CUT failed at the fast timing shows that the clock rate used was conservative. This is expected, as the rated clock speed was based on worst-case design parameters, but due to the statistical nature of component delays, most circuits will operate faster than the worst-case timing. This is important for this experiment, since it means that any timing failures that are found are true delay defects, and not just a result of aggressive timing.

It is also important to note that the defect density (i.e. defects per unit area) is low and fairly constant across all CUT types, as shown in Fig. 6. There are approximately 2 defects per million gates for the Stage 2 CUT tests. This indicates that the process is mature and we are investigating random “spot defects" rather than more gross process problems.

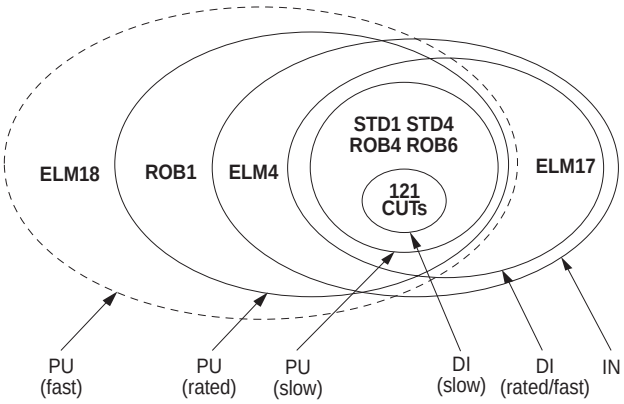

Fig. 5: Failing CUTs for Different Test Clocking Modes

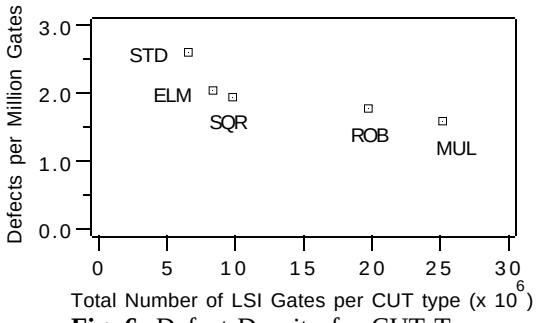

Fig. 6: Defect Density for CUT Types

4.2 Defect Classification

Repeating the test sets for different conditions allows some classification of defective CUTs. Furthermore, the failure counters give much more information than simply pass/fail for each test. First we will define a TIC defect.

Defn.: *Combinational Defect.*

The behavior of the defect only depends on the input pattern applied, and not the previous patterns.

Defn.: *Timing-Independent Defects*

The behavior of the defect does not depend on the clock speed (less than or equal to rated speed).

Defn.: *Timing-Independent Combinational Defect (TIC).*

If a defect has both the above properties, then it is a timing-independent combinational (TIC) defect. For example, a defect that behaves like a stuck-at fault is a TIC defect.

Figure 7 shows that 72 CUTs out of 128 are classified as having TIC defects for the tests applied. For a defect to be classified as a TIC defect in this experiment, both the first failing vector and number of failing vectors must match for each test set, both Data Source modes, the three clocking modes, and slow and rated timing. Note that the actual number of non-TIC defects could be greater than 56, since classified TIC defects are not necessarily TIC defects, they just behave as TIC defects within the resolution of the experiments performed.

For the 72 CUTs that have been classified as TIC defects, the values in the failure counters were compared to a diagnostic dictionary for stuck-at faults, and the analysis shows that 41 CUTs behave like stuck-at faults (pin faults) within the resolution of the experiment. This was determined by comparing the values of the first fail vector and number of failing vectors with a fault dictionary for all the test sets applied to the CUTs. Once again, the actual number could be less than 41.

The 56 CUTs that do not have TIC defects were further classified into "timing" problems and "pattern dependent" problems. This is a very rough classification, as we are only considering two different timings. The results are that 42 CUTs behaved differently for slow and rated timing, and 54 CUTs behaved differently when the pattern preceding each vector was changed.

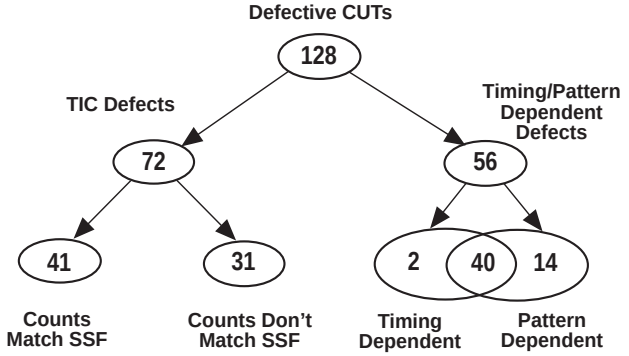

Fig. 7: Defect Classification

4.3 Test Results Summary for Each Test Set

Even though 56 CUTs had non-TIC defects, many of these CUTs were detected by test sets that did not target these defects explicitly. The summary of the test results for the Test Chip are shown in Table 3. The test sets are described in more detail in [2,18]. The table lists the number of test escapes for each test set, under all the clocking modes and timing conditions that the test set was applied, at the rated supply voltage of 5V. The 5 CUTs have been grouped together in this summary, so the escape rates are for a chip containing both control and data-path logic. Note that the number of defective CUTs is 128 for most of the tests, but it is lower, as indicated in the table, for some tests that were not applied to all CUTs (for example, the robust tests were not available for MUL and SQR, and results for DI clocking mode at fast timing are not included as these tests were not applied to the ROB, ELM and STD circuits under these conditions due to tester limitations).

Several observations can be made from Table 3. One observation is that there are substantial differences in escape rates even for similar tests, such as the 100% single stuck-at tests. Applying stuck-at vectors using the simulated scan data source was sometimes better and sometimes worse than the parallel load data source. Running tests at a lower speed clearly increases the escapes. There are differences between the clocking modes at the same test timing. Generally, the PU clocking mode has fewer escapes than the DI clocking mode.

In general, defects that cause timing changes by introducing extra capacitive coupling or ground bounce might be exercised better with a test applied with at-speed timing, whereas defects that depend on charging or discharging a capacitor might be exercised better with a test that allows complete discharging before starting to charge the capacitor (Spice simulations of a simple circuit confirm the possibility of this effect.).

Table 4 lists the actual escaping CUTs for several test sets, divided into SSF-TIC defects, other TIC defects, and non-TIC defects. This shows the relationship between the escapes for the different test conditions.

Table 4 shows that most of the test escapes are for CUTs with non-TIC defects. The 99% coverage stuck-at test also missed one SSF-TIC defect. There is no simple covering relation between the defects detected under the the different test conditions. Even for the exhaustive test, different CUTs escape for the PU, DI and IN clocking modes at the same timing.

5 STABILITY CHECKING TEST RESULTS

All CUT outputs have stability checkers. There are 216 stability checkers per Test Chip, using the conservative 5 gate NAND design described in [16]. For each test, counters in the response analysis circuitry record the total number of sampling and stability checking errors, as well as the first-fail vectors, as described in Sec. 2.

As Stability Checking can be used with all test sets, and all test modes except DI (at-speed) where there is no

Table 3: Number of Test Escapes for All CUTs and Tests (128 defective CUTs except for *, † and ‡)

	Data Source:	Parallel Load						Simul. Scan			
	Clocking Mode:	DI		PU			IN	PU			IN
	Test Set / Test Timing:	s	r	s	r	f	n/a	s	r	f	n/a
1.1*	Design Verification	7	6	7	8	8	8	10	10	9	9
2.1	SSF Tool 1 (100%, gate faults)	14	10	10	9	8	8	10	9	9	10
2.2	SSF Tool 2 (100%, gate faults)	9	7	7	5	3	5	6	3	3	5
2.3	SSF Tool 2 (100%, pin faults)	9	8	8	5	4	6	8	5	5	7
2.4	SSF Tool 3 (100%, pin faults)	15	12	11	10	9	11	14	12	11	13
2.5	SSF Tool 3 (100%, compressed)	15	13	12	11	10	10	14	15	13	14
2.6	SSF Tool 4 (100%, gate faults)	11	8	7	5	5	6	6	4	4	5
2.7	SSF Tool 4 (99.0%)	11	11	8	5	5	7	10	8	8	10
2.8	SSF Tool 4 (98.0%)	12	9	9	7	6	8	9	8	7	7
2.9	SSF Tool 4 (95.0%)	16	13	13	11	11	12	13	11	11	12
2.10	SSF Tool 4 (90.0%)	19	17	18	16	16	17	17	15	14	16
2.11	SSF Tool 4 (80.0%)	26	24	25	23	22	24	25	24	23	24
2.12	SSF Tool 4 -- Min 5 Det/Fault	7	4	4	2	1	3	3	1	1	3
2.13	SSF Tool 4 -- Min 15 Det/Fault	7	4	4	1	1	2	4	1	1	2
3.1	Switch-level ATPG	12	11	11	9	8	10	13	12	12	13
4.1	Pseudo-Random/Exhaustive	7	2	3	1	1	2	-	-	-	-
5.1	Weighted Random - (WR-MUR)	8	5	5	2	2	3	-	-	-	-
5.2	Weighted Random - (WR-WAI)	7	4	4	1	1	2	-	-	-	-
6.1	Stuck-Open ATPG (equiv gate)	8	5	5	3	2	4	5	3	4	4
7.1	Transition Fault, ATPG Tool 5	10	6	6	4	5	6	-	-	-	-
7.2	Transition Fault, ATPG Tool 6	12	11	10	8	7	9	-	-	-	-
8.1†	Gate Delay Fault -- X→0	17	16	18	16	16	16	-	-	-	-
8.2†	Gate Delay Fault -- X→ran	13	11	11	9	9	9	-	-	-	-
9.1	Path Delay -- Crit Path -- X→0	35	35	35	34	34	34	-	-	-	-
9.2	Path Delay -- Crit Path -- X→ran	27	27	28	27	27	27	-	-	-	-
9.3‡	Path Delay -- Robust -- X→0	7	5	4	2	1	3	-	-	-	-
9.4‡	Path Delay -- Robust -- X→ran	8	5	5	3	2	3	-	-	-	-
9.5‡	Path Delay -- Robust Test	7	4	3	2	2	3	-	-	-	-
9.6‡	Path Delay -- Non-Robust-A	12	10	10	7	7	9	-	-	-	-
9.7‡	Path Delay -- Non-Robust-B	8	4	4	2	2	3	-	-	-	-

* 59 Defective CUTs (MUL, SQR)
† 88 Defective CUTs (SQR, ELM, STD, ROB)
‡ 69 Defective CUTs (ELM, STD, ROB)

time for a checking period, tests were not generated specifically for Stability Checking. The results for slow and rated timing are presented below.

5.1 Slow Timing

The results for slow timing are that 34 CUTs have stability checking failures. These are all from the 128 CUTs set that had sampling failures. Furthermore, the 34 CUTs were classified as having non-TIC defects in Fig. 7 based on the sampling tests. Note that these are fairly large delay faults, as the clock rate in slow timing is 2/3 of the rated speed.

Several conclusions can be drawn from this data. First, the stability checkers are operational, otherwise the counts would be zero. Second, there are no "false alarms" or stability checking failures that do not correspond to a CUT with a sampling failure. Third, the Stability Checking results are consistent with the sampling results at different speeds in identifying CUTs with timing defects.

Another area of interest is the possibility of invalidation of tests for delay faults by hazards in the CUT. The Stability Checking results show that it is possible. For example, in PU clocking mode, slow timing, there are 3 CUTs (MUL4, ROB4, STD4) for the parallel load data source and 4 CUTs (MUL4, MUL40, ROB6, STD4) for the simulated scan data source, for which some test sets produce Stability Checking failures but no sampling failures. For the parallel load data source, there are 4 test sets with this property for MUL4 (1.1, 2.1, 2.4, 2.11), 2 for ROB4 (2.3, 8.1), and 4 for STD4 (2.1, 9.1, 9.2, 9.3). Furthermore, the above 4 test sets for MUL4 also had no sampling failures at rated speed.

Table 4: Actual CUT Test Escapes for Select Test Sets

test	Data Source	CLK Mode	Timing	SSF TIC	Other TIC	Non-TIC	Total Escapes
4.1	Parallel	PU	slow			ELM4,17 ROB1	3
(exh)	Parallel	PU	rated			ELM17	1
	Parallel	PU	fast			ELM17	1
	Parallel	DI	slow			ELM4,17 STD1,4 ROB1,4,6	7
	Parallel	DI	rated			ELM4 ROB1	2
	Parallel	IN	n/a			ROB1,6	2
5.2	Parallel	PU	slow			ELM4,17 ROB1 STD4	4
(WR)	Parallel	PU	rated			ELM17	1
	Parallel	PU	fast			ELM17	1
	Parallel	DI	slow			ELM4,17 ROB1,4,6 STD1,4	7
	Parallel	DI	rated			ELM4,17 ROB1 STD4	4
	Parallel	IN	n/a			ELM4 ROB1	2
2.4	Parallel	PU	slow		MUL2,11	ELM4,17 ROB1 STD4 MUL1,4,9,10 SQR1	11
(SSF)	Sim. Scan	PU	slow		MUL2,11	ELM4,17 ROB1,7 STD4 MUL1,3,4,5,9,10 SQR1	14
(100%)	Parallel	PU	rated		MUL2,11	ELM17 STD4 ROB1 MUL1,4,9,10 SQR1	10
	Sim. Scan	PU	rated		MUL2,11	ELM17 ROB1,7 SQR1 MUL1,3,4,5,9,10	12
	Parallel	PU	fast		MUL2,11	ELM17 STD4 SQR1 MUL1,4,9,10	9
	Sim. Scan	PU	fast		MUL2,11	ELM17 ROB7 SQR1 MUL1,3,4,5,9,10	11
	Parallel	DI	slow		MUL2,11	ELM3,4,17 ROB1,4,6 STD1,4 SQR1 MUL1,4,9,10	15
	Parallel	DI	rated		MUL2,11	ELM4,17 ROB1, STD1,4 MUL1,4,9,10 SQR1	12
	Parallel	IN	n/a		MUL2,11	ELM4,17 STD4 ROB1 MUL1,4,9,10 SQR1	11
	Sim. Scan	IN	n/a		MUL2,11	ELM4,17 ROB1,7 SQR1 MUL1,3,4,5,9,10	13
2.6	Parallel	PU	slow		ROB2	ELM4,17 ROB1,3,7 STD4	7
(SSF)	Sim. Scan	PU	slow		ROB2	ELM4,17 ROB1,7 STD4	6
(100%)	Parallel	PU	rated		ROB2	ELM17 ROB1,3,7	5
	Sim. Scan	PU	rated		ROB2	ELM17 ROB7,9	4
	Parallel	PU	fast		ROB2	ELM17 ROB1,3,7	5
	Sim. Scan	PU	fast		ROB2	ELM17 ROB7,9	4
	Parallel	DI	slow		ROB2	ELM3,4,17 ROB1,3,4,6,7 STD1,4	11
	Parallel	DI	rated		ROB2	ELM3,4,17 ROB1,3,7 STD4	8
	Parallel	IN	n/a		ROB2	ELM4,17 ROB1,3,7	6
	Sim. Scan	IN	n/a		ROB2	ELM4,17 ROB1,7	5
2.7	Parallel	PU	slow	ELM1	MUL2 ROB2	ELM4,17 ROB1,9 STD4	8
(SSF)	Sim. Scan	PU	slow	ELM1	MUL2 ROB2	ELM4,17 ROB1,7,9 STD4 MUL1	10
(99%)	Parallel	PU	rated	ELM1	MUL2 ROB2	ELM17 ROB9	5
	Sim. Scan	PU	rated	ELM1	MUL2 ROB2	ELM17 ROB7,9 STD4 MUL1	8
	Parallel	PU	fast	ELM1	MUL2 ROB2	ELM17 ROB9	5
	Sim. Scan	PU	fast	ELM1	MUL2 ROB2	ELM17 ROB7,9 STD4 MUL1	8
	Parallel	DI	slow	ELM1	MUL2 ROB2	ELM4,17 ROB1,4,6,9 STD1,4	11
	Parallel	DI	rated	ELM1	MUL2 ROB2	ELM3,4,17 ROB1,6,9 STD1,4	11
	Parallel	IN	n/a	ELM1	MUL2 ROB2	ELM4,17 ROB1,9	7
	Sim. Scan	IN	n/a	ELM1	MUL2 ROB2	ELM4,17 ROB1,7,9 STD4 MUL1	10
2.13	Parallel	PU	slow			ELM4,17 ROB1 STD4	4
(SSF)	Sim. Scan	PU	slow			ELM4,17 ROB1 STD4	4
(15x)	Parallel	PU	rated			ELM17	1
	Sim. Scan	PU	rated			ELM17	1
	Parallel	PU	fast			ELM17	1
	Sim. Scan	PU	fast			ELM17	1
	Parallel	DI	slow			ELM4,17 ROB1,4,6 STD1,4	7
	Parallel	DI	rated			ELM4,17 ROB1 STD4	4
	Parallel	IN	n/a			ELM4 ROB1	2
	Sim. Scan	IN	n/a			ELM4 ROB1	2

5.2 Rated Timing

At rated timing, there were 188 Stability Checking failures. This is significantly more than expected, and almost all the "extra" failures were due to the ROB circuit.

In order to understand this behavior, the clock rate on the ATE was increased slowly to find the first sampling and Stability Checking error, and it was found that the Stability Checkers started checking the output waveform too early. This is a consequence of the Stability Checker design being separate from the sampling flip-flop, and the timing to the two circuits was not controlled accurately enough. Unfortunately this makes direct comparison between the different techniques more difficult at the rated timing, as outputs that change just before the setup time of the sampling flip-flop will have Stability Checking errors. This shows that it is very desirable to incorporate the stability checker into the flip-flop design to minimize skew problems.

6 SIGNATURE ANALYSIS TEST RESULTS

Hardware was included in the Test Chip to permit a thorough analysis of the aliasing behavior of both serial and parallel signature analyzers. Intermediate signatures were also taken, which can be processed in various ways, such as investigating multiple signature schemes. Due to area limitations, only one of the CUTs, the MUL, has a signature analyzer.

No instance of aliasing was observed for any of the 168 tests applied to each MUL CUT type. This is probably not very surprising, as the sample size for the signature analysis experiment turned out to be very small (only 40 MUL CUTs failed any of the sampling tests at normal voltage).

Another purpose of the signature analysis experiment was to see what fraction of failures behave exactly as stuck-at faults. Of the 40 defective MUL CUTs, 17 were classified as having TIC defects and 7 matched single stuck-at faults based on the failure counters.

A dictionary of single stuck-at fault (SSF) signatures was computed, against which the observed faulty signatures were matched. Table 5 show that for 5 CUTs every single failing signature matched a single stuck-at signature, and 2 CUTs matched most of the failing signatures. This is strong evidence that there are some defects (5 of 40 in this case) that behave just like stuck-at faults.

Table 5: Signature Analysis Diagnostic Results

CUT	# Failing Signatures	# Matching SSFs
MUL8	45	**4 1**
MUL13	39	39
MUL14	43	43
MUL16	37	37
MUL19	31	31
MUL25	27	**2 5**
MUL27	37	37

7 VALIDITY OF EXPERIMENTAL RESULTS

When doing an experiment of this nature there is always the question of repeatability of results. It has been reported in [25] that almost half of the failed parts passed retest. In this experiment, special effort was made to ensure repeatability, as many of the primary causes of problems mentioned in [26] have been minimized or checked (e.g. program software errors, improper initialization, race conditions, uncalibrated hardware, etc.)

As verification, the exhaustive test was repeated at the end of the test sequence (after the Very-Low-Voltage and IDDQ tests). Table 6 shows the results for both the first-fail vector and the total number of failing vectors. Of the 128 CUTs that have been considered in this paper, 110 have identical responses and 9 more are close (counts within 10%), verifying the repeatability of the experiment. A few variations are expected as there are many CUTs with timing failures. (The 5 missing are due to the IDDQ value being high enough to abort the test.)

An example of close counter values is MUL1, where the first failing vector for sampling was 2,736 for both tests, and the number of failing vectors was 1,280 and 1,281 for the first and last test respectively.

ELM4 and MUL4 are interesting because the number of failing vectors decreases significantly for the second test. For ELM4, the first sampling failure is vector 29 with 58,476 total sampling failures for the first test, whereas the first sampling failure is vector 26,488 with only 461 sampling failures for the second test.

Table 6: Repeatability Results

Comparison	#	CUTs
Identical	110	
Close	9	ROB1,6,9,18 STD4,12 MUL1,6,15
Different	4	ROB15,20 ELM4 MUL4
Missing	5	ROB34,35 MUL38,39,40
Total	128	

8 PROPAGATION DELAY MEASUREMENTS

The results presented in this section were not part of the main experiment, and were done to investigate issues related to the modeling of delay, as limitations of conventional delay fault models have been suggested.

Accurate propagation delay measurements were taken for the SQR CUT, to investigate the effect of inaccurate modeling of gate delay in practice. This CUT has only 12 inputs, making the super-exhaustive test possible. The CUT consists of two cascaded multipliers, and there are $7x10^{15}$ structural paths in this circuit, so test pattern generation for all paths was not possible, as is often the case in practice. As this test was very time-consuming, it has only been done for 4 SQR CUTs.

Figure 8 shows the clocking mode (PU clocking mode) and clock waveform used for this test.

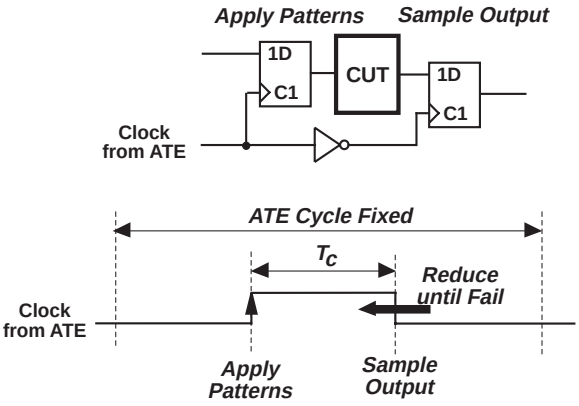

Fig. 8: Test Setup for Measuring Propagation Delays

Patterns were applied to the CUT on the rising edge of the clock, and the CUT outputs were sampled on the falling edge of the clock. The advantage of this type of clocking is that the only timing-critical pin on the ATE is the clock, so that skew between tester pins does not have to be taken into account. The duty cycle of the clock was decreased in 25 ps steps until the CUT started failing.

The tests applied are shown in Table 7. The critical path test only tested the 100 longest paths for rising and falling transitions. The paths were chosen using a simple gate delay model (unit delay). For the critical path, gate delay, and robust tests, the test generators left unused inputs at X. The tests were repeated with 0s assigned to the X's, as well as 0 or 1 randomly assigned to the X's. All vectors were sampled, as well as every second vector as is normally done for delay testing.

Table 7: Tests Applied to SQR CUT

Test Set		Length	Strobes
2.4	Single-Stuck-Fault	22	22
7.2	Transition Fault	304	152
9.1	Critical Path, X→0	1,692	846
9.2	Critical Path-R, X→ran	1,692	846
9.2	Critical Path-R2, X→ran, Sample all	1,692	1,692
8.1	Gate Delay, X→0	976	488
8.2	Gate Delay-R, X→ran	976	516
	Exh-pr (LFSR)	4,096	4,096
	Exh-gray (Single Trans.)	4,096	4,096
	Exh-max. Trans.	4,096	4,096
4.1	Super Exhaustive	16.8M	16.8M

Figure 9 shows the experimental results for the SQR CUT. The propagation delays on four die were measured, and the maximum and minimum values relative to the "super-exhaustive" test were plotted. The longest delay is not exercised by any test except the "super-exhaustive" test. For this circuit, the results for the single-stuck, transition, and critical path tests were very similar. For example, the stuck-at test needs to be applied about 10% faster than the desired speed of the CUT in order to detect timing failures.

Three exhaustive tests were also applied. The first was generated with a primitive polynomial, the second is a gray code with single bit transitions between vectors, and the third test maximizes the number of transitions between vectors (either *n* or *n*-1, for an *n*-bit vector). The gray code performs very poorly, and the circuit must be clocked at least 22% faster than the worst-case delay to detect the delay fault. The node activity for the three exhaustive tests was computed, and as expected, the activity for the gray code was significantly lower than for the other two tests (12% compared to 24% for the pseudo-random, and 33% for the maximal-transition test).

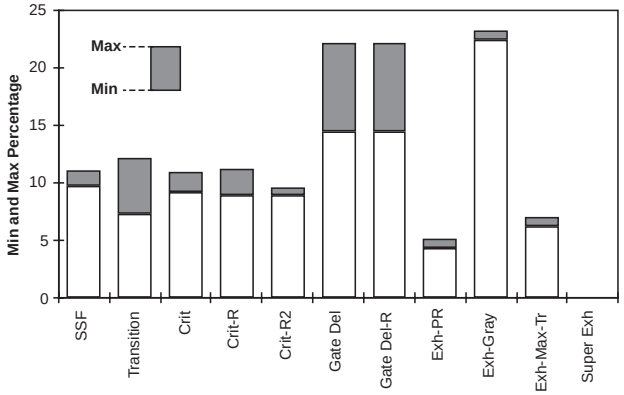

Fig. 9: Relative SQR CUT Propagation Delay Results

The propagation delay measurements in this section show that the longest delays in circuit are not exercised by using test sets generated using a simple delay model. Even passing an exhaustive test does not guarantee that the circuit functions at the designed speed.

The critical path test was no better than the stuck-at tests. This shows the danger in testing only a small fraction of the paths in the circuit, and using an inaccurate model to choose the paths.

(Approximately 100 measurements were remade to check the repeatability of the ATE, and all measurements for the SQR CUT were within 25 ps, so there were no ATE consistency problems.)

9 CONCLUSION

This paper presents new results from the Test Chip experiment, covering different clocking modes and speeds. The emphasis of the paper has been on timing failures.

The main result is that even for a mature process, timing or pattern dependent defects make up a significant fraction (44%) of the defect population. There are at least 42 CUTs with defects that are timing dependent out of 128 CUTs, and at least 54 CUTs for which the behavior depends on the previous pattern applied. These could be delay , stuck-open , or even feedback bridging faults.

Of the 72 TIC defects at most 41 were accurately modeled by stuck-at faults (the signature analysis shows

that some defects behave very much like stuck-at faults). Due to the detection of non-targeted faults, however, the escape rate for stuck-at tests for different clocking modes was between 6 and 15 CUTs for slow timing, and between 3 and 15 CUTs for rated timing.

In terms of individual test sets, it is difficult to compare those with few escapes with enough statistical significance. However, there was a definite drop in defect coverage when the tests were run at slow speed, and generally, "delay" application of vectors was better than "at-speed" application of vectors. No test set had fewer than 7 escapes with "at-speed" application of vectors at slow speed.

The Stability Checker designs functioned as expected at the lower clock rates, and cases of test invalidation by hazards were found.

The results of the propagation delay measurements show that none of the tests applied sensitized the longest delay through the circuit, as indicated by their performance versus the super-exhaustive test.

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