Error Sequence Analysis

Jaekwang Lee, Intaik Park and Edward J. McCluskey
Stanford University
{jaekwang, intaik, ejm}@stanford.edu

Abstract

With increasing IC process variation and increased operating speed, it is more likely that even subtle defects will lead to the malfunctioning of a circuit. Various fault models, such as the transition fault model and the path-delay model, have been used to aid delay defect detection. However, these models are not efficient for small-delay defect coverage or for test pattern generation time. Error sequence analysis utilizes the order in which the errors occur during a frequency sweep of a transition test to identify small-delay defects that may escape the same test applied in the conventional way. Moreover, it can detect such defects even in the presence of inter-die process variations, such as lot-to-lot and wafer-to-wafer process variation. In addition, error sequence analysis is very effective in separating devices with delay defects from devices that have failed due to process variation.

1. Introduction

An error sequence refers to the order of error occurred during a frequency sweep test. A *frequency sweep test* is the application of a launch-on-capture transition test set [Savir 94] at various clock frequencies from slow speed to fast speed. As the clock frequency increases, new errors occur. The *error sequence* is the order in which errors occur during the frequency sweep test.

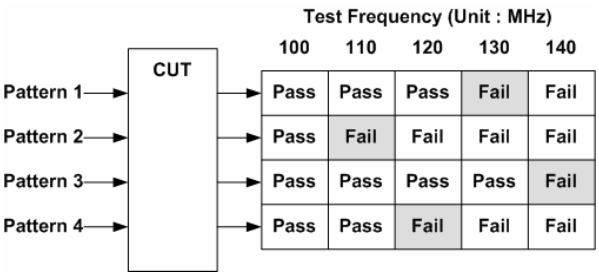

Figure 1. Frequency Sweep Output Table

For example, in Fig. 1, the clock frequency sweeps from 100MHz to 140MHz in 10MHz steps with a test set consisting of 4 test patterns. Pattern 2 starts to fail at 110MHz, pattern 4 at 120MHz, pattern 1 at 130MHz, and finally pattern 3 starts to fail at 140MHz. In this case, the error sequence is pattern 2-4-1-3.

In a defect-free Integrated Circuit test, the longest sensitized signal path will fail first, followed by other sensitized paths based on their path-delays; this ordered set of errors becomes the error sequence of the circuit. The error sequences of defect-free ICs would be similar regardless of inter-die process variation, because the inter-die process variation often affects the delay of all paths in the circuit.

Assume that there is a switching delay defect in logic gate or interconnect. If the defect is activated by some patterns, the defect will lengthen the delay of sensitized paths; thus, the paths will fail earlier than usual. If the size of the delay defect is greater than the granularity of the sweeps, the error sequence will differ from that of a good circuit. For example, when there is no defect in the circuit (Fig. 2.a), and four paths (A-C-D, A-C-E, B-C-D, and B-C-E) are sensitized by a pattern set, path A-C-E is the second longest path, failing earlier during the frequency sweep than any other signal path, except for path A-C-D. The path A-C-E fails at a clock period of 0.75ns. However, if there is an additional 0.25ns delay defect in block B (Fig. 2.b), this delay is added to path B-C-D, which now becomes the second longest path. Therefore, a delay defect might change the sequence of the error occurrence, and error sequence analysis will detect it.

This 0.25ns additional delay defect at block B may not be detected during conventional testing, because the total delay of path B-C-D with the delay defect is still shorter than the test clock period. However, in a field operation, some paths that have not been tested by a test pattern set can be sensitized, and the defect can be propagated to those paths, possibly causing a malfunction. By observing the change in error sequences, error sequence analysis can also detect these hard-to-detect small delay defects.

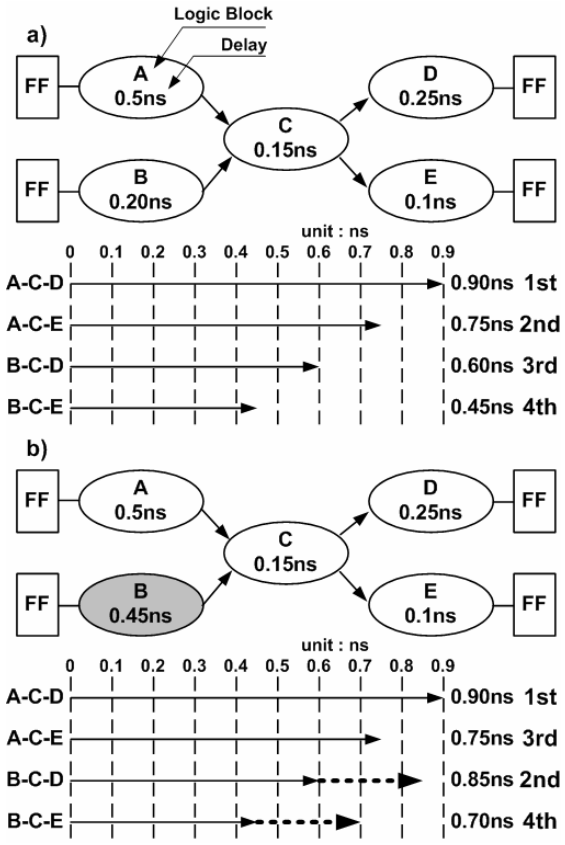

Figure 2. a) Error-free Status of System; b) a 0.25ns Additional Delay Defect at Block B

In previous research, Yan and Singh [Yan 03] [Yan 04] compare the switching delay of adjacent dies to detect small-delay defects using multiple clock frequencies. Since the process variations in the neighboring dies are much smaller than the process variations in the dies located on different wafers or lots, circuits with small-delay defects can be separated from slower circuits due to the process variation. However, this method cannot detect small-delay defects in the short path, because it can be masked by the longer paths as in the above example. Nevertheless, these defects can still affect the system if the defects are propagated to untested long paths in field operation. Error sequence analysis detects multiple errors by sweeping the test clock frequency and sequencing the errors; thus, small-delay defects in the short paths can also be detected.

Kruseman et al. and Turakhia et al. identify small-delay defects using multiple pattern groups [Kruseman 04] [Turakhia 07]. Each group is composed of patterns that have similar path lengths. This method reduces the variation in the path length of a test set; therefore, small-delay defects masked by long paths can easily be detected. However, hazard-free paths are necessary in this method, which result in decreased defect coverage and increased test vector generation time. Error sequence analysis sweeps the test frequency; thus, it can detect the start-to-fail frequency even for hazardous patterns when the size of the hazard is larger than the frequency sweep granularity; this fact was demonstrated in [Yan 03].

In ELF18 tests, the start-to-fail clock period of the pattern with longest path-delay varies from 8.2ns (fast devices) to 10.6ns (slow devices). Even though the pattern groups with similar path-delays are used, their failing clock period may vary considerably due to process variation, and small-delay defects hidden in the fast devices will not be fully detected. However, error sequence analysis can detect the defects even in the presence of process variation.

In this paper, section 2 presents the advantages of error sequence analysis; section 3 considers issues in using error sequence analysis. ELF18 test results are presented in Section 4; section 5 concludes this paper and discusses future work.

2. Advantages of Error Sequence Analysis

Error sequence analysis is effective in detecting small-delay defects without using thorough tests that were mentioned in [Nigh 2004]. These methods can detect most defects but require a considerable amount of time to generate. Also, error sequence analysis remains effective in the presence of inter-die process variation.

2.1. Small-delay Defect Detection

The transition fault model [Waicukauski 87] was proposed to detect the delays in either a rising or falling transition. One advantage of the transition fault model is the fact that test vector generation algorithms are easy to apply because the algorithms are based on the stuck-at fault model. In addition, the number of faults is linear in the number of fault sites, meaning that pattern generation takes less time than in the path-delay fault model [Smith 85] whose number of faults might increase exponentially with the number of nodes.

However, the transition fault model is not effective in detecting small-delay defects when the size of the defect is smaller than the path slack. For example, in Fig. 3, two paths of Fig. 2 are shown: B-C-D and A-C-E, in addition to another path B-F. When the transition fault model is used, conventional automatic test pattern generation (ATPG) tools might propagate the defect to a shorter path. In that case, the ATPG tool might set the propagation path for the delay defect at block B as B-C-D; then, the path slack is 0.3ns; this 0.25ns delay

defect will not be detected. However, this undetected small-delay defect would affect path B-F, giving a faulty path-delay of 1.05ns > 1.0ns.

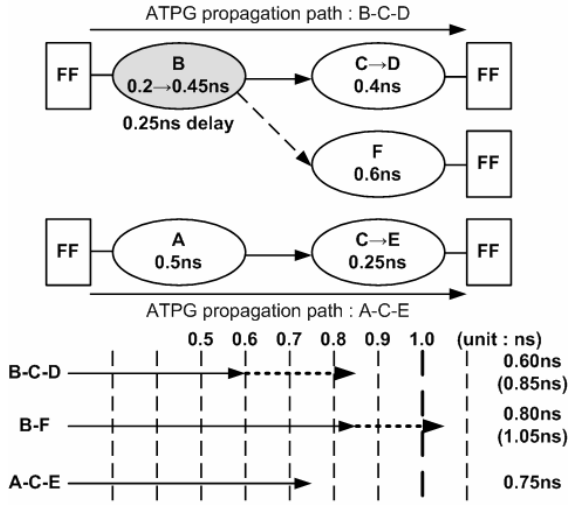

Figure 3. Transition Fault Model vs. Error Sequence Analysis (test clock period: 1.0ns)

This small-delay defect could be detected by error sequence analysis using the same transition fault test vectors. There is a propagation path A-C-E whose nominal delay is 0.75ns. In the fault-free case, the delay of path B-C-D is 0.60ns. Thus, path B-C-D is detected later on a frequency sweep test than path A-C-E. On the other hand, given the 0.25ns delay defect, the delay of path B-C-D becomes 0.85ns, meaning that path B-C-D is detected earlier than path A-C-E - the 0.25ns small-delay defect at block B is detected. Therefore, error sequence analysis can detect small-delay defects that may escape a transition-fault-based test using the same test vectors.

The path-delay fault model can also be used to detect small-delay defects. Ideally, this model tests all the paths in a circuit; if the cumulative delay of any path exceeds the clock period, the circuit fails the test. Therefore, it can detect the small-delay defects distributed throughout the path in the circuit. However, the number of faults, which is equal to the number of paths, increases exponentially with circuit size, meaning that pattern generation and application is impractical.

Various algorithms, such as K-Longest Path Per Gate Algorithm [Qiu 03] [Qiu 04] and ALAPTF [Gupta 04], were proposed to reduce the pattern generation time in the path-delay fault model. However, in field operation the longest actual paths might be different from the tested paths [Turakhia 07].

On the other hand, error sequence analysis does not require propagating the defect to longer paths; if a pattern can activate the defect and propagate it to any path, the error sequence would be changed and error sequence analysis might detect it. In other words, the analysis does not require detailed delay information about the circuit under test nor complicated algorithms to propagate the defect to longer paths.

2.2. Process variation

Process variation can make changes in the parametric values of a circuit, such as the operating speed, the quiescent current, the threshold voltage and the minimum operating voltage. For example, if the threshold voltage increases, gates operate more slowly because, given the same gate voltage V_G, the gate overdrive voltage (V_G–V_T) decreases; then, less current flows through the channel. This reduced current affects the operating speed of the circuit. As the gate dimensions decrease, controlling the manufacturing process becomes more difficult; thus, the process variation increase, and a single test frequency for a delay test would not be effective for devices with small-delay defects.

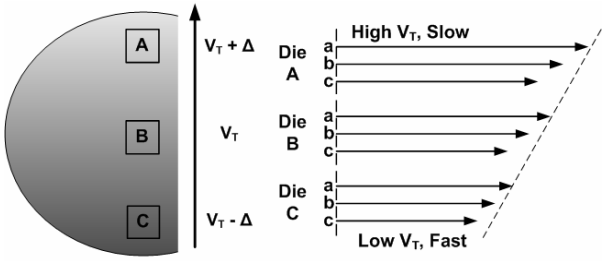

Figure 4. Process Variation within a Wafer

An example of a threshold voltage shift with respect to path-delays is shown in Fig. 4. Even though the device speed changes, the order of path-delays within a device would be similar. Error sequence analysis considers the order of error occurrence during the frequency sweep, i.e. the relative delay of paths. Therefore, it is effective even in the presence of inter-die process variations, such as wafer-to-wafer and lot-to-lot process variation.

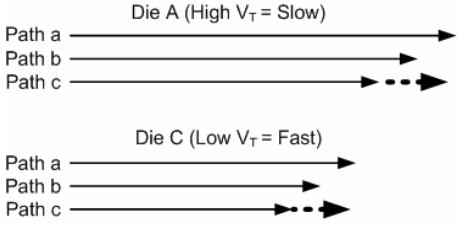

Figure 5. Path Delay When Both Small-delay Defects and Process Variation Exist

In Fig. 5, path-delays of die A and die C of Fig. 4 are shown. An extra delay in path c caused by a delay defect is represented by the dotted lines. In this example, despite the different path-delays, the small-delay will change the order in which paths a, b, and c fail during the frequency sweep, meaning that the error sequence would be different for each.

3. Considerations in Error Sequence Analysis

3.1. Testing Time

Error sequence analysis requires a frequency sweep; the test set is applied several times at various test clock frequencies. For example, if 20 different frequencies are used for frequency sweep test, this test may take at least 20 times more time than transition test. Furthermore, the results of each application must be logged, which may take significant storage space. Therefore, error sequence analysis might be too expensive for production tests.

However, there are some devices that pass all the manufacturing tests but fail in the field; these devices are test escapes. Figure 3 of Section 2.1 is a good example of a test escape. This example passes the transition test; however, if the delay defect at block B is activated and propagated to the longer path F, the system will fail. If the device is returned and tested using the same test vectors, the device will pass the test again. These devices are called "No Trouble Found" (NTF) and the defects in the NTF devices are usually very hard to detect. There are several approaches to discovering causes of fault in NTF devices, such as using very thorough patterns, running the device at various operating conditions, and additional burn-ins; these approaches are usually very expensive.

Error sequence analysis can be effective in failure analysis in NTF devices. Error sequence analysis can detect small-delay defects without the need for generating additional thorough test patterns. If a pattern set can sensitize the defective path and the granularity of the frequency sweep is smaller than the defect size, the small-delay defects can be detected using error sequence analysis. Therefore, the delay test patterns, which could not detect those small-delay defects in production test, can be effectively used in error sequence analysis. In addition, error sequence of a device can be a good characterization of a device; thus, error sequence analysis can be applied in characterization tests in which thorough testing and analysis are required.

3.2. Intra-die Process variation

Even though the effect of intra-die process variation (a.k.a. within-die process variation) is smaller than that of inter-die process variation, it cannot be ignored because it can affect the error sequence of the defect-free paths with a similar path-delay. Therefore, error sequences which can easily be reversed by the effect of the intra-die process variation should be identified and those sequences should not be counted in error sequence analysis.

Error Sequence Table can be used to discover sequence relations among errors. In Table 1, the number at row P_X, and column P_Y is the number of times that pattern X fails earlier than pattern Y in the frequency sweep test. For example, pattern 1 fails before pattern 2 with a frequency of 60%, and the error at pattern 3 appears before the error at pattern 2 with a frequency of 30%. In this example, sequence P1-P2 is less clear (60%) than sequences P1-P3 (95%) and P1-P4 (100%). In other words, sequence P1-P2 can be easily reversed by the effect of intra-die process variation. In this case, the reverse sequences in P1-P3 and P1-P4 are more considerable than the reverse sequence in P1-P2. Setting the threshold for a significant sequence is determined by the test thoroughness goal.

Table 1. Error Sequence Table (unit : %)

	P1	P2	P3	P4
P1		60	95	100
P2	40		70	90
P3	5	30		55
P4	0	10	45	

3.3. Setting Sweeping Step Size and Range

In error sequence analysis, the frequency sweep step size and range determine the resolution of the analysis. If the frequency sweep step size is large, small-delay defects which are smaller than the step size might not be detected. However, if the frequency step size is small, the test cost rises. If the sweep range is small, small-delay defects propagated in very short paths would not be detected, even at the highest frequency in the range. On the contrary, if the frequency sweeping range is large, the test cost is high. Therefore, setting the appropriate step size and the range is a trade-off between test resolution and test cost.

Pattern	730	73	1058	1163	616	566	1214	130	1093	138
730		100%	100%	100%	100%	100%	100%	100%	100%	100%
73	0%		68.4%	73.5%	77.9%	76.9%	85.9%	96.3%	92.9%	93.8%
1058	0%	10.2%		32.0%	33.5%	48.1%	48.7%	94.1%	85.4%	90.8%
1163	0%	10.5%	14.3%		30.9%	34.6%	42.0%	79.1%	79.5%	88.0%
616	0%	6.1%	11.2%	28.8%		32.8%	33.8%	78.6%	88.3%	85.0%
566	0%	8.0%	13.6%	22.6%	24.9%		37.5%	78.4%	88.3%	94.7%
1214	0%	4.0%	5.3%	19.5%	6.0%	24.3%		66.0%	64.8%	73.0%
130	0%	0.4%	0.1%	1.0%	1.2%	1.2%	3.8%		24.7%	37.8%
1093	0%	1.6%	1.4%	0%	0.6%	0.6%	7.9%	22.8%		30.6%
138	0%	1.5%	0.8%	0.2%	1.3%	0.2%	4.2%	19.0%	13.9%	

Table 2. Error Sequence Table of First 10 Failing Patterns

4. Experiments

Error sequence analysis was performed on Stanford CRC ELF18 test chips. ELF18 chips were manufactured by Philips 0.18um Corelib technology. Each chip consists of 6 DSP cores, in which R.E.A.L Digital Signal Processing cores are implemented [Mitra 04]. In this experiment, 2,748 ELF18 cores were used. They were tested using a test set generated by the transition fault metric. The pattern has 1,417 test vectors and 97% transition fault coverage. During clock period sweeping, the step size was 100ps; the range was 1ns from the first failing period of the test core. For instance, if a core begins to fail at the 10ns clock period, the sweep range is 10ns to 9ns.

Table 2 shows the Error Sequence Table for the 10 most frequently failing patterns. These patterns fail sooner than other patterns during the frequency sweep test. As mentioned in Section 3.2, the number at row x, and column y is the percentage of times that pattern x fails before pattern y. For instance, pattern 73 fails earlier than pattern 1214 with a frequency of 85.9%, the reverse sequence occurs with a frequency of 4.0%, and both errors occur at the same clock period with a frequency of 10.1% (=100%-85.9%-4.0%). Even among the first 10 failing patterns, there are some noticeable error sequences; for example, pattern 730 always fails earlier than any other patterns, and pattern 73 fails earlier than pattern 130 with the percentage of 96.3%, but the reversed sequence happens with percentage of 0.4%.

After ELF18 test, there were 146 cores which violated the error sequence significantly; these failing cores show the error sequences whose possibility are less than 1%. Transition test with same test vectors was also done for the suspect cores. The transition fault test was performed at the clock period of 100MHz, set by the manufacturer's suggestion and the shmoo plots of good cores. Among the Error Sequence Analysis failing cores, 38 cores fail only the error sequence analysis; 108 cores fail both the error sequence analysis and the transition fault test.

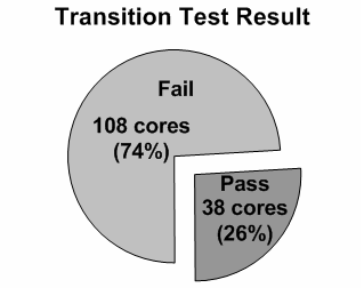

Figure 6. Error Sequence Analysis Failing Cores Analysis

This result shows that Error Sequence Analysis can detect additional defective cores that conventional transition fault test cannot detect. Cores that pass the transition test but fail the error sequence analysis are suspect cores. The delay defects in suspect cores can affect the system in the field operation if two conditions are satisfied: 1) the delay defects are propagated to untested long paths; 2) the size of the defect is larger than the path slack of the long path. Nevertheless, if both conditions are not satisfied, the system will operate correctly regardless of the existence of defects. Removing these devices might result in a yield loss; therefore, error sequence analysis is not acceptable as a production test, but is acceptable for analyzing NTF devices, because the analysis can detect hard-to-detect delay defects using the same test sets as production tests.

Figure 7 shows the error sequences of four cores. Core a) is a good core; it passes the transition test and error sequence analysis. Cores b) and c) fail the transition test; however, the cause of the failure might be different for each. In core b), there is no error sequence reversal; thus, the reason for the failure might be a reduction in speed due to process variation, but in

core c), the error at pattern 405 occurs much sooner than the other errors, meaning that there might be a delay defect in the path related to pattern 405. Core d) passes the transition test; whereas the error at pattern 242 occurs much sooner than usual, indicating a delay defect. Consequently, error sequence analysis can be effective in analyzing the delay defective devices.

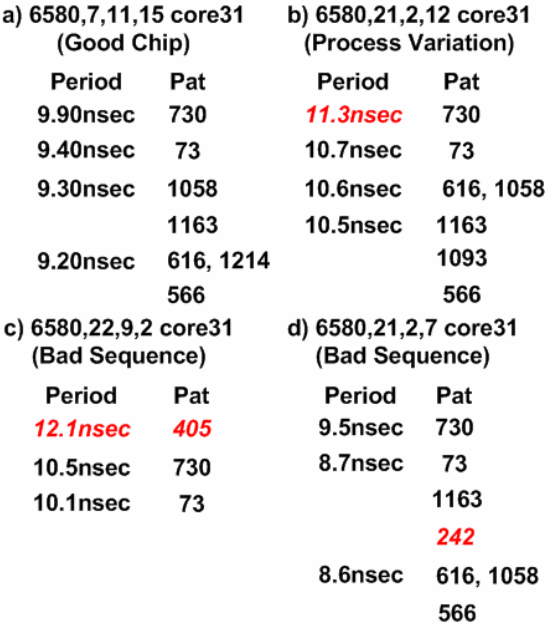

Figure 7 Error Sequences of Four Cores a) Good Core, b) Fails Transition-fault Test, c) Fails Both, d) Fails Error Sequence Analysis

5. Conclusions and Future Work

Error sequence analysis can detect delay defects by comparing the error sequence following a frequency sweep test. Even if the size of the delay defects is small, error sequence analysis can detect the defect without generating additional thorough test patterns. In addition, error sequence analysis is effective even in the presence of inter-die process variation because it compares the relative order of path-delays. Therefore, error sequence analysis will effectively separate delay defective cores from the cores that fail due to process variation. Because the frequency sweep is very expensive, this technique can be used in NTF analysis and characterization tests, for which thorough tests are necessary and test cost might not be a major issue. Some consideration can be given to improving the test quality and test time of error sequence analysis.

For instance, very low voltage testing [Hao 93] can be combined to the error sequence analysis. Very low voltage testing was proposed to detect resistive shorts in a circuit. Since the effect of resistive shorts increases at low voltage, the frequency sweeping step size can increase, which will reduce the test time of the error sequence analysis.

6. Acknowledgments

The authors would like to thank Bill Price, Stefan Eichenberger, and Fred Bowen of NXP for providing the ELF18 test chips, and Erik Volkerink of Verigy for providing the tester time. The authors also thank Kyoung Youn Cho of Stanford CRC for his support in the test experiment.

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