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AN EXPERIMENTAL CHIP TO EVALUATE TEST TECHNIQUES EXPERIMENT RESULTS

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Abstract

This paper describes the testing of a chip especially designed to facilitate the evaluation of various test techniques for combinational circuitry. The different test sets and test conditions are described. Several tables show the results of voltage tests applied, either at rated speed or 2/3 speed, to each defective CUT. Data for CrossCheck, Very-Low-Voltage, IDDQ and delay tests are also given.

1. Introduction

The design of an experiment to evaluate combinational circuit test techniques is described in a companion paper, [1]. This paper discusses the wafer sort test procedure and presents some of the test data collected. LSI Logic manufactured four wafer lots of the test chip which were tested on a 100MHz Tester (Schlumberger ITS9000FX) by Digital Testing Services. Each die contains a number of circuits-under-test (CUTs) and test support circuitry, including on chip pattern generators, output response analyzers, and CrossCheck circuitry, [2]. Gross parametric and test support circuitry tests (Stage 1 tests) were applied to each die, and those dice that failed Stage 1 tests were excluded from this experiment. All of the dice passing the Stage 1 tests (5491 dice) were tested with the Stage 2 tests of the CUTs; 162 dice failed at least one of these tests. The Stage 2 tests take at least 1 minute of tester time per die since many test sets and test conditions are used. Failing die require additional tester time to log the error data.

Each die contains 5 different CUTs: two multipliers and three control logic blocks, Table 1. MUL is a 12x12 partial product multiplier with only the 12 most significant outputs observable. SQR consists of a 6x6 multiplier whose 6 most significant outputs are fed into another 6x6 multiplier, so that the second multiplier acts as a squarer. The three control logic blocks implement the same function synthesized in three different ways. STD is implemented using the standard LFT150K library [3], ELM uses only elementary gates, and ROB is a robust path-delay-fault testable implementation. More CUT details are given in the companion paper, [1].

Table 1 Circuits-under-test (CUTs)

Acronym	Description
STD	Control logic, standard gate
ELM	Control logic, elementary gate
ROB	Control logic, robust path delay fault testable
MUL	12x12 multiplier
SQR	6x6 multiplier and squarer

This paper briefly discusses the test sets applied to the CUTs and the conditions under which these tests are applied. The main focus of this paper is on test results.

2. CUT Test Sets

This section lists the test sets applied to the CUTs. Many test sets are included in an attempt to make the experiment as thorough as possible. Both university and commercial ATPG tools are used to generate the CUT tests. The commercial tools include tools from AT&T, CheckLogic, ExperTest, GenRad, IBM, Mentor Graphics, Sunrise, and Syntest; University tools include tools from U. Illinois, U. Iowa, Virginia Polytechnic Institute & State U., U. Texas and Yale U.

The CUT test sets are discussed briefly below. The length of each test set is given with the test results in Tables 3-5. For more details, refer to [4].

Design Verification Tests (Test 1.1)

Design verification vectors were manually generated by the designer to verify the functionality of MUL and SQR. There are no design verification vectors for the control circuits, as their function is not defined.

Single-Stuck-At Fault Tests (Tests 2.1-2.13)

These are conventional stuck-at tests. Many different stuck-fault tests are included. Separate tests are included for faults modeled at the I/Os of the LSI cells (pin faults), and internal faults for the complex LSI cells. Test sets that detect every fault at least 5 times (500% fault coverage) and 15 times (1500% fault coverage) are included, as well as tests with lower fault coverages

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(between 80% and 100%).

Separate test sets with lower fault coverage are included, even though we know precisely at what fault coverage the CUT failed the 100% coverage test. This was done to avoid the assumption that a 90% test set is a subset of a 100% test set. The reason is that most tools do a reverse fault simulation to compress the test set. Therefore to avoid the concern that the results might be biased by assuming the 90% test set is a subset of the 100% test set, both test sets are included.

Switch-Level Tests (Test 3.1)

This is a switch-level single-stuck-fault test set generated using the transistor-level representation of the LSI cells given in the LFT150K [3] data book.

Pseudo-random Tests (Test 4.1)

This is the pseudo-random test generated by the Parallel Data Load LFSR. It is also the exhaustive test (2^{2N} exhaustive for SQR) since the LFSR is clocked through all the possible states as described in [4]. The pseudo-random vectors are generated with the primitive polynomial $f(X) = X^{23} + X^6 + X + 1$, with alternating 1s and 0s as the initial contents of the LFSR. Single stuck fault grading was performed through the first 150K vectors.

Weighted Random Tests (Tests 5.1 and 5.2)

Two weighted random pattern generation algorithms are used. The first algorithm [5] uses equally-weighted pseudo-random vectors, followed by a single set of weights computed using ATPG. The second algorithm [6] uses initial weights and then multiple weight distributions, also based on ATPG.

Stuck-Open Tests (Test 6.1)

This test is generated for transistor stuck-open faults, where LSI Logic cells are modeled as elementary gates. Modeling these cells as elementary gates is not accurate, especially for transistor level faults in some of the complex gate. This test is included since we are not able to generate a more accurate stuck-open test set.

Transition Fault Tests (Tests 7.1 and 7.2)

Two deterministic test sets for transition faults are generated using commercial ATPG tools.

Gate Delay Tests (Tests 8.1 and 8.2)

A gate delay test is generated in which each gate is tested through the longest path (path with the greatest delay) through the gate. The gate delay test is applied twice to investigate the effect of many signals changing simultaneously in the CUT. This is done by replacing all "X's" by 0s in one test to minimize the number of transitions propagating through the circuit, and replacing "X's" with 0s and 1s randomly in the second test.

Path Delay Tests (Tests 9.1 to 9.7)

Two types of path delay tests are investigated. Path delay tests are generated for all paths that are greater than a certain fraction of the longest path in each circuit (normally called *critical* paths). An attempt is also made to generate path delay tests for every path in the CUTs. This is not possible for the multipliers, since there are too many paths. Two robust test sets are included for the control circuits. As described in the gate delay tests, some of the path delay tests are applied twice, one minimizing the number of extra transitions. Two non-robust path delay test sets are also included.

IDDQ Tests (Tests 10.1 to 10.3)

Two ATPG tools are used to generate IDDQ tests. Pseudo-random vectors of length 64 (128 for ROB) are also used. Current is measured for every vector.

CrossCheck Tests (Tests 11.1 to 11.2)

These tests are provided by CrossCheck. Note that the CrossCheck tests do not distinguish between CUT and support circuitry failures.

A modified CrossCheck test has also been generated. This test tries to distinguish between CUT failures by enabling one CUT at a time.

Signature Analysis Tests (Test 12.1)

Pseudo-random vectors were applied several times to each MUL CUT using the pseudo-random data source, and the output responses were compacted each time with a different signature register configuration [1].

Propagation Delay Measurements

This is not a CUT test, but is done as part of the Stage 2 tests. The propagation delay of the internal delay lines used to generate the 'internally-generated' clock mode is measured. This test gives some information of the variance in the overall speed across dice.

3. Test Conditions

The CUT test sets are run under the different test conditions described below. Unless otherwise specified, all tests were applied at room temperature with V_{IL}=0V, V_{IH}=4.5V, and V_{OL}=V_{OH}=1.5V.

3.1 Test Ordering

The exhaustive test is applied at the beginning and end of the test suite. This is done to verify the repeatability of the experiment.

3.2 Clocking Modes and Speed

Each test is run at several speeds as well as three different clocking modes: direct, pulse width generated, and internally generated clocking. Direct clocking, where the clock is directly controlled from ATE, are done at rated, fast (not for the RB circuits), and slow speed. Similarly, pulse width generated clocking, where the inputs to the CUTs are clocked at the rising edge of the clock pulse and outputs are sampled at the falling edge, are done at rated, fast, and slow speed. Rated speed depends on CUT delays. Fast speed is 25% faster than rated speed for the multipliers, and 5% faster than rated speed for the RB control blocks, and slow speed is two-thirds the rated speed. The speed of the internally generated clocking mode is determined by internal delay lines on the die. Exact

ATE timing can be found in [4].

The dice are tested at slow speed to study cases where test vectors were applied at slower-than-rated speed [7]. The dice are also tested at fast speed to investigate aggressive designs based on statistical timing.

3.3 Simulated Scan Vectors

Not all possible pairs of patterns can be applied using a scan chain. This is an issue for two-pattern test sets such as stuck-open and delay tests. Therefore, the effect of applying patterns through a scan chain is investigated in this experiment. This is done using the simulated scan data source described in [1].

3.4 Very-Low-Voltage

Very-Low-Voltage testing [8] in which the supply voltage is reduced below the normal operating range is investigated on the Test Chip. The idea is to provoke functional failures in weak circuits by operating the circuit at a reduced supply voltage. The input signal and supply voltage are 1.7 volts, and clocking is done at a reduced speed. The reduced clock rate was determined from the Test Chip prototypes, and is 5.6 times slower than the clock rate at 5 volts. The pulse width generated clocking mode is used for the Very-Low-Voltage tests. The long exhaustive tests are not applied at Very-Low-Voltage to conserve tester time. For Very-Low-Voltage tests, V_{IH}=1.7V, and V_{OH}=V_{OL}= 0.85V.

Test sets and test conditions are summarized in Table 2. PU, DI, IN, and VL, denote PUlse width generated clocking, DIrect clocking, INternally generated clocking, and Very-Low-Voltage, respectively. A 'Y' in a table entry means that the corresponding test set was applied under the given test conditions.

Notice that the different test speeds are not shown in Table 2; each PU and DI column under normal supply voltage in Table 2 represents three different test speeds: rated, fast, and slow. Combining all the different test conditions, each test set is repeated up to 15 times, each with a different test condition. The single stuck-at tests, for example, are applied using both the parallel load and the simulated scan data sources. Using the parallel load data source, the single stuck-at test sets were applied with normal supply voltage and pulse width generated clocking (3 speeds), direct clocking (3 speeds), or internally generated clocking (1 speed), and with Very-Low-Voltage (1 speed), for a total of 8 different test conditions. Using the simulated scan data source, the single stuck-at test sets were applied with normal supply voltage and pulse width generated clocking (3 speeds) or direct clocking (3 speeds), and with Very-Low-Voltage (1 speed), for a total of 7 different test conditions. The total number of test conditions for both parallel load and simulated scan patterns is therefore 15. Notice also that the results reported in this paper do not cover all test conditions, but only those conditions that are indicated by shaded boxes in Table 2.

In the next section, interesting CUTs are presented in more detail, with test quality evaluations for each test set. A comparison between rated and slow speed is given, particularly, comparisons between stuck-at tests applied at rated speed and delay tests applied at slow speed are presented.

4. Test Results

Four different wafer lots of the Test Chip were manufactured by LSI Logic and tested by Digital Testing Services (DTS). The total number of dice passing Stage 1 tests (gross parametric tests and test support circuitry tests) is 5491, as shown in Fig. 1. There are only 162 dice that failed some Stage 2 tests. Stage 2 yield is 5329/5491=97.04%, which is extremely high considering the thoroughness of Stage 2 tests.

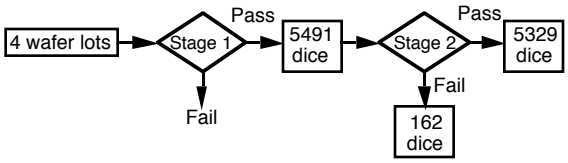

Figure 1 Test Result Statistics

The errors on the 162 dice that failed Stage 2 tests were detected by either a) sampling the output voltage at normal voltage, b) sampling the output voltage at very low supply voltage, c) sampling internal node voltages using CrossCheck circuitry, d) measuring IDDQ, or e) a combination of the above observation methods. Each of these observation methods is discussed in the following

Table 2 Test Conditions

		Data Source									
		Parallel Load				Simulated Scan			Pseudo Random		
	Supply Voltage	Normal V			VLV	Normal V		VLV	Normal V		
	Clock Mode	PU	DI	IN	EX	PU	DI	EX	PU	DI	IN
Test Set	1.1 Design Verification 2.1-13 Single Stuck-At 3.1 Switch-Level	Y	Y	Y	Y	Y	Y	Y			
	4.1 Pseudo-Random								Y	Y	Y
	5.1-2 Weighted Random	Y	Y	Y	Y	Y	Y	Y			
	6.1 Stuck-Open	Y	Y	Y	Y	Y	Y	Y			
	7.1-2 Transition Fault 8.1-2 Gate Delay Fault 9.1-7 Path Delay Fault	Y	Y	Y	Y						

Supply Voltage: Normal (5V)
VLV - Very-Low-Voltage (1.7V)

Clock Modes: PU - Pulse Width Generated Clocking
DI - Direct Clocking
IN - Internally Generated Clocking

subsections. Propagation delay measurement and stability checking [9] results are also shown at the end of this section. Signature analysis results have not yet been analyzed.

4.1 Sampling at Normal Voltage

A total of 125 dice failed with sampling errors at normal supply voltage and rated speed. Two of the 125 defective dice had more than one CUT failures: one die had defective MUL and STD CUTs, and the other die had defective ROB and STD CUTs. No defective die had more than two defective CUTs. The total number of defective CUTs is therefore 127. Of the 127 defective CUTs, there are 35 ROB, 16 ELM, 17 STD, 40 MUL, and 19 SQR CUTs. All 127 defective CUTs failed the exhaustive test, thus validating our basis of using the exhaustive test as an absolute reference.

Of the 127 CUTs that failed at rated speed, 77 CUTs failed every test set, while 50 CUTs (21 ROB, 7 ELM, 5 STD, 15 MUL, and 2 SQR) escaped some tests. For the purpose of this experiment, the CUTs that failed every test set were not interesting; our interest is in CUTs failing some, but not all, tests.

4.1.1 Test Escapes at Rated Speed

Tables 3-5 summarize the test escapes for tests applied with pulse width generated clocking at rated speed and normal supply voltage. Each failing CUT is represented by a column in the table. STD CUT #79 (shown in Table 4) is on the same die as a ROB CUT that failed every test (included in 'All' column of Table 5). MUL CUT #15 (Table 3) is on the same die as a STD CUT that failed every test. These are the only two dice that have more than one CUT failures.

An 'E' in a table cell indicates that the defective CUT in the given column escaped the test set shown in the corresponding row. For each CUT, the length of each test set is given. The last column for each CUT (All) is for those CUTs that failed every test set, hence there are no 'E' in any row. The number in parentheses indicates the number of CUTs that failed every test, e.g., there were 25 MUL CUTs that failed every test set. Test escapes are studied in the following subsections.

Table 3 Test Escapes for multiplier circuits

	Test Set	MUL																SQR			
		Test	CUT#														All	Test	CUT#		All
		Len	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	(25)	Len	41	42	(17)
1.1	Design Verification	57		E		E				E	E	E	E	E					90			
2.1	SSF Tool 1 (100%, gate faults)	62		E	E	E			E										34			
2.2	SSF Tool 2 (100%, gate faults)	163	E		E														74			
2.3	SSF Tool 2 (100%, pin faults)	61	E	E															34			
2.4	SSF Tool 3 (100%, pin faults)	21	E	E		E					E	E	E						22	E		
2.6	SSF Tool 4 (100%, gate faults)	68																	39			
2.7	SSF Tool 4 (99.0%)	78		E															38			
2.8	SSF Tool 4 (98.0%)	69	E	E															39			
2.9	SSF Tool 4 (95.0%)	62	E				E	E	E										39			
2.10	SSF Tool 4 (90.0%)	63	E	E	E		E	E	E	E					E				35			
2.11	SSF Tool 4 (80.0%)	49	E	E	E	E	E	E	E	E						E	E		20		E	
2.12	SSF Tool 4 -- Min 5 Det/Fault	258																	168			
2.13	SSF Tool 4 -- Min 15 Det/Fault	754																	473			
3.1	Switch-level ATPG	110																	56			
4.1	Pseudo-Random/Exhaustive	2^{24}																	4096			
	N^2 Exhaustive	–	–	–	–		–		–	–	–	–	–	–	–	–	–		2^{24}			
5.1	Weighted Random - (WR-MUR)	23332																	417			
5.2	Weighted Random - (WR-WAI)	12341																	372			
6.1	Stuck-Open ATPG (equiv gate)	269		E															153			
7.1	Transition Fault, ATPG Tool 5	84		E	E														68			
7.2	Transition Fault, ATPG Tool 6	434																	304			
8.1	Gate Delay Fault -- X→0	-	–	–	–		–		–	–	–	–	–	–	–	–	–		976			
8.2	Gate Delay Fault -- X→ran	-	–	–	–		–		–	–	–	–	–	–	–	–	–		976			
9.1	Path Delay -- Crit Path - X→0	620	E	E	E		E	E											1692			
9.2	Path Delay -- Crit Path - X→ran	620	E	E	E		E	E											1692			
11.1	CrossCheck	3556	E				E												3556			

* X→0 means that X is replaced by 0; X→ran means that X is replaced randomly with 0 or 1.
E indicates that the CUT escaped the correponding test at both rated and slow speed
- indicates that the correponding test was not applied for the given CUT

Table 4 Test Escapes for ELM and STD circuits

	Test Set	E L M									S T D						
		Test Len	C 60	U 61	T 62	# 63	64	65	66	All (9)	Test Len	C 76	U 77	T 78	# 79	80	All (12)
2.1	SSF Tool 1 (100%, gate faults)	79				E					68				S		
2.2	SSF Tool 2 (100%, gate faults)	144				S					129	E			S		
2.3	SSF Tool 2 (100%, pin faults)	144				S					129	E			S		
2.4	SSF Tool 3 (100%, pin faults)	82				S					69				E		
2.5	SSF Tool 3 (100%, compressed)	66				E					62				S		
2.6	SSF Tool 4 (100%, gate faults)	93				S					72				S		
2.7	SSF Tool 4 (99.0%)	91	E			S					71				S		
2.8	SSF Tool 4 (98.0%)	87		E		S					80				S		
2.9	SSF Tool 4 (95.0%)	74	E			S					73	E			S		
2.10	SSF Tool 4 (90.0%)	72	E	E	E	S					67				S		
2.11	SSF Tool 4 (80.0%)	58	E	E	E	S					48				S	E	
2.12	SSF Tool 4 -- Min 5 Det/Fault	397				S					339				S		
2.13	SSF Tool 4 -- Min 15 Det/Fault	1163				S					1046				S		
3.1	Switch-level ATPG	109				S					108				S		
4.1	Pseudo-Random/Exhaustive	2^{24}				S					2^{24}						
5.1	Weighted Random - (WR-MUR)	1438				S					3404				S		
5.2	Weighted Random - (WR-WAI)	738				S					634				S		
6.1	Stuck-Open ATPG (equiv gate)	219				S					203				S		
7.1	Transition Fault, ATPG Tool 5	256				S					222				S		
7.2	Transition Fault, ATPG Tool 6	292		E		S					274				S		
8.1	Gate Delay Fault -- X→0	304	E	E	E	E					312	E			S		
8.2	Gate Delay Fault -- X→ran	304	E	E		S					312	E			S		
9.1	Path Delay -- Crit Path - X→0	408	E	E		E	E	E	E		992	E	E	E	S		
9.2	Path Delay -- Crit Path - X→ran	408	E		E	E	E				992	E	E	E	S		
9.3	Path Delay -- Robust - X→0	2864				S					2864				S		
9.4	Path Delay -- Robust - X→ran	2864				S					2864				S		
9.5	Path Delay -- Robust Test	3044				S					3044						
9.6	Path Delay -- Non-Robust-A	542	E			S					562				S		
9.7	Path Delay -- Non-Robust-B	2156				S					2164						
11.1	CrossCheck	3556									3556						

* X→0 means that X is replaced by 0; X→ran means that X is replaced randomly with 0 or 1.
E indicates that the CUT escaped the correponding test at both rated and slow speed
S indicates that the CUT escaped the correponding test at slow speed only

4.1.1.1 Design Verification Vectors

Design verification vectors were poor in detecting defective MUL CUTs. Seven of the 15 interesting defective MUL CUTs (46.7%) were not detected by design verification vectors. The high escape rate for design verification tests was expected, since these tests are not targeting manufacturing defects.

4.1.1.2 Single Stuck-At Tests

A single stuck-at test set with low coverage is not necessarily a subset of a single stuck-at test set with higher coverage. This is why in some cases (such as ROB CUT# 94 in Table 5) lower coverage test sets (90% and 95%) detected a defective CUT that higher coverage test sets (100%, 99%, and 98%) missed. Table 6 shows the relationship between test escapes and single stuck-at fault coverage for tests generated using a single stuck-at fault ATPG (tests 2.6-2.13 in Table 3-5). The corresponding defect level (DL), measured in *defects-per-million* (DPM), is calculated by assuming that the test escapes are shipped with 5329 'good' dice; i.e.,

$$\text{Defect Level} = \frac{\text{test escapes}}{\text{parts shipped}} = \frac{\text{test escapes}}{5329 + \text{test escapes}} \times 10^6 \text{ DPM} \quad (4.1)$$

Equation 4.1 is valid if and only if there are no dice with more than one CUT that escaped the same test; i.e., the total number of CUT test escapes is the total number of die escapes for each test. Since there are two dice that failed two CUTs, and on each of these two dice, one of the two failing CUTs failed every test set, each CUT test escape is equivalent to a die test escape.

The number of gates and the total number of CUT failures for each CUT are also shown in Table 6. Notice that the number of CUT failures generally increases with the size of the CUT. However, there is no direct relationship between the number of test escapes and the size of the CUT. For example, although SQR is larger

and has fewer inputs and outputs than ELM, there are fewer SQR test escapes.

Table 5 Test Escapes for ROB circuit

	Test Set	Test Len	ROB #																						All
			93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	(14)
2.1	SSF Tool 1 (100%, gate faults)	244	E	E					E															
2.2	SSF Tool 2 (100%, gate faults)	490	E																					
2.3	SSF Tool 2 (100%, pin faults)	489	E			S																		
2.4	SSF Tool 3 (100%, pin faults)	262	E																					
2.5	SSF Tool 3 (100%, compressed)	234	E									E												
2.6	SSF Tool 4 (100%, gate faults)	275	E	E	E				E															
2.7	SSF Tool 4 (99.0%)	254	S	E							E													
2.8	SSF Tool 4 (98.0%)	245	E	E	E																			
2.9	SSF Tool 4 (95.0%)	219	E				E		E				E											
2.10	SSF Tool 4 (90.0%)	190	E		E	E	E																	
2.11	SSF Tool 4 (80.0%)	159	E	E		E	E	E	E	E														
2.12	SSF Tool 4 -- Min 5 Det/Fault	1235	E																					
2.13	SSF Tool 4 -- Min 15 Det/Fault	3745	S																					
3.1	Switch-level ATPG	327	E	E	E	E	E	E		E				E										
4.1	Pseudo-Random/Exhaustive	2^{24}	S																					
5.1	Weighted Random - (WR-MUR)	34330	S	E																				
5.2	Weighted Random - (WR-WAI)	7807	S																					
6.1	Stuck-Open ATPG (equiv gate)	766	E																					
7.1	Transition Fault, ATPG Tool 5	796	E																					
7.2	Transition Fault, ATPG Tool 6	586	E	E	E	E				E						E								
8.1	Gate Delay Fault -- X→0	612	E	E	E	S	E	E					E	E	E	E	E							
8.2	Gate Delay Fault -- X→ran	612	E	E											E	E	E							
9.1	Path Delay -- Crit Path - X→0	400	E	E	E	E	E	E	E	E	E	E	E	E	E	E		E	E	E	E	E		
9.2	Path Delay -- Crit Path - X→ran	400	E	E	E	E	E	E	E	E	E			E	E		E	E					E	
9.3	Path Delay -- Robust - X→0	7,068	E																					
9.4	Path Delay -- Robust - X→ran	7,068	E	E																				
9.5	Path Delay -- Robust Test	7,092	E																					
9.6	Path Delay -- Non-Robust-A	884	S	E	E	E	E								E									
9.7	Path Delay -- Non-Robust-B	4,136	S	E																				
11.1	CrossCheck	3,556						E																

* X→0 means that X is replaced by 0; X→ran means that X is replaced randomly with 0 or 1.
E indicates that the CUT escaped the correponding test at both rated and slow speed
S indicates that the CUT escaped the correponding test at slow speed only

Table 6 Test escapes vs. single stuck-at fault coverage

Test Set	Fault Cov.	Test escapes STD	ELM	ROB	MUL	SQR	Total	DL (DPM)
2.11	80%	1	3	7	10	1	22	4036
2.10	90%	0	3	4	8	0	15	2807
2.9	95%	1	1	4	4	0	10	1873
2.8	98%	0	1	3	2	0	6	1125
2.7	99%	0	1	2	1	0	4	750
2.6	100%	0	0	4	0	0	4	750
2.12	500%	0	0	1	0	0	1	188
2.13	1500%	0	0	0	0	0	0	0
Tot. #	Defect	17	16	35	40	19	127	
	Gates	1520	1192	3592	4584	1784	12672	

Notice that the number of test escapes decreases in general with increasing fault coverage, which translates to lower defect level and better quality. A single stuck-at test with 100% coverage did not detect all defective CUTs; there were a total of 3 CUT escapes. However, test sets in which each fault is detected multiple times (2.12 and 2.13) provide quality levels comparable to an exhaustive test, although the number of test patterns is significantly fewer than an exhaustive test.

4.1.1.3 Pseudo-random test

The pseudo-random test set is an exhaustive test whose patterns were generated by a 24 bit LFSR in the data source. By recording the vector number of the first failing vector in the exhaustive pseudo-random test set for each die, we can deduce the number of failing dice that would be detected after running a pseudo-random test of any arbitrary length.

Most of the CUTs failed within the first few hundred vectors. There were only 9 defective CUTs that escaped after 1,000 vectors, 4 defective CUTs that escaped after 5,000 vectors, and only 2 defective CUTs that escaped after 10,000 vectors. Table 7 lists the defective CUTs that escaped the pseudo-random test for test lengths greater than

50 vectors. The CUT numbers in Table 7 corresponds to the CUT numbers in Tables 3-5. For each test length *N*, the CUTs that escaped are those listed in rows with test lengths greater or equal to *N*. For example, for test length of 5,000, the CUTs that escaped are ROB CUT #94, #96, and MUL CUT #3, and #5. Notice that SQR is not listed in Table 7, since all SQR were detected in the first 50 pseudo-random vectors.

Table 7 Pseudo-random test escapes

Test Len	SSF cov	Test esc	DL (DPM)	Escaped CUT #			
				STD	ELM	ROB	MUL
150K	99.7	0	0				
50K	99.4	1	188			96	
8K	98.2	2	375			94	
5K	97.9	4	750				3,5
4K	96.9	5	937			97	
2K	95.1	7	1312				1,14
1K	93.1	9	1686	76		104	
800	91.6	11	2060			99	6
500	89.6	15	2807		60	105	7,15
300	87.5	18	3366	79		107	2
200	85.5	20	3739			111	11
150	83.8	23	4297		61	100 106	
100	80.7	26	4855		62	101 108	
70	78.8	29	5412		64	95,98	
50	73.4	36	6710		65, 66	93, 102, 109	8,10

4.1.1.4 Weighted random tests

There were no test escapes for weighted random test 5.2. Only one defective CUT (ROB CUT# 94) escaped the weighted random test 5.1. Interestingly, this CUT passed test 5.1 and failed 5.2, even though test 5.1 is more than 4 times longer than test 5.2 for ROB.

Weighted random test escapes for MUL and ROB are compared with pseudo-random tests in Table 8. In general, the number of test escapes for pseudo-random and weighted random tests are comparable for short test lengths (~100 vectors). For longer tests, weighted-random test 5.2 detected the failing dice with a test length shorter than the pseudo-random test, while weighted-random test 5.1 needed more vectors than the pseudo-random test to detect all failing MULs. The main difference between the two weighted-random test sets is that test 5.1 uses a single weight distribution after some equally weighted pseudo-random patterns, while test 5.2 uses multiple weight distributions (6 weights for MUL, and 7 weights for ROB).

4.1.1.5 Stuck-open and Transition Fault Tests

Although the stuck-open test was generated using an inaccurate elementary gate model, there were only two test escapes (MUL CUT# 2 and ROB CUT# 93).

CUTs that escaped the stuck-open test also escaped transition fault test 7.1. Transition fault test 7.1 had one more CUT escape (MUL CUT# 3). The number of ROB escapes for transition fault test 7.2 is fairly high (6 escapes), but there were no multiplier escapes for transition fault test 7.2.

Table 8 Weighted-random test escapes

(a) ROB

Test Length	Test escapes PR (4.1)	Test escapes WR (5.1)	Escaped CUTs (5.1)	Test esc WR (5.2)	Escaped CUTs (5.2)
34330	2	1	94	0	-
5000	2	2	96	1	100
4000	3	3	97	2	93
3000	3	3	-	5	94,96, 97
1000	4	4	104	6	95
500	6	7	93, 99, 105	7	105
200	8	9	107, 111	10	101, 104, 106
100	12	12	100, 106, 108	12	99, 107

(b) MUL

Test Length	Test escapes PR (4.1)	Test escapes WR (5.1)	Escaped CUT (5.1)	Test esc WR (5.2)	Escaped CUT (5.2)
20000	0	0	-	0	-
19000	0	1	5	0	-
8000	0	2	3	0	-
6000	2	2	-	1	3
4000	2	3	1	1	-
2000	4	4	14	4	1, 5, 6
1000	4	4	-	4	-
500	7	7	6, 7, 15	4	-
200	8	8	2, 11	6	2,15
100	8	8	-	6	-

4.1.2 Test Escapes at Slow Speed

The CUTs were tested at two-third the rated speed. There were no CUTs that passed at rated speed and failed slow speed, therefore, each 'E' in Tables 3-5 also indicates that the given CUT escaped the corresponding test at slow speed. On the other hand, there are some defective CUTs that failed some tests at rated speed, while the same tests passed at slow speed. These slow speed escapes are denoted with 'S' in Tables 3-5.

Two CUTs that failed at rated speed escaped all tests at slow speed. These are ROB CUT# 93 and ELM CUT# 63. Furthermore, two CUTs failed more test sets at rated speed than slow speed. Failure on ROB CUT# 96 was not detected by test sets 2.3 and 8.1 at slow speed, but it is detected by those two tests at rated speed. Failure on STD CUT# 79 was detected only by tests 4.1, 9.5, and 9.7 at slow speed.

These 4 dice (ROB CUT# 93, 96, ELM CUT# 63, and STD CUT# 79) failed fewer tests at slower speed. Therefore, these are speed dependent failures.

4.1.3 At-speed tests vs. Delay tests

Comparisons between a delay test and a single stuck-at

test set with 100% fault coverage applied at rated speed (commonly known as at-speed tests) were not conclusive. Comparing the robust delay test set 9.4 with the single stuck-at test set 2.6 applied at-speed, the robust delay test detected all ROB CUTs that were detected with the at-speed test, as well as two ROB CUTs that were not detected by the at-speed test (ROB CUT# 95 and #99). However, the single stuck-at test 2.2 applied at speed detects all ROB CUTs that were detected by delay test 9.4, as well as a ROB CUT that was not detected by the delay test (ROB CUT# 94).

Notice that the path delay fault test sets that were generated only for critical paths (Tests 9.1 and 9.2) have many test escapes. The critical path delays were calculated using pre-layout delay values, since post-layout delays were not available when these test sets were generated.

4.2 Very-Low-Voltage Tests

The results of Very-Low-Voltage tests are summarized in Table 9. Most CUTs that failed normal voltage tests failed Very-Low-Voltage tests as well. However, there were 13 CUTs (in 13 different dice) that failed at Very-Low-Voltage only (6 MUL, 5 SQR, and 2 ROB). These CUTs are not shown in Tables 3-5.

Table 9 Normal Voltage vs. Very-Low-Voltage Tests

		Normal Voltage: Pass	Normal Voltage: Fail
Very Low Voltage	Pass	5353 dice	5 dice
	Fail	13 dice	120 dice

There are five cases of Very-Low-Voltage test escapes: MUL CUT# 11, ELM CUT# 67 (not shown in Table 4), and ROB CUT# 94, 98, and 101. The CUTs were not tested with exhaustive patterns under Very-Low-Voltage conditions because of tester time limitations. Ten CUTs failed more tests at Very-Low-Voltage than normal voltage (MUL CUT# 1, 2, 4, SQR CUT# 42, SIM CUT# 62, STD CUT #79, ROB CUT# 93, 99, 102, and 103), and 3 CUTs failed more tests at normal voltage than at Very-Low-Voltage (MUL CUT# 9, 16, and STD CUT# 76). Notice that MUL CUT# 16 shown in Table 12 was not explicitly listed in Table 3, since it failed all tests at normal voltage and rated speed. It was implicitly included in the column with 25 dice listed as 'All', indicating that every test detected a failure in those CUTs.

In summary, more tests and CUTs failed at Very-Low-Voltage than at normal voltage, especially for speed dependent failures such as ROB CUT# 93 (failed some normal voltage tests at rated speed and escaped all tests at slow speed). Several CUTs failed at Very-Low-Voltage only. These failures may be weak parts that cause infant mortalities [8]. Further experiments such as failure analysis or burn-in are needed to reveal whether these Very-Low-Voltage failures have a higher probability of subsequent functional failure.

4.3 CrossCheck Tests

The results of CrossCheck tests are summarized in Table 10. There were 3 CUTs (each in a different die) that escaped CrossCheck tests: MUL CUT# 1 and 3, and ROB CUT# 98. Failures on these 3 CUTs were found to be speed dependent; more vectors failed in the pseudo-random test at higher speeds for each case.

Notice that CrossCheck tests were performed with V_{SST} (test ground) tied to ground. Tying V_{SST} to a voltage source below ground (–1V) could yield better coverage, however, this setup was not possible for our experiment.

Table 10 Normal Voltage Sampling Tests vs. CrossCheck Tests

		Normal Voltage: Pass	Normal Voltage: Fail
CrossCheck Tests	Pass	5366 dice	3 dice
	Fail	0 die	122 dice

4.4 IDDQ Measurements

During Stage 1 tests (gross parametric and test support circuitry tests), IDDQ measurements were made, and parts with high IDDQ were not part of the experiment. All inputs to the CUTs were held at 0 during these measurements, and the threshold current was set to 500μA for test support circuitry tests. The IDDQ measurements made during Stage 2 tests target specific CUTs: input vectors were either generated by an ATPG tool or pseudo-random vectors were used.

Each IDDQ measurement is recorded during Stage 2 IDDQ tests. The range of IDDQ currents in runs up to 33.3mA, however, the maximum IDDQ currents of most CUTs fall between 30μA and 110μA, with almost 3,000 die with a maximum current of 40μA.

Setting an IDDQ threshold of 200μA, 36 defective CUTs escaped all IDDQ tests (10 MUL, 3 SQR, 6 STD, 4 ELM, and 13 ROB); 15 dice failed some IDDQ tests and passed all normal voltage sampling tests.

The number of defective MUL CUTs that were detected at any given IDDQ test length is shown in Figure 3. Although both ATPG tools used the pseudo stuck-at model to generate test patterns, ATPG Tool 1 was much more efficient in terms of test length and number of rejects. ATPG Tool 2 needed more vectors than the pseudo-random test to detect the defective MULs. Notice that none of the three test sets were able to detect all 40 defective MULs. Similar results were found in other CUTs.

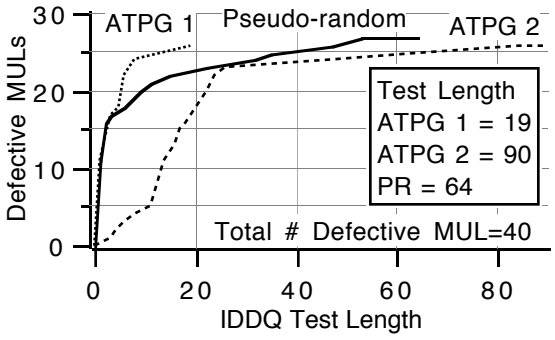

Figure 3 IDDQ Rejects vs. Test Length for MUL

4.5 Propagation Delay Measurements and Stability Checking

Due to the limited space, we will present stability checking and delay measurement results for MUL CUT only. There were 21 MUL CUTs that failed stability checking. Of these 21 MUL CUT failures, 3 failed sampling tests at Very-Low-Voltage only. Although most CUTs failed every test at all speeds, 16 MUL CUTs failed more vectors in the pseudo-random test at higher speeds, hence the failure behavior of these CUTs are also speed dependent.

Figure 4 shows the distribution of propagation delay measurements for all MULs. The number above each column indicate the number of MULs that failed stability checking. Stability checking failures spread across dice with various propagation delays, indicating that stability checkers detected localized delay defects.

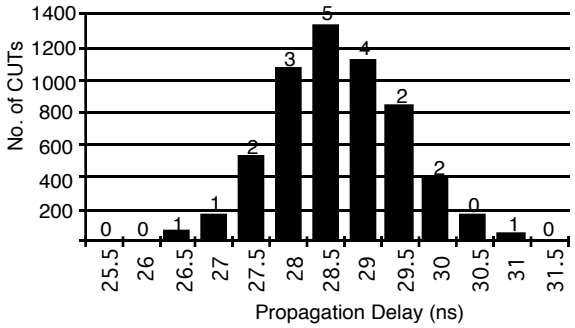

Figure 4 Propagation Delays for MUL

5. Summary

This paper reports some results on a Test Chip that was designed to compare many test methodologies under various test conditions. The amount of data processed for each failing die is large; due to space limitations, we could only report a few important results here.

Single stuck-at tests with 100% fault coverage may not be adequate to detect all defective dice. An interesting result is that a single stuck-at test set with each stuck-at fault detected more than once may yield higher quality. This result shows that even though the single stuck-at model may be inaccurate to model real defects, a sufficiently high (can be over 100%) single stuck-at fault coverage may be adequate to achieve high quality levels.

Four speed dependent CUTs were found. These failures indicate the need for AC tests, either applying delay tests or boolean tests at-speed.

Weighted-random tests were more effective in reducing the test lengths when multiple weights are used. Random patterns (both unweighted and weighted) were effective in detecting all bad CUTs.

There were more Very-Low-Voltage failures than normal voltage failures, although a few CUTs that failed at normal voltage escaped at Very-Low-Voltage. Very-Low-Voltage only failures may be weak parts that may fail at normal voltages early in the device's lifetime. Further experiments are needed to see whether these failures are actually infant mortalities.

IDDQ tests cannot detect all defective dice, they must be used in conjunction with voltage tests. The efficiency of IDDQ tests varies from one ATPG tool to another, even when the same fault model is used to generate the IDDQ test vectors.

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