SCAN SYNTHESIS FOR ONE-HOT SIGNALS

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1. Introduction

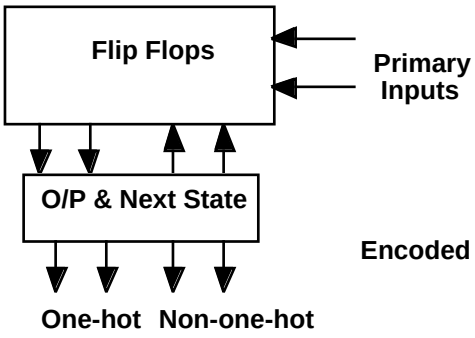
Among the different design for testability (DFT) techniques available today, scan path based methods [Williams 83] are probably the most basic and most widely used. In a scan-path based design, the circuit has two operating modes; the normal functional mode and test mode during which the circuit bistables are interconnected into a shift register. Thus, in the test mode, it is possible to shift an arbitrary test pattern into the bistables. By returning the circuit to normal mode for one clock period, the outputs of the combinational circuitry are stored in the bistables. If the circuit is then placed into test mode, it is possible to shift out the contents of the bistables and compare these contents with the correct response [McCluskey 86]. Thus, a sequential circuit is transformed into a combinational one during testing thereby making test generation simpler.

Many circuits contain logic that is controlled by mutually exclusive (one-out-of-*n*) input signals. A typical example is an *n*-to-*1* multiplexer implemented with *n* transmission gates, each controlled (enabled) by a mutually exclusive control signal. Unfortunately, the presence of such circuits poses a problem in scan-based or BIST designs. At any point during the scan process, the bistables may contain a state that is invalid during functional operation, resulting in non-mutually exclusive values on the control signals. This can result in abnormal (unpredictable) behavior of the entire circuit. In designs containing tristate buses, the presence of non-mutually exclusive values in the tristate control inputs may cause damage to the circuit. The goal of our synthesis technique is to generate designs that are safe for scan and BIST operations in the presence of mutually exclusive signals. In general, our technique generates designs with less area than the conventional technique of synthesizing such designs without taking in account safety during scan or BIST operations.

Different approaches have been proposed for handling one-hot latches (latches that are supposed to contain mutually exclusive values) in a scan path based design. The simplest is to remove such latches from the scan path thereby resulting in a partial-scan design [Cheng 90][Lee 90][Abramovici 91]. Another approach gates the output of the mutually exclusive latches during scanning, resulting in a particular set of mutually exclusive values enforced on the latch outputs irrespective of its contents. Another way of circumventing this problem is to remove these system latches from the scan chain and use a set of shadow latches for scanning. Values are scanned into the shadow latches during scan-in and are parallel loaded into system latches. During scan-out the reverse process is followed. However, this approach does not help when random patterns are loaded into the system latches during testing. The L3 latch based LSSD technique presented in [Das Gupta 81] can also be used to take care of the one-hot latch problem. The L3 latch is used to break the path from an LSSD to a non-LSSD network so that the non-LSSD does not interfere with the testing of the LSSD logic. With an L3 latch based scheme, first the desired pattern is scanned into the latches. Next, the pattern is loaded into the L3 latches by applying a P-clock pulse. Thus, the non-LSSD logic sees the final scanned-in value (a valid state) and not the intermediate values (invalid states). An encoder/decoder based scheme for solving this problem was presented in [Pateras 95]. We consider a more general problem, where any set of signal lines (not necessarily the latch outputs) can contain mutually exclusive values. Thus, we target a more general class of circuits. Our aim is to synthesize these circuits such that mutually exclusive values are maintained regardless of the state of the bistables.

2. Our proposed synthesis technique

The general model of the circuit we are considering is shown in Fig 1. We assume that any set of signal lines derived from the output and next state logic can contain mutually exclusive values.



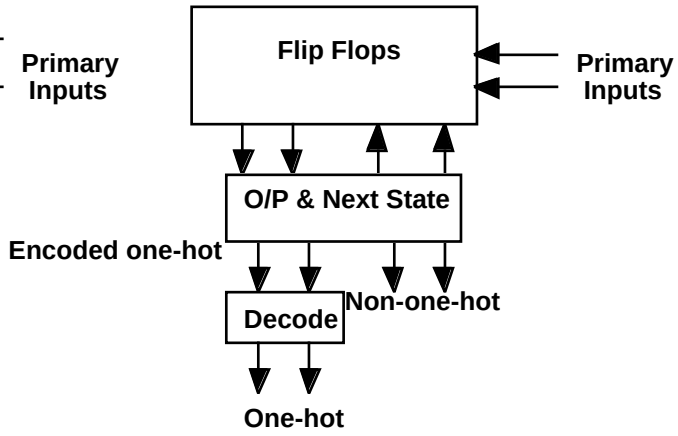


Figure 1 : General Structure of FSM **Figure 2** : Modified FSM to ensure 1-hots

With reference to Figure 1, it is easy to see that the one-hot output condition may be violated due to the presence of a faults or don't cares in the output and the next state logic. The most straightforward way to guarantee the one-hot condition of the outputs regardless of the contents of the flip-flops or faults in the output logic is to insert encoding logic on the outputs that are guaranteed to be one-hot,. The logic has *n* inputs corresponding to the *n* one-hot signals and produces *n* one-hot outputs.

Table 1 Part of FSM-1

Present State	Output
state 0	1000 000
state 1	0100 001
state 2	0010 010
state 3	0001 011

Table 2 : FSM-1 with encoded one-hots

Present State	Output
state 0	00 000
state 1	01 001
state 2	10 010
state 3	11 011

Table 3 : 2 to 4 Decoder

Input	Output
00	1000
01	0100
10	0010
11	0001

This encoding logic is placed between the logic generating the one-hot signals and the logic having the one-hot signals as their inputs. A typical example of such an encoder is a *priority encoder* which produces a *'1'* on output *i* and *'0'* on remaining outputs if all inputs *1.. i-1* are *'0'*, input *i* is *'1'* and the remaining inputs are *don't cares*. Thus, the priority encoder ensures that, as long as it is fault-free, there is no chance of its outputs being non-mutually exclusive. We are currently experimenting with the minimum area implementation of such an encoder. The greatest advantage of such a scheme is that it is independent of any assumption about the general structure of the circuit that produces one-hot signals.

We explain our approach to solving this problem with the help of an example. Let us consider the specification for FSM-1 (Table 1). It has 4 states and 7 outputs. The first 4 of the 7 outputs are mutually exclusive (one-hot). This information is passed on to the FSM synthesis procedure. Our technique is to alter the synthesis scheme so that the outputs that are supposed to be one-hot are fully encoded. Next, the encoded outputs are fed into an area-efficient decoder that generates one-hot outputs (Fig 2).

As shown in Table 2, the first four outputs of FSM-1 are encoded using two bits. For example, in the first transition, the first of the one-hot outputs is supposed to be 1 as per Table 1 (FSM-1). Hence, the current encoded output is 00. The truth table for the output decoder is shown in Table 3. Under fault-free conditions, the decoder produces mutually exclusive values on its outputs. The above example is a specific case when the number of mutually exclusive signals is a power of 2. When the number of one-hot signals is not a power of 2, we can still apply our synthesis scheme with minor modifications to the decoder specification. Suppose we have *m* mutually exclusive signals which have been encoded using $n = \lceil \log_2 m \rceil$. Not all the 2^n combinations will appear on the output of the FSM. Hence, while specifying the decoder, we map the unused combinations to particular decoded values with an aim to reduce the size of the decoder.

3. Experimental Results

In this section, we present a set of preliminary experimental results. We added 8, 12, 16 and 20 one-hot outputs to several of the MCNC Logic Synthesis FSM benchmark circuits. We synthesized the FSMs

using the one-hot encoding option in *sis*. Next, we used our scheme to encode the one-hot outputs, synthesize the FSM with encoded outputs and feed the encoded outputs to a decoder to generate the one-hot signals. We compared the area requirement of our scheme to that of the general scheme of synthesizing FSMs with one-hot outputs without taking special care to handle the one-hot outputs during scan. Table 4 shows the experimental results on some of the MCNC FSM benchmark circuits. Note that our synthesis scheme not only ensures a safe scan operation, it also results in the lowest area implementations. The area results correspond to gate areas obtained after performing technology mapping using LSI logic g10p library.

Table 4: Preliminary area results after inserting special techniques to handle one-hot signals.

FSM Name	8 1-hot outputs added			12 1-hot outputs added			16 1-hot outputs added		
	Area [1]	Area [2]	%-age reduction	Area [1]	Area [2]	%-age reduction	Area [1]	Area [2]	% -age reduction
bbara	839	557	34 %	592	617	- 4 %	953	745	21 %
bbtas	195	147	25 %	215	214	0.4 %	229	222	3 %
beecount	476	360	24 %	532	409	23 %	529	419	20 %
dk14	920	897	3 %	881	874	0.7 %	931	1014	- 8 %
dk16	2481	1026	58 %	2626	1189	54 %	1556	1259	19 %
ex6	935	714	24 %	843	730	13 %	833	700	15 %
pma	924	708	23 %	924	740	19 %	924	768	16 %

1. Conventional synthesis : one-hot requirement is not guaranteed during scan.

2. Our synthesis technique : one-hot requirement is guaranteed during scan.

4. Conclusions

In this abstract we have addressed a critical problem of synthesizing scan based designs containing logic that is controlled by mutually exclusive (one-out-of-n) input signals. While our prime motivation is to ensure safe scan and BIST operations, we have the added advantage that our technique generates lower area designs as compared to techniques that do not consider the safe scan/BIST issue. We are currently working on improving the area results of our synthesis technique, evaluating the fault coverage of the resulting circuit, and incorporating our technique into **TOPS**, the Stanford CRC synthesis-for-test tool. We are also investigating new techniques that allow specification of mutually exclusive signals in the FSM description.

5. References

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