Delay Testing of Data Paths with Scan

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Extended Abstract

We are investigating the use of orthogonal scan paths to facilitate delay testing for data paths. Recent research, such as that done at the Center for Reliable Computing at Stanford, indicates that delay testing should be performed to assure high quality parts. Testing for a delay fault generally requires a two-pattern test. The first pattern sensitizes a path in the logic and the second pattern stimulates any delay fault. Because of the dependencies between flip-flops, applying two-pattern tests to sequential logic is more complicated than applying the single pattern tests necessary for detecting single-stuck faults, even if a full scan path is present. An appropriately configured orthogonal scan path [Avra 92] [Bhattacharya 96] [Norwood 96], in which the scan path flow follows the data path flow, may simplify the application of two-pattern tests for data paths.

Current methods for applying two-pattern tests with a traditional scan path, where the scan path flow is perpendicular to the data path flow, generally fall into four approaches.

1) Modification of the scan elements to prevent the flip-flop outputs from toggling during scan. This approach is often called enhanced scan. Any two-pattern test can be applied, but the area overhead can be large since the modification typically requires the addition of a latch to each flip-flop.
2) The flip-flops can be partitioned so that for any particular two-pattern test, adjacent flip-flops, i.e., flip-flops next to each other, in the scan path are not both required to apply the needed patterns. In this way, the first pattern can be scanned into the active

flip-flops, and the second pattern can be scanned into the previous, inactive, flip-flops. Once the first pattern has sensitized the logic, the second pattern is applied with a single scan clock. This method allows for the application of arbitrary two-pattern tests, but a partitioning of the flip-flops may not be possible and the interconnect overhead can be high. [Hurst 95] has examined this approach for multiple finite state machines.

3) The first pattern is scanned into the scan path to sensitize the logic. This vector is selected such that the second pattern can be obtained from the output of the combinational logic after one system clock. This method makes the ATPG more complicated and restricts the set of two-pattern tests that can be applied.
4) The first pattern is scanned into the scan path to sensitize the logic. The second pattern is obtained by shifting the scan path one bit. In other words, the second pattern is just a shifted version of the first pattern [Savir 92]. This greatly restricts the set of two-pattern tests that can be applied.

Using orthogonal scan, the basic idea of the second approach can be applied to data paths. The registers can be partitioned into sets, such that each set of registers can be used independently of the other sets to apply vectors to a subset of the data path logic. The different sets can be interleaved in the orthogonal scan path so that no two registers from the same set are adjacent. In this way, one set of registers can be loaded with the first pattern, and the second pattern can be loaded into the preceding registers, which belong to different sets. Each part of the data path can then be delay tested during different test sessions. Any two-pattern test can be applied in this manner.

There are quite a few issues to be resolved. What types of delay faults can be detected? How should the registers be partitioned? Can functional logic and test logic be shared? What is the area overhead to achieve the delay fault testability? Can high-level knowledge be exploited during synthesis to achieve better results? These are some of the questions that are being addressed.

References

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