Techniques to Identify the Potential Cause of Overkill

Center for Reliable Computing
Stanford University
December 2004
Task ID: 1175.001
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Abstract

Chips that produce correct results under operating conditions (*good chips*) may fail structural tests applied via scan chains (also called *overkill chip*). In a *System Level Test (SLT),* a chip is inserted in an actual system and tested whether it produces correct outputs in a system. We applied various structural tests as well as SLT to test chips fabricated with 0.14μm and 0.13μm technology, and identified potential overkills. Based on the structural and system level test results, we classified the test chips into two categories: chips that fail structural tests but pass system level test (also called *FP devices*) and chips that fail both structural tests and system level test (also called *FF devices*). We observed that FP and FF devices fail at different scan cells and logic design blocks. We investigated if there are design problems that cause FP devices to fail at the same logic design blocks or the same scan cells. We have not found any experimental evidence of such design problems yet.

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1 Introduction

Chips that produce correct results under operating conditions (*good chips*) may fail structural tests applied via scan chains (also called *overkill chip*). There are three main sources of overkill: (1) multi-cycle path and (2) long false path (3) excessive switching activities.

1. *A multi-cycle path* is a path that requires two or more clock cycles to propagate a response and to capture the response at the scan chain flip-flops [Saxena 02]. During normal operations, it is guaranteed by design that the contents of the destination flip-flops of multi-cycle paths are sampled only at appropriate times. However, in the test mode, the destination flip-flops of multi-cycle paths may be sampled at incorrect times. Therefore, the multi-cycle paths may cause overkill.
2. *A false path* is a path that cannot be sensitized during normal operation. A path that can be sensitized during normal operation is called a *valid path*. A false path whose delay is greater than the system clock period is called a *long false path*. In scan-based transition fault testing, some test patterns could sensitize the long false paths and transitions propagated along the long false paths are not guaranteed to settle down to the logic values expected from fault-free simulation because the test is applied with the system clock whose period is smaller than the delay of long false paths [Kim 03]. Therefore, long false paths may cause overkill.
3. In many cases, power consumption during the test mode is higher than during functional operation [Saxena 01]. In addition, switching activity of test pattern could affect their defect detection capability [Millman 88] [Saxena 03]. Therefore, a good chip could fail the structural test depending on the switching activity. Hence, the optimum switching activity of structural test patterns should be determined to minimize overkill.

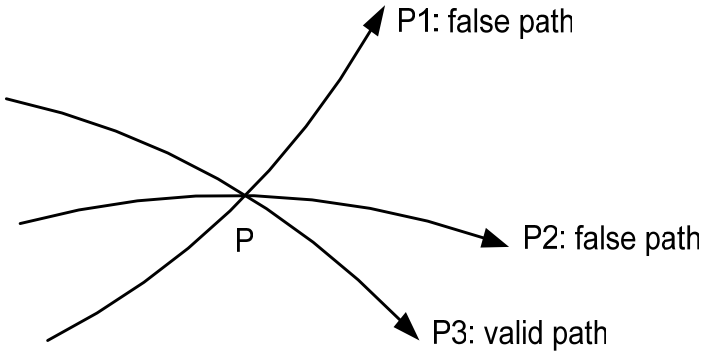

Figure 1 Long false path

Table 1 Delay of paths – example

Path		Delay (ns)	
		Defect-free circuit	2ns of delay defect at node P
Case 1	P1	9	11
	P2	6	8
	P3	7	9
Case 2	P1	11	NA
	P2	12	NA
	P3	9	NA

Note that overkill could also occur even if a chip is defective because a chip can operate correctly in the presence of some defects. For example, a chip with a defect on a false path could still operate correctly in a system because this defect is not sensitized in a system. However, this chip could fail a scan-based transition fault test if it sensitizes and tests a false path.

Fig. 1 shows the portion of a chip that contains three paths crossing at a node P. Let's assume P1 and P2 are false paths and P3 is a valid path. We will also assume that this circuit requires system clock with a period of 10ns.

We will first consider how overkill could occur with the presence of defects at a node P (case 1). Delays of three paths are given in Table 1 of case 1. Structural delay test pattern could test a delay defect at node P through P1, which is a false path. It would cause overkill because delay through this false path is greater than 10ns (Note that P1 is a long false path

because its delay is greater that the system clock period). However, the delay defect tested through P2 will not cause overkill because delay through this false path is smaller than 10ns. Hence, false path sensitization does not always result in the overkill occurrence. If a node P is stuck at 0 or 1, overkill would not occur even if a node P is tested through a long false path because a node P will also cause a valid path (P3) to fail the test. The node P stuck at 0 or 1 would not cause overkill only if there is no valid path crossing the node P. However, it is difficult to guarantee that defects tested through false paths do not include valid paths. Therefore, chips that fail SSF test would contain less overkill chips than chips that fail transition delay test. Hence, only the chips that pass SSF test but fail transition delay test will be considered in this report.

Overkill occurrence without the presence of defect is explained with Fig. 1 and Table 1 of case 2 (case2). P1 and P2 are long false paths, whose delay is greater than system clock period. If P1 or P2 is tested by a structural delay test, this chip will fail the test. However, this is good chip because the delay of the valid path P3 is smaller than system clock period. Therefore, overkill could happen. This may be responsible for many structural test failures.

We explained main sources of overkill and presented simple examples of how overkill could occur with or without the presence of defects.

This report is organized as follows.

Section 2 presents the two different nVidia test chips we used for this project.

Section 3 presents two test flows used for this project. Various structural test conditions are also presented in detail.

Section 4 presents the classification of our test samples. Based on various structural tests we applied, we classified the test chips into five categories: 1) structural test escapes 2) weak suspects 3) rated-speed failures 4) slow-speed failures 5) overkill candidates. This section provides criteria for the classification in detail.

Section 5 presents the experimental results on the potential cause of overkill. We will investigate the discrepancies between FP and FF devices in terms of scan cells and logic

design blocks. We will also investigate if there are design problems which cause FP devices to fail at the same scan cells and design blocks.

This report concludes with Section 6.

2 Test Chips

This section presents the two test chips used in the experiments. Table 2 presents the characteristics of the test chips.

Table 2 Characteristics of test chips

Test chip	Feature size of the Technology	Number of logic gates	Number of Flip-Flops	Number of Clock Domains	Number of I/Os
ELF14	0.14μm	3.8 million	NA	>10	>100
ELF13	0.13μm	7.2 million	NA	>10	>100

ELF14 is a graphics processor fabricated with 0.14μm technology. There are 3.8 million logic gates. It has about 57 million transistors and more than 10 clock domains. The nominal supply voltage is 1.44V. Three major clock domains operate more than 90% of the chip area. It has several hundreds of I/Os.

ELF13 is also a graphics processor using 0.13μm technology. It has 7.2 million logic gates and more than 10 clock domains. The nominal supply voltage is 1.355V and the number of I/Os is greater than those in ELF14.

3 Test flows

In this section, we will explain how test chips were collected and what tests were applied to them. The production test flow is used to collect the test chip samples. After collecting the samples, we applied various tests according to the experiment test flow in order to categorize the test chip samples and to analyze the difference between FP and FF devices.

3.1 ELF14 Production test flow

Fig. 2 presents the ELF14 production test flow.

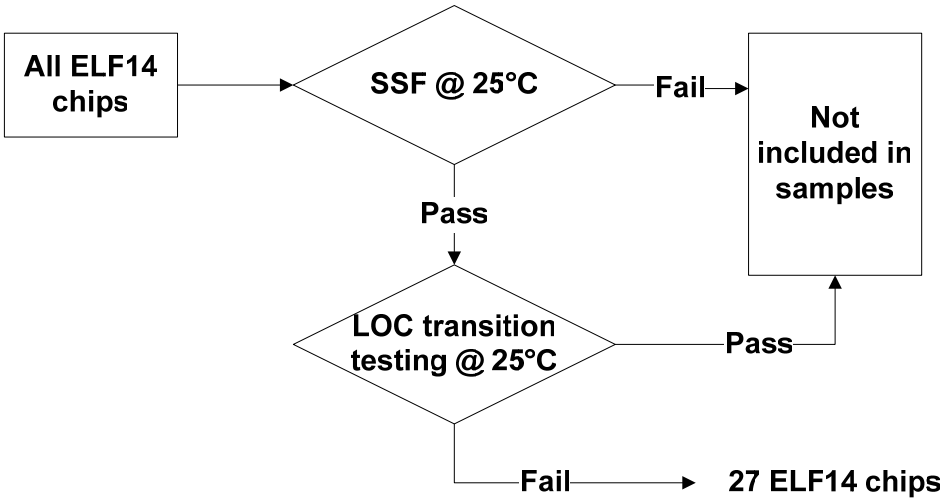

Figure 2 ELF14 Production test flow

NVidia selected 27 chips using their production test flow. Launch-On-Capture transition test patterns were applied to the test chips. *Launch-On-Capture* (LOC) transition test patterns force the scan enable signal to low after the scan chain data is shifted into the scan flip-flops. Subsequently, the system clock is applied twice to launch logic values and capture the response of the chip.

3.2 ELF14 Experiment test flow

Fig. 3 presents the ELF14 experiment test flow.

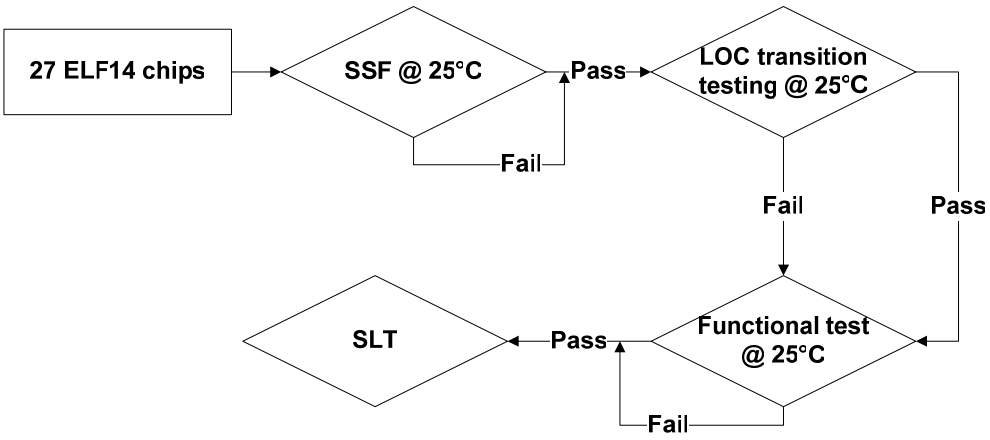

Figure 3 ELF14 experiment test flow

Our experiment test flow is applied to the 27 chips in order to characterize them.

SSF test set which is more thorough than the one in the production test flow is applied. Same LOC test set is used both in the production and experiment test flow. Table 3 presents the test sets applied to the ELF14 chips in the experiment test flow (NVidia does not allow publishing the test set length and fault coverage of LOC test set).

Table 3 Structural test sets for ELF14 experiment test flow

Test set	Number of test patterns	Fault coverage (%)
LOC	NA	NA
SSF	3734	96.89

Functional testing generated based on the Verilog simulation is also applied to the 27 chips.

In a *System Level Test (SLT)*, a chip is inserted in an actual system and tested whether it produces correct outputs in an actual system.

Structural tests and the functional test are applied at room temperature (25°C) and SLT is applied at system temperature.

3.3ELF13 Production test flow

Fig. 4 presents the ELF13 production test flow.

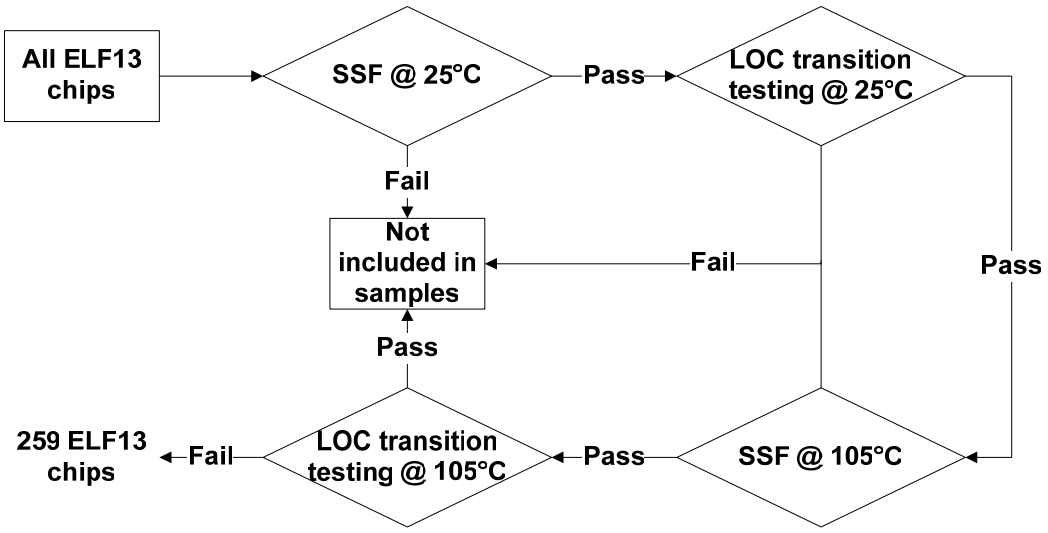

Figure 4 ELF13 Production test flow

NVidia selected 259 ELF13 chips using the production test flow. Chips that failed structural tests at room temperature were not included in our samples because nVidia assumes that they would only contain small number of potential overkill chips.

3.4 ELF13 Experiment test flow

More structural test sets were applied to those 259 chips using our experiment test flow in order to characterize them. Fig. 5 presents the experiment test flow.

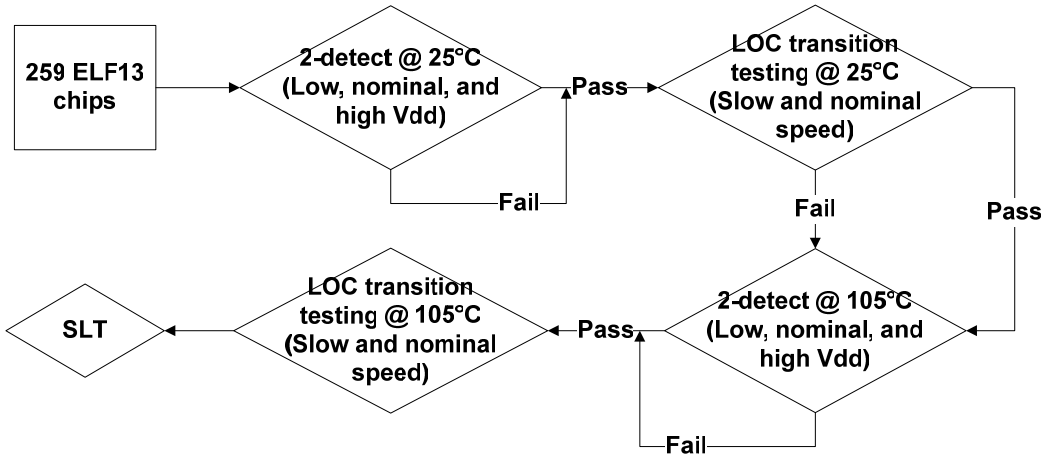

Figure 5 ELF13 experiment test flow

All the structural tests were applied at room (25°C) and hot (105°C) temperatures while SLT was only applied at room (25°C) temperature. Table 4 presents the test conditions applied in the experiment test flow in detail.

Table 4 Test conditions

Test	Test conditions			
	Test set	Speed (MHz)	Voltage (V)	Temperature (°C)
Test 1	LOC	Nominal	1.355	25
Test 2	LOC	10	1.355	25
Test 3	2-detect	<10	0.9	25
Test 4	2-detect	<10	1.355	25
Test 5	2-detect	<10	1.6	25
Test 6	LOC	Nominal	1.355	105
Test 7	LOC	10	1.355	105
Test 8	2-detect	<10	0.9	105
Test 9	2-detect	<10	1.355	105
Test 10	2-detect	<10	1.6	105

2-detect test patterns were applied at three different supply voltages to investigate the voltage dependent defects: low *Vdd (0.9V)*, nominal *Vdd (1.355V)*, and high *Vdd (1.6V)*. Low voltage value was selected under the following criteria: (1) this value should not cause good chips to fail (2) this value should not cause chips to fail during scan data loading. Table 5 presents the summary of the test length and the fault coverage of the test sets used in the experiment test flow.

Table 5 Structural test sets for ELF13 experiment test flow

Test set	Test set length	Fault coverage (%)
LOC	25,909	84.4%
2-detect	11,777	94.3%

4 Definitions, Test chip categories, and Results

In this section, we will categorize the test chips based on the experiments presented in section 3.2 and 3.4.

4.1 Definitions

4.1.1 Test escape

Various structural test sets as well as system level test are applied to our test chips. A chip that passes all the structural tests but fail system level test is called a *structural test escape*.

4.1.2 Rated-speed failure

A chip that passes slow speed test but fails nominal speed LOC transition delay test is called a *rated-speed failure*.

- In ELF14, SSF test is a slow speed test.
- In ELF13, slow speed LOC transition delay test and 2-detect test with nominal and high Vdd are slow speed tests.

4.1.3 Slow-speed failure

A chip that fails more than one slow speed test is called a *slow-speed failure*.

4.1.4 Weak suspect

Weak ICs contain *flaws*, which are defects in a chip that do not cause failures under normal operating conditions but result in degradation in chip performance or noise immunity. Weak chips due to certain flaws can be easily detected at certain lower-than-normal power supply voltage [Hao 93]. In ELF13, a chip that fails 2-detect test with low Vdd but passes all other structural tests is categorized as a weak suspect. We did not apply the low voltage test to ELF14. Therefore, weak suspects are not available for ELF14.

4.1.5 Overkill candidate

A chip that passes the System Level Test, functional test, but fails structural tests is called an *overkill candidate* because they are not identified as good chips.

4.2 Results of test chip classification

4.2.1 ELF14

Table 6 presents the test results of ELF14.

Table 6 ELF14 test results

Chip ID	SSF	LOC	Functional	SLT	Overkill candidate
1	P	F	P	F	N
2	P	F	P	P	Y
3	P	F	P	P	Y
4	P	F	P	P	Y
5	P	F	P	P	Y
6	P	F	P	P	Y
7	P	F	P	P	Y
8	P	F	P	F	N
9	F	F	P	F	N
10	P	F	P	F	N
11	F	F	P	P	Y
12	P	F	P	F	N
13	P	F	F	P	N
14	P	F	P	P	Y
15	P	F	P	P	Y
16	P	F	P	P	Y
17	F	F	P	F	N
18	P	F	F	F	N
19	F	F	F	F	N
20	F	F	P	F	N
21	P	F	P	F	N
22	P	F	P	F	N
23	F	F	P	P	Y
24	P	F	P	P	Y
25	P	F	P	P	Y
26	P	F	P	P	Y
27	P	F	P	P	Y

Table 7 presents the classification of the ELF14 test chips.

Table 7 ELF14 test chip classification

Category	System Level Test/Functional Test		Total
	Pass	Fail	
Structural test escape (TE)	0	0	0
Rated-speed failure	13	8	21
Slow-speed failure	2	4	6
Overkill candidate	15	0	15

4.2.2 ELF13

Table 8 presents the test results of ELF13 classification.

Table 8 ELF13 test chip classification

Temperature	Category	System Level Test		Total
		Pass	Fail	
Hot temperature only	Structural test escape (TE)	NA	0	2
	Rated-speed failure	91	21	112
	Slow-speed failure	23	6	29
	Weak suspect (WS)	15	3	18
	Overkill candidate	129	0	129
Room temperature only	Structural test escape (TE)	NA	26	26
	Rated-speed failure	1	0	1
	Slow-speed failure	10	2	12
	Weak suspect (WS)	20	2	22
	Overkill candidate	31	0	31
Hot and room temperature	Structural test escape (TE)	NA	7	7
	Rated-speed failure	20	21	41
	Slow-speed failure	7	7	14
	Weak suspect (WS)	13	4	17
	Overkill candidate	40	0	40

Note that our samples pass the LOC transition delay test at room temperature but we observe some rated-speed failures. This is because the LOC transition delay test set applied at the experiment test flow has higher fault coverage than the LOC transition delay test set applied at the production test flow.

5 Potential cause of overkill

In the following sections, we will investigate failing scan cells and failing design blocks of FP and FF devices. We will also investigate if there are design problems that cause overkill candidates to fail at the same logic design blocks or the same scan cells.

5.1 Preliminaries

In this section, new terminology and key observations will be introduced.

Definition 5.1.1 (Failing scan cell): A scan cell that captures the failing bits is called a *failing scan cell*.

We will explain more terminologies using the example test results in Table 9.

Chip 1, 2, and 3 fail structural test. Chip 1 and 3 pass SLT and chip 2 fail SLT. The failing bits of chip 1 are captured in scan cell 1 and 2.

Table 9 Example of Test Results

Chip	1	2	3
Structural test	F	F	F
SLT	P	F	P
Failing scan cells	1, 2	2, 3	2

Definition 5.1.2 (Overkill candidate, FP device, FF device): A chip that fails structural tests but passes System Level Test and functional test is called *overkill candidate*, because it is not yet known whether it is actually a good chip (also called *FP devices*). FP stands for Fail structural test and Pass SLT.

A chip that fails the structural test and fails either SLT or functional test is called an *FF device.* FF stands for Fail structural test and Fail SLT.

Example 5.1.2: Chips 1 and 3 exemplify FP devices. Chip 2 is an example of an FF device.

Definition 5.1.3 (FP failing scan cell, FF, or Common): A chip that fails the structural test can either pass or fail SLT. The failing scan cell of a chip that passes SLT is called *FP failing scan cell.* The failing scan cell of a chip that fails SLT is called *FF failing scan cell.* A failing scan cell that is called FP failing scan cell and FF failing scan cell is also called *Common failing scan cell.*

Example 5.1.3: Scan cells 1 and 2 are categorized as FP failing scan cells because they capture the failing bits of chip 1 and 3, which pass SLT.

Scan cells 2 and 3 are FF failing scan cells because they capture the failing bits of chip 2, which fails SLT.

Note that scan cell 2 is called both an FP failing scan cell and FP failing scan cell. Hence, we call scan cell 2 a common failing scan cell.

Definition 5.1.4 (FP only failing scan cell, FF): A failing scan cell that is an FP failing scan cell, but is not common failing scan cell is called an *FP only failing scan cell*. FP failing scan cells are the union of the common failing scan cells and the FP only failing scan cells. A failing scan cell that is an FF failing scan cell, but is not common failing scan cell is called an *FF only failing scan cell*. FF failing scan cells are the union of the common failing scan cells and the FF only failing scan cells.

Example 5.1.4: A scan cell 1 is an FP only failing scan cell because it is an FP failing scan cell, but not a common failing scan cell. A scan cell 3 is an FF only failing scan cell because it is an FF failing scan cell, but not a common failing scan cell.

5.2 Scan cell comparison between FP and FF devices

In this section, failing scan cells of FP devices will be compared to those of FF devices.

5.2.1 Results

Failing scan cells from 21 ELF14 rated-speed failures were collected. Among 21 chips, 13 chips pass SLT and 8 chips fail SLT. In order to collect as many failing scan cells as possible, structural testing was continued until the tester could accommodate. Fig. 6 summarizes the comparison of the number of failing scan cells of the LOC transition test.

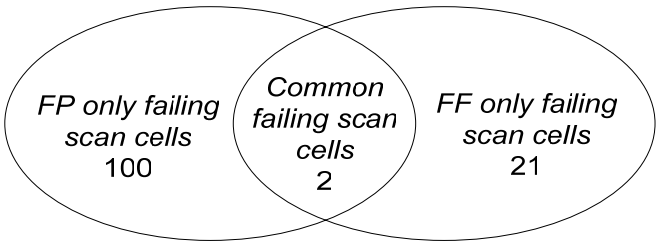

Figure 6 Comparison of the number of failing scan cells for ELF14

Failing scan cells from 112 ELF13 rated-speed failures were collected. Among those 112 chips, 91 chips pass SLT and 21 chips fail SLT. Fig. 7 presents the comparison of the number of failing scan cells of the LOC transition test.

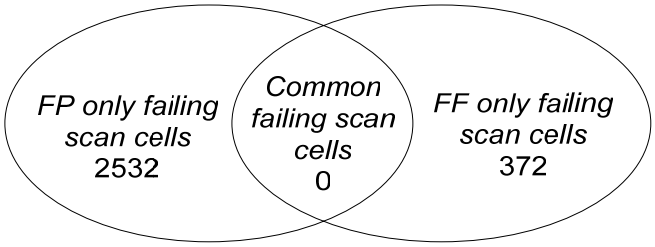

Figure 7 Comparison of the number of failing scan cells for ELF13

5.2.2 Observations

From our experiments, we can make the following three observations:

1. Some failing scan cells are only associated with FP devices. These scan cells could be associated with overkill candidates. These scan cells can be considered false failing scan cells. For example, false paths could be sensitized through those scan cells.
2. Some failing scan cells are only associated with FF devices. Hence, those scan cells only capture the valid failing bits and are not associated with overkills.
3. Only a very few failing scan cells (<2%) capture failing bits associated with both FP and FF devices.

5.3 Failing scan cell comparison among FP devices

In this section, we will provide the experimental results on how many FP devices have the same failing scan cells. We will investigate if there are failing scan cells that are repeatedly observed across FP devices.

Failing scan cells collected from 13 of ELF14 FP devices and 91 of ELF13 FP devices are analyzed to find out if they fail at the same scan cells.

Fig. 8 presents the failing scan cell distribution of FP devices in ELF14 chips.

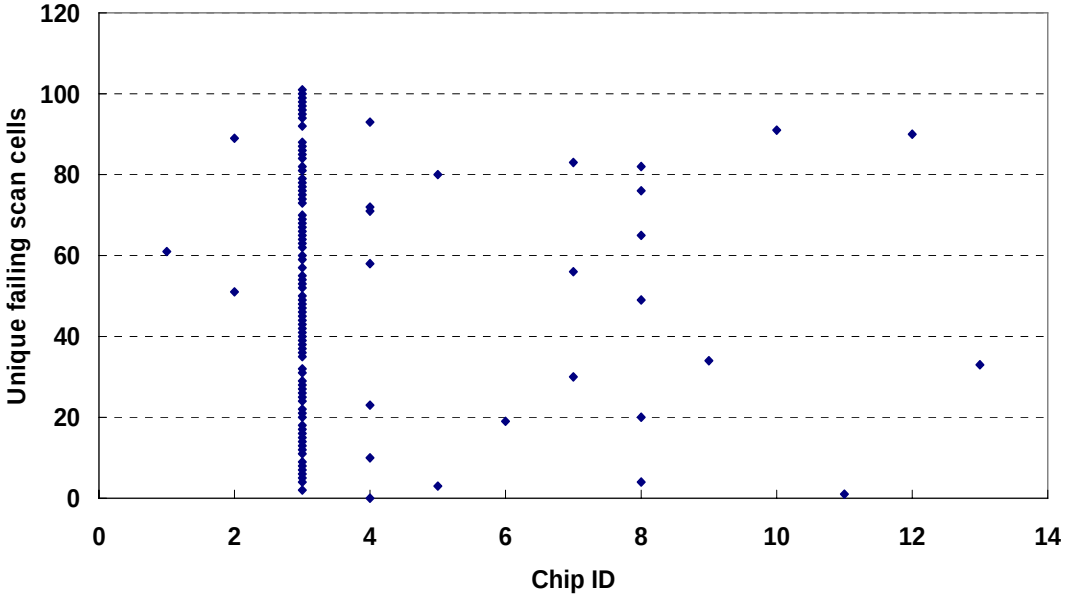

Figure 8 Failing scan cell distribution of FP devices - ELF14

X axis represents 13 of ELF14 FP devices. Y axis represents the unique failing scan cells collected from each FP device. Netlist names of failing scan cells are replaced with numbers from 0 to 101, which correspond to 102 unique failing scan cells collected from FP devices. If a certain failing scan cell appeared from all FP devices, a horizontal line corresponding to this failing scan cell is marked in Fig. 8. As can be seen from Fig. 8, failing scan cells are randomly distributed over FP devices and no horizontal line is observed. Fig. 9 presents the same plot for 91 of ELF13 chips. We can also observe the random distribution of failing scan cells in ELF13 chips. Fig. 10 (ELF14) and 11 (ELF13) present the number of unique failing scan cells and the number of FP devices from which those failing scan cells are collected.

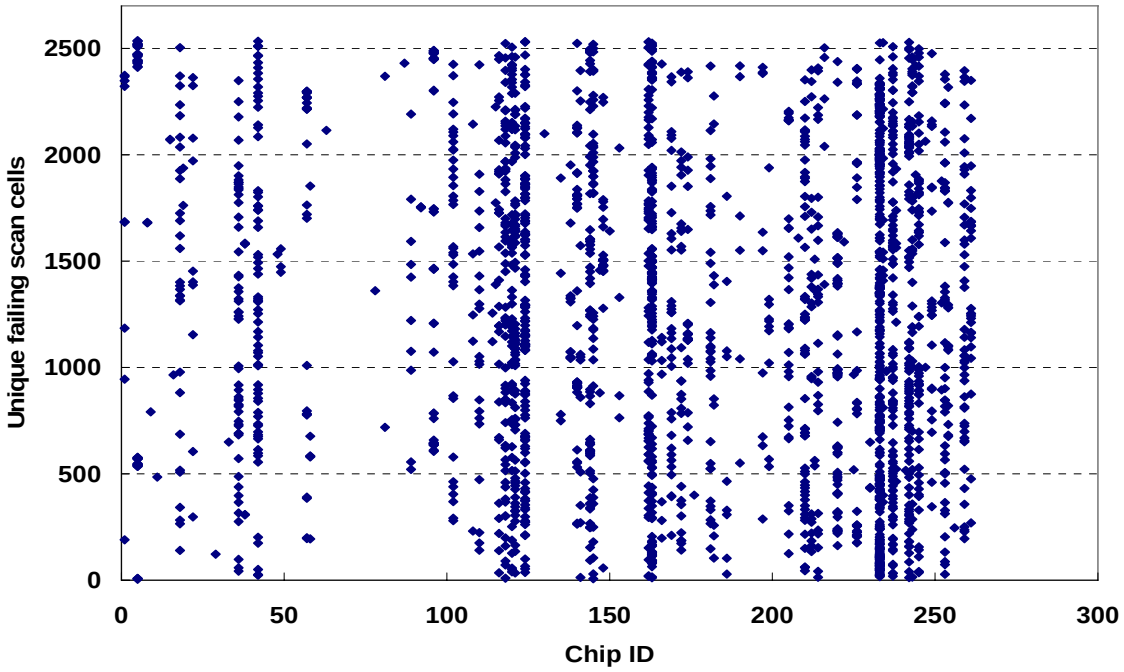

Figure 9 Failing scan cell distribution of FP devices - ELF13

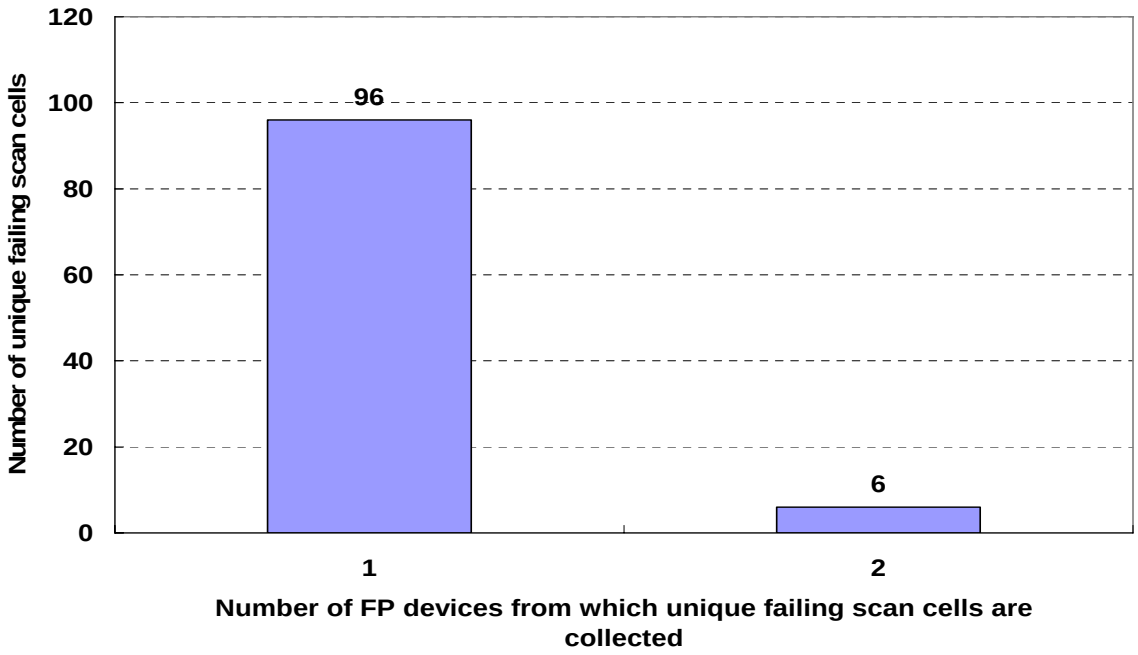

Figure 10 FP devices vs. unique failing scan cells - ELF14

96 (94.1%) out of 102 failing scan cells are observed from one FP device and they are not repeatedly observed from other FP devices (see Fig. 10). There are 6 failing scan cells

that can be obtained from two different FP devices. No failing scan cells are observed from more than three different FP devices.

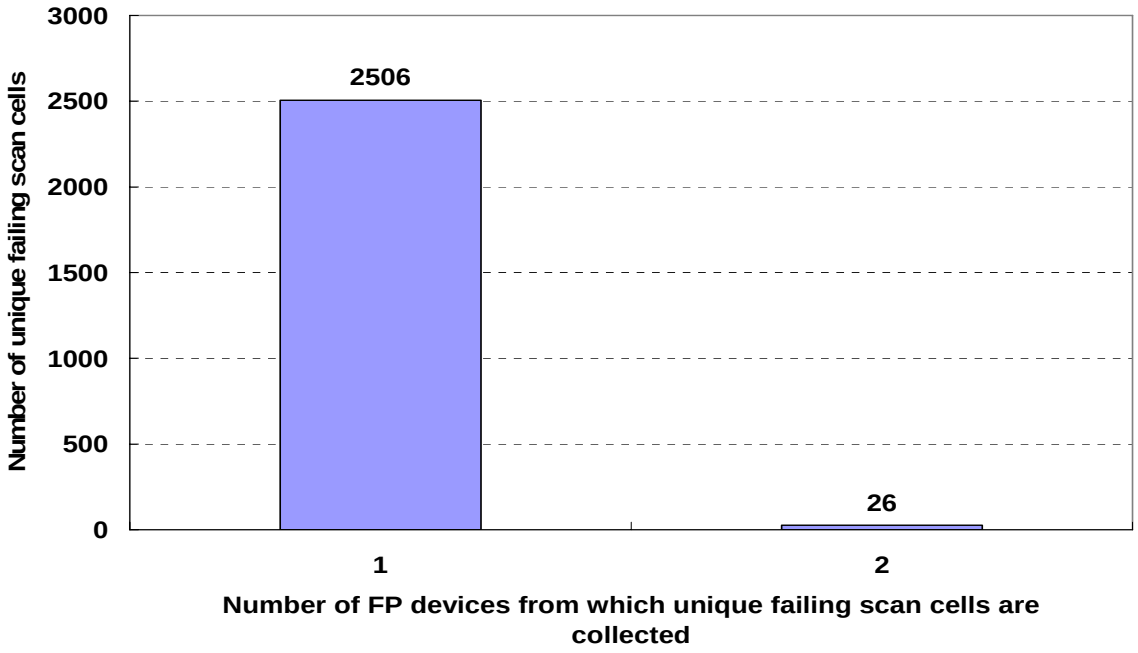

Figure 11 FP devices vs. unique failing scan cells - ELF13

2506 (98.9%) out of 2532 failing scan cells are observed from one FP device in ELF13 (see Fig. 11). 26 failing scan cells are observed from two different FP devices. As can be seen from ELF14 chips, there is no failing scan cell that is coming from more than three different FP devices.

From the above experimental results, we can draw the following conclusions on the potential cause of overkill occurrence.

There is no scan cell that consistently captures the failing bits in FP devices and each FP device has its own failing scan cells that are not repeated from other FP devices. This implies that there could be little design problems in the occurrence of potential overkills. In the following section, design issues will be further investigated by comparing the logic design blocks that could cause the overkill candidates. Furthermore, we cannot predict the failing scan cells that would cause a good chip to fail structural tests based on the samples of overkill.

5.4 Design block comparison between FP and FF devices

Faults that could cause a chip to fail a structural test were collected. Faults obtained from FP devices will be compared to those obtained from FF devices. Experiments were conducted on 112 of ELF13 rated-speed failures at hot temperature only.

A fault could cause a chip to fail a structural test (also called a *candidate fault*). Fig. 12 presents the flow to obtain the candidate faults.

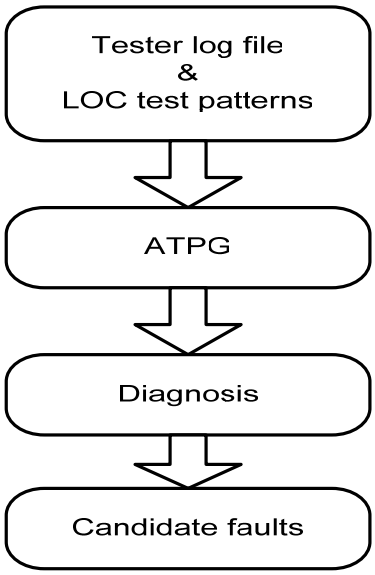

Figure 12 Flow to obtain candidate faults

Many commercial ATPG tools provide diagnostic capability to obtain candidate faults. They can calculate the candidate faults based on the failing patterns and failing scan cells collected from an ATE. *FP candidate faults* are the candidate faults collected from FP devices and *FF candidate faults* are the candidate faults collected from FF devices. *Common candidate faults* are the candidate faults obtained both from FP devices and FF devices. 2532 FP candidate faults were collected from 91 rated-speed failures of FP devices and 372 FF candidate faults were collected from 21 rated-speed failures of FF devices. No common candidate faults were found in this experiment.

Current chip design consists of several design blocks which consist of many sub-design blocks. Fig. 13 illustrates the hierarchical levels of design blocks.

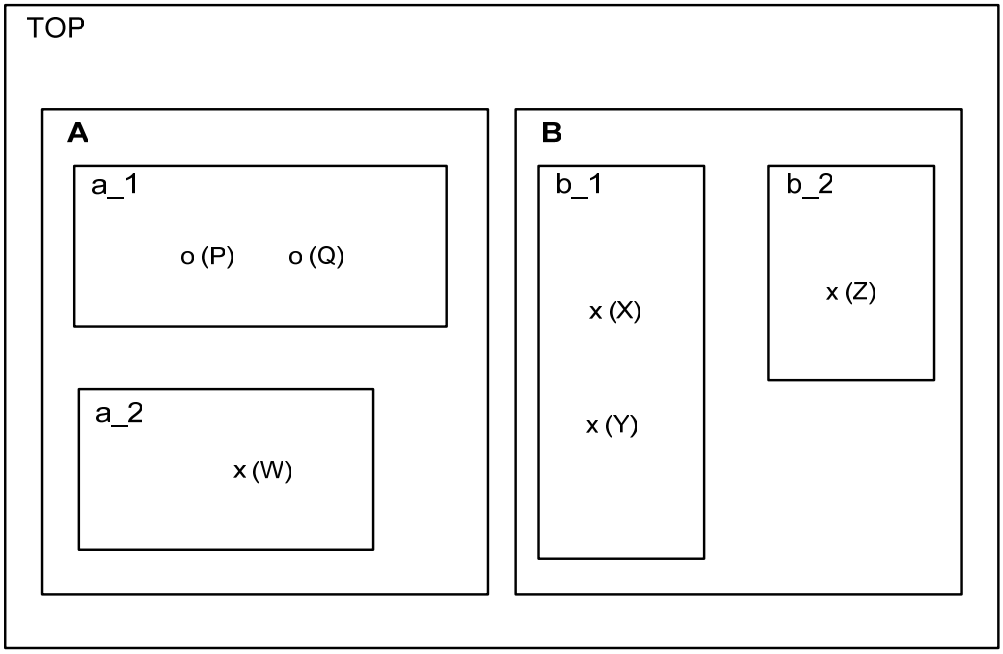

Figure 13 Design level - example

Each rectangle represents design block. Labels at the upper left corner of each rectangle represent the names of the design blocks and design levels. TOP block is the highest level in the hierarchy of an example chip, which is the chip itself. TOP block consists of two sub-design blocks A and B, which are the first level. First level of sub-design blocks contain second level sub-design blocks, which are a_1, a_2, b_1, and b_2. A design block that contains candidate fault(s) is called a *failing design block*. An *FP failing design block* is a failing design block that contains FP candidate fault(s). Two circles (P and Q) in sub-block A represent FP candidate faults. A design block A is an FP failing design block at the first level because it contains FP candidate faults P and Q. A design block a_1 is also an FP failing design block at the second level. Note that failing design blocks can be defined at each design level. An *FF failing design block* is a failing design block that contains FF candidate fault(s). Four Xs (W, X, Y, and Z) in sub-block A and B represent FF candidate faults. Design blocks A and B are FF failing design blocks at the first level because they contain FF candidate faults W, X, Y, and Z. A failing design block that contains FP and FF candidate faults is called a *common failing design block*. A design block A is a common

design block at the first level because it contains FP candidate faults P, Q and an FF candidate fault W. Table 10 summarizes the design blocks depending on the design levels.

Table 10 Candidate faults comparison vs. design level – example

Design level	Name of design block considered	FP failing design blocks	FF failing design blocks	Common failing design blocks
0	TOP	TOP	TOP	TOP
1	A, B	A	A, B	A
2	a_1, a_2, b_1, b_2	a_1	a_2, b_1, b_2	None

From the failing scan cell comparison, we discovered that there is few failing scan cells that are common in both FP and FF devices.

Table 11 presents the comparison of failing design blocks in ELF13.

Table 11 Failing design block comparisons

Design level	Number of FP failing design blocks	Number of FF failing design blocks	Number of common failing design blocks
1	10	8	6
2	263	34	6
3	293	50	9
4	312	66	10
5	541	82	14
6	1548	302	11
7	3298	500	3
8	5285	668	0

ELF13 has more than 15 design levels. Table 11 shows that there are no failing design blocks associated with both FP and FF devices from the 8^{th} design level. Experimental results are consistent with the results from failing scan cell comparisons. Failing bits in FP devices come from the specific design blocks which are different from FF devices and those failing bits are propagated to the specific scan cells where the failing bits from FF devices are not propagated to.

From our experiments, following observations can be made:

1. Some design blocks containing FP candidate faults at design level 8 or below are only associated with the chips that pass SLT. These failing design blocks are associated with overkill candidates.
2. Some design blocks containing FF candidate faults at design level 8 or below are only associated with the chips that fail SLT. Hence, those failing design blocks correspond to the valid failures and are not associated with overkills.
3. Failing design blocks in 1 and 2 do not overlap each other at design level 8 or below. This implies that the chip is designed such that some logic blocks contain false paths that could cause the overkill. Those logic blocks do not overlap with the logic blocks that could cause the valid failures.

5.5 Design block comparison among FP devices

In this section, we will compare failing design blocks among FP devices in order to find if there is any design issue which causes FP devices to fail at the same design blocks. Table 12 presents how many failings design blocks come from how many different FP devices according to the design levels.

Table 12 Failing design block comparison among FP devices – ELF13

Design level	Number of failing design blocks from one FP device	Number of failing design blocks from more than two different FP devices
1	0 (0%)	10 (100%)
2	253 (96.2%)	10 (3.8%)
3	279 (95.2%)	14 (4.8%)
4	294 (94.2%)	18 (5.8%)
5	503 (92.9%)	38 (7.1%)
6	1514 (97.8%)	34 (2.2%)
7	3269 (99.1%)	29 (0.9%)
8	5230 (98.9%)	55 (1.1%)

Except the first design level, less than 10% of failing design blocks are repeatedly observed from more than two different FP devices. Failing design block comparisons in conjunction with failing scan cell comparisons imply that there could be little design issues causing FP devices to fail at the same scan cells and design blocks.

6 Summary and future work

This report investigates the potential cause of overkills. Experiments were conducted on two different designs of graphics processor from nVidia with two structural test sets consisting of 10 different test conditions and SLT.

Test chips were classified into 5 categories based on the test results. 43% (112 chips) of the ELF13 chips behaved as rated-speed failures at hot temperature only. Among them, 35% (91 chips) pass SLT and 8% (21 chips) fail SLT.

Rated-speed failures were further analyzed to investigate the potential cause of overkills. We observed that FP and FF devices fail at different scan cells and logic design blocks. We also investigated if there is any design problem that could cause the overkill candidates to fail structural tests systematically. Our experimental results show that the test chip design does not contain any failure mechanism that could cause potential overkills to fail at the same scan cells or logic design blocks.

We will conduct more thorough diagnosis to locate the defects and to understand the defect mechanisms in overkill candidates. Thorough defect characterization of FP devices will include the path delay tests which will be generated for paths that pass through candidate faults and will be applied to further isolate the defect locations.

7 Acknowledgements

This research is funded by SRC under contract No. 1175.001. This research is cooperation with nVidia. We would like to thank Bruce Cory of nVidia for his valuable help. We also would like to thank to Subhasish Mitra of Intel and Stanford CRC, Erik Volkerink of Agilent and Stanford CRC, and Francois-Fabien Ferhani of Stanford CRC for their valuable comments and suggestions.

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